

IMPROVEMENTS IN OR RELATING TO RANGEFINDERS

The present invention relates to rangefinders, and more particularly to rangefinders wherein a beam of light is projected on a scene to illuminate a small area on an object, and an image sensor senses the location of the small area in an image of the scene to determine the distance to the object in the scene.

Automatic rangefinders are known in which a beam of light is projected upon an object in a scene to form an illuminated small area on the object. An image of the scene, including the illuminated small area, is formed on a linear image sensor. The location of the image of the illuminated small area along the image sensor is determined by the range of the object in the scene. Conversely, the range of the object can be determined from knowledge of which sensor the image of the illuminated area is incident upon. Such a rangefinding device finds application for example in an automatic focusing camera.

The general arrangement of elements and mode of operation of such a known rangefinding device will be described with reference to FIG. 1. Means for projecting a beam of light is shown by way of example as a light emitting diode (LED) 1 and a lens 2. The beam is projected along a path 3 to illuminate a small area on an object O_1 in a scene. The scene is imaged by a second lens 4 onto an image sensor comprising a linear array 5 of photosensors. The signals produced by the photosensors are analyzed by control electronics 6 to determine the position of the illuminated small area in the scene and produce a signal 7 representing the range of the object.

As shown by example in FIG. 1, the apparent position of the illuminated small area in the scene

is a function of distance along light path 3 to the object. For an object O_1 located at a distance D_1 from the rangefinding device, the image of the illuminated small area will fall on the array 5 at a location S_1 . For an object O_2 at a further distance D_2 , the image of the small area will fall on the array 5 at a location S_2 . By examining the output of the array 5, the control electronics 6 determines (for example, by comparing the outputs of the sensors to determine that output which is a maximum) the location of the illuminated small area in the scene and thereby the range of the object.

When the ambient illumination is relatively bright, the scene itself, regardless of the illuminated small area, will produce substantial modulation of the photosensor array. Under such circumstances, it may not be possible to determine the location of the illuminated small area merely by examining the outputs of the photosensors. The effects of ambient scene light can be removed however by operating the sensor with the beam off and again with the beam on, and subtracting the signals produced thereby. The information in the difference signal is solely from the illuminated small area. One way of accomplishing this subtraction is described in US-A-4274735.

US-A-4274735 describes a device having a pair of memory capacitors associated with each photosensor in the array. The capacitors are selectively connectable to the photosensors by field effect transistor (FET) switches, and each pair is further connectable to an associated differential amplifier. In operation, a photosensor is first connected to one of the capacitors while the light beam is off. The photosensor is then connected to the other capacitor

while the light beam is on. Both the capacitors are then connected to the differential amplifier to produce a signal free from background information. The signals are compared in an array of comparators to determine the location of the illuminated small area by sensing the largest difference signal from the array of differential amplifiers.

To effectively remove the relatively large signal due to background light from the relatively small signal due to the illuminated small area, each of the differential amplifiers must have very good common mode rejection. Furthermore, so that the amplifiers themselves do not introduce overwhelming pattern noise into the signals, they must be very closely matched. The need for a plurality of closely matched differential amplifiers exacts a high price on any attempt to increase the signal-to-noise ratio of the device.

Furthermore, the use of an array of comparators to determine the maximum difference signal from the differential amplifiers complicates the signal processing circuitry.

It is an object of the present invention to simplify the signal processing electronics of a rangefinder while improving the signal-to-noise ratio achievable therein.

According to the present invention there is provided a device for finding the range of an object in a scene, including means for projecting a beam of light to illuminate a small area on the object, a plurality of photosensors for producing signals indicative of the amplitude of light incident on them from respective portions of the scene including portions at different ranges along the path of the beam, means for identifying the photosensor upon which is incident light from said small area on the

object, said identifying means including charge storage means for storing charge discretely from each photosensor, switching means for selectively connecting the photosensors to the storage means to
5 add charge to the storage means when the light beam is turned on and to remove charge from the storage means when the light beam is turned off, the greatest stored charge after a complete cycle of charge addition and removal being associated with
10 the photosensor upon which light from the said small area is incident, the range of the object being determinable from knowledge of which photosensor has associated with it said greatest stored charge.

15 Each photosensor may be a photodiode and the charge storage means may include a plurality of diodes. The switching means may include FET transistors connecting each photodiode to its respective storage diode in a bridge configuration.

20 The photosensors preferably are disposed in a linear array.

The charge remaining in each storage diode after a complete cycle constitutes a difference signal. The device may further include a charge
25 coupled device shift register and transfer gate means for transferring the difference signals from the storage diodes in parallel into the shift register whereby the difference signals delivered from the shift register may be compared to
30 determine the range of the object.

The present invention will now be described, by way of example, with reference to Figs. 2 to 11 of the accompanying drawings, in which:-

FIG. 2 is a schematic diagram of a bridge network photosensitive element for use in an image sensor in an embodiment of the present invention;

5 FIG. 3 is a schematic diagram of an image sensor including a bridge network photosensitive element as illustrated in Fig. 2;

10 FIG. 4 is a partial plan view showing the storage diodes and charge transfer gates of the charge coupled device shift register in an integrated image sensor as illustrated in Fig. 3;

FIG. 5 is a partial plan view showing the bridge network of switches and photosensors in the integrated image sensor;

15 FIG. 6 is a partially broken-away perspective view showing the channels and electrode structure of the bridge network of switches and the photosensor;

20 FIG. 7 is a schematic block diagram showing the signal processing and control electronics of a rangefinder, having the bridge network image sensor, according to the present invention;

25 FIG. 8 is a schematic diagram showing the signal processing electronics for reading out and peak detecting the signal produced by the image sensor;

FIG. 9 is a flow chart showing the general operation of the rangefinder illustrated in Figs. 2 to 8; and

30 FIGS. 10 and 11 are timing diagrams useful in explaining the operation of the rangefinder embodying the present invention.

Referring first to FIG. 2, a photosensitive element, generally designated 10, includes a
35 photosensor, such as a photodiode 12, charge storage means, such as a storage diode 14, and four FET

switches 16, 18, 20 and 22 forming a bridge network for controllably connecting the photodiode 12 between a bias voltage $\pm V_B$ and the cathode of storage diode 14. When FET switches 16 and 20 are open, and switches 18 and 22 are closed, the photodiode 12 is connected to the storage diode 14 anode-to-cathode and current generated by the photodiode 12 flows in the direction of the solid arrows to accumulate charge on the capacitance of storage diode 14. Conversely, when FET switches 18 and 22 are open and 16 and 20 are closed, the photodiode 12 is connected to the storage diode 14 cathode-to-cathode and current generated by the photodiode 12 flows in the direction of the phantom arrows to remove charge from the storage diode 14. The state of FET switches 18 and 22 is controlled by a bridge control signal ΦB_1 applied to their respective gates, and the state of FET switches 16 and 20 is controlled by a bridge control signal ΦB_2 .

Storage diode 14 is charge coupled to the charge transfer channel of a charge coupled device (CCD) shift register (not shown in FIG. 2) by a transfer gate 24 (shown in phantom since it is not a part of bridge network photosensitive element 10). Net charge accumulated on storage diode 14 is transferred to the CCD device by applying a transfer signal T_1 to the transfer gate 24. One of the transfer electrodes 26 (shown in phantom) of the CCD shift register is shown in FIG. 2.

The CCD shift register is arranged to transfer the charge in a direction generally perpendicular to the plane of the drawing in FIG. 2.

In operation, the bias voltage $\pm V_B$ is set for earth and bridge control signals ΦB_1 and ΦB_2 are applied to momentarily close all

four FET switches 16, 18, 20, and 22 to initialize the photodiode 12 and the storage diode 14. Next, bridge control signals ΦB_1 and ΦB_2 are applied to the FET switches to connect the photodiode 12 to the storage diode 14 anode-to-cathode and a positive bias voltage $+V_B$ (e.g. +5 volts) is applied to reverse bias the photodiode 14. The photodiode 12 is exposed to light for a predetermined time during which a charge is accumulated on the storage diode 14. Then, the bridge control signals ΦB_1 and ΦB_2 are reversed to connect the photodiode 12 to the storage diode 14 cathode-to-cathode, and the polarity of the bias voltage $-V_B$ is inverted (e.g. -5 volts) to maintain the reverse bias on the photodiode 12. The photodiode 12 is exposed to light for a second predetermined time interval during which charge is removed from the storage diode 14. After the second exposure, bridge control signals ΦB_1 and ΦB_2 may be applied to disconnect the photodiode 12 from the storage diode 14, or the steps of accumulating and removing charge from the storage diode 14 may be repeated several times before disconnecting the photodiode 12, to improve the signal to noise ratio of the device. The charge remaining on the storage diode 14 is the difference between the amount of charge applied to the storage diode 14 and the amount of charge removed. As explained below, this feature is employed in a rangefinder to remove the contribution due to the ambient illumination from the charge produced by the photosensitive elements.

Referring now to FIG. 3, a linear image sensor, generally designated 28, includes a linear array of bridge network photosensitive elements 10 each as described above. The storage diodes 14 are charge coupled to a CCD shift register 30 by

transfer gate 24. CCD shift register 30 is a conventional four-phase buried channel CCD shift register controlled by four-phase clock signals ϕ_{1-4} and having an output diode 32. An output preamplifier 34 detects the signal on the output diode 32.

Charges accumulated in the storage diodes 14 are transferred in parallel under control of transfer signal T_1 in the direction of arrows X into the CCD shift register 30, and are then shifted serially in the direction of arrow Y under control of the four-phase clock signals ϕ_{1-4} to output diode 32. The signals are detected at the output diode 32 by output preamplifier 34.

Preferably, the array of bridge network photosensitive elements 10 and the CCD shift register 30 are integrated on a common substrate, using well known integrated circuit techniques. An embodiment of the integrated image sensor will now be described with reference to FIGS. 4, 5 and 6.

FIG. 4 is a partial plan view illustrating the storage diodes 14 of the photosensitive elements 10, the transfer gate 24, and the electrode and channel structure of the CCD shift register 30.

The device was constructed using well known CMOS fabrication techniques in a p-well 35 on an n-type silicon substrate 36. The device is constructed in isolating wells using CMOS technology so that the photodiodes described below will be electrically isolated from the rest of the circuit. The CCD shift register 30 is of the buried channel variety, employing an n-type region 38, as shown by chain lines in the p-well 35, to form the buried charge transfer channel. The storage diodes 14 are formed by n+-type regions in the p-well substrate 36. Channel stopping regions 40 shown by cross-hatching

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surrounding the storage diodes 14 and the CCD shift register channel, comprise, for example, p⁺-regions under thickened field oxide. Contact to the p-well 35 is provided by contact windows 43 in the p⁺-regions of the p-well 35. Gaps 42 in the channel stopping regions 40 between the storage diodes 14 and the region 38 of the CCD shift register 30 allow the formation of surface channels communicating between the storage diodes 14 and the CCD shift register 30.

Two levels of polysilicon overlying the surface and buried channels define the transfer electrode structure of the CCD shift register 30 and the transfer gate 24.

A first level of polysilicon defines the phase-2 and phase-4 transfer electrodes (44 and 46 respectively) of the CCD shift register 30, and a second level defines the phase-1 and phase-3 electrodes (48 and 50 respectively) and the transfer gate 24. When voltage is applied to the transfer gate 24 and the phase-2 electrode 44, a surface channel is formed along the gaps 42 in the channel stopping regions 40, thereby charge coupling the storage diodes 14 with the CCD shift register 30.

FIG. 5 is a partial plan view of the bridge network and the photodiode of the photosensitive elements, wherein features have been added to each successive column starting on the left and culminating in a fully formed bridge network photosensing element in the column on the far right. The FET switches 16, 18, 20 and 22 and the photodiode 12 are formed in p-wells 52 (see first column) in the n-type substrate 36. As illustrated in the second column of FIG. 5, n-type regions 54 in the p-wells 52 form the sources and drains of the FET switches, and the junction for photodiode 12. p⁺-

type regions 56 allow for ohmic contact to be made to the substrate of the FET switches and the anode of photodiode 12.

As shown in the third column of FIG. 5, the first level of polysilicon is patterned to define horizontal conductors 58 and the second level of polysilicon is patterned to define the gates and interconnections of the gates for the FET switches. A first conductor pattern 60 defines interconnected gates 64 and 68 for FET switches 18 and 22 respectively. A second conductor pattern 66 defines interconnected gates 62 and 70 of FET switches 16 and 20 respectively. Finally, the column on the far right shows the bridge network photosensitive element with aluminium conductor patterns that complete the circuit. A conductor 72 connects the bias voltage $\pm V_B$ to the sources 74 and 76 of FET switches 22 and 16 respectively. A conductor 78 connects the drain 80 of FET 22 to the cathode 82 of photodiode 12. A conductor 84 connects the drain 86 of FET 16 to the anode 88 of photodiode 12. A conductor 90 connects the cathode 82 of photodiode 12 to the source 92 of FET 20. A conductor 94 connects the anode 88 of the photodiode 12 to the drain 96 of FET 18, and a conductor 98 connects the drain 100 and the source 102 of FETs 20 and 18 respectively to the cathode of storage diode 14 (see FIG. 4). Finally, conductors 104 connect the substrates of the FET switches 16, 18, 20, and 22 to the horizontal conductors 58 for applying a substrate bias.

FIG. 6 is a perspective view of a portion of one of the bridge network photosensitive elements with the substrate broken away to reveal a cross section of the device along a line through the middle of the FETs 16, 18, 20 and 22 and photodiode

12. Not shown in FIG. 6 are the layers of insulating oxide between the respective layers of polysilicon and aluminium conductors, which are provided in a known manner according to well known integrated circuit manufacturing techniques.

— Referring now to FIG. 7, overall control of the rangefinder is provided by a programmed microprocessor 106, (or alternatively with custom integrated circuits designed to perform the same functions and integrated on the same chip as the image sensor) through conventional driver circuits 108. The microprocessor 106 is supplied with timing signals from a clock circuit 110 and with power via a main power switch 112 from a battery 114.

Four-phase clock signals ϕ_1 -. ., a transfer signal T_1 , bias voltage $\pm V_B$ and bridge control signals ϕB_1 and ϕB_2 are supplied to the linear image sensor 28 from driver circuits 108 under control of microprocessor 106 to produce output signals from the CCD shift register of the image sensor 28. The signals from the CCD shift register are sampled by a sample and hold circuit 111 and are supplied to a peak detector 113 that produces a pulse each time a signal larger than any previous signal is produced by image sensor 28. The output of peak detector circuit 113 is supplied to a latch circuit 115. Latch circuit 115 is connected to receive the output count of a digital counter 116. Counter 116 receives a reset signal R and a timing signal ϕ_T , having the same frequency as the four-phase clock signals ϕ_1 -. . The output of the latch circuit 115 is supplied to an input port of microprocessor 106.

The driver circuit 108 also powers an LED 117 and an output device 118 such as a range display or a range servo. LED 117 preferably emits infra-red light.

FIG. 8 is a more detailed circuit schematic of the output preamplifier 34 of the image sensor 28, the sample and hold circuit 111, and the peak detector 113. A portion of the CCD shift register 30 showing an output gate 120 and an output diode 32 are also shown.

The output preamplifier 34 is an on-chip sense and reset amplifier including a sense FET 122 and a reset FET 124. The sense FET 122 is a surface channel device and reset FET 124 is a buried channel device, thereby simplifying the power supply requirements of the circuit. A buried channel FET 126 is connected between the drain of the FET 122 and earth in a constant current configuration for converting the sensed charge on diode 32 to an output voltage at node A.

The sample and hold circuit 111 includes a clamping portion comprising a series capacitor 127, a clamping FET 128, and a buffer amplifier 129; and a sample and hold portion comprising a sampling FET 130, a storage capacitor 131, and an amplifier 132. Samples of the signal voltage at node A are taken by applying a clamping pulse ϕ_{CL} to the gate of FET 128 while the voltage at node A is at the reset level, then applying a sampling pulse $\phi_{S/H}$ to the gate of FET 130 when the voltage at node A is at the final signal level, thereby removing any variations from the signal caused by reset noise. The final signal voltage is stored on capacitor 131 and reproduced at node B by amplifier 132 until the next sample is taken.

Peak detection of the voltages at node B is accomplished by a comparator 134, a reference capacitor 136, a sampling FET switch 138, and a timing FET switch 140. The peak detector circuit 113 includes a threshold setting portion comprising

a preset FET switch 142 connecting capacitor 136 to earth, and a threshold setting FET switch 144 connecting the capacitor 136 to controlled voltage source V_{cc} through a resistor 146.

5 The operation of the rangefinder will now be described with reference to FIGS. 9, 10 and 11. FIG. 9 is a flow chart showing a control program for the microprocessor 106 (see FIG. 7). The program starts, for example, upon closure of main power
10 switch 112 at time t_0 by initializing the image sensor. The image sensor is initialized by supplying control signals ΦB_1 and ΦB_2 to simultaneously close all four FET switches 16, 18, 20, and 22 while the bias voltage V_B is held at
15 the earth potential (see FIGS. 10 d, e, f), thereby earthing the anodes and cathodes of both the photodiode 12 and the storage diode 14. Next, the microprocessor 106 sends a reset signal R to counter 116 to initialize the counter 116. Then, at
20 time t_1 , the microprocessor 106 turns on the LED 117, sets the bias voltage $\pm V_B$ on the sensor element positive (+), and opens FET switches 16 and 20 by commanding ΦB_2 low, thereby connecting the photodiodes 12 to supply charge to the respective
25 storage diodes 14. This condition is maintained for a time period τ_1 while charge generated by both ambient scene illumination and the light in the small illuminated area of the object supplied by LED 117, is accumulated in the storage diodes 14. At time
30 t_2 , the LED 117 is turned off, the polarity of the bias voltage $\pm V_B$ is reversed, FET switches 18 and 22 are opened, and switches 16 and 20 are closed (see FIG. 10c-f). The photodiodes 12 are now connected to remove charge due to ambient scene
35 illumination from the storage diodes 14. This condition is maintained for a time period τ_1 to

remove exactly the same amount of background charge as was added in the previous step. The charge remaining on the storage diodes 14 after the second integration time period τ_1 is due solely to the light from the LED 117. Alternatively, the steps of accumulating charge with the LED on and removing charge with the LED off may be repeated several times to increase the final signal level without significantly increasing the noise, thereby improving the signal-to-noise ratio of the device.

At time t_1 , prior to the expiration of the second time period τ_1 (or the final time period τ_1 if several repeats are employed), the signal processing circuitry is initialized to set the threshold of the peak detector circuit. FET switch 142 (see FIG. 8) is turned on momentarily by generating a ϕ_{preset} pulse (FIG. 10g) thereby earthing capacitor 136. Then FET switch 144 is turned on by a pulse ϕ_{TH} for a time period τ_2 (FIG. 10h) to charge capacitor 136 to a value determined by the time constant of resistor 146 and capacitor 136. At time t_4 the charges remaining in storage diodes 14 are transferred to the CCD shift register by applying a pulse T_1 to the transfer gate 24 while the voltage on the phase-2 electrode ϕ_2 is held high (see FIG. 10a and b). The CCD shift register is then read out to generate the range signal by applying the four-phase clock signals ϕ_1 -.4 to the transfer electrodes 44, 46, 48, and 50 (see FIG. 10b).

Processing of the signals from the CCD will now be described with reference to FIG. 11. The four-phase clock signals ϕ_1 -.4 are shown in FIGS. 11a-d. While the signal charge resides under the phase-3 electrode 50 and the phase-4 electrode 46 (ϕ_3 and ϕ_4 simultaneously high) a reset

pulse ϕ_R is applied to FET 124 in output preamplifier 34 to prepare the output diode 32 to receive signal charge. At this point, the voltage at output node A goes to a high level (200 in FIG. 11f). When the voltage applied to the phase-3 electrode 50 is removed (ϕ_3 goes low), some of the charge may spill over the output gate 120, which is held at a fixed potential, onto the output diode 32, causing the voltage at node A to go to an intermediate level (202 in FIG. 11f). Finally, when the voltage on the phase-4 electrode 46 (ϕ_4) goes low, the remainder of the signal charge is moved to the output diode 32, causing the voltage at node A to reach its final value (204 in FIG. 11f).

While the signal is at its reset level 200, a clamping pulse ϕ_{CL} (see FIG. 11g) is applied to clamping FET 128, then when the final signal value is present at node A, a sampling pulse $\phi_{S/H}$ is applied to sampling FET 130 (see FIG. 11h) thereby storing the final voltage on storage capacitor 131. The voltage on capacitor 131 is followed by amplifier 132 and produced at node B of the circuit (see FIG. 11i).

The voltage at node B is a step-wise smooth curve representing the successive values of the signals from successive photosensitive elements of the image sensor. Comparator 134 compares the first sample with threshold voltage V_{TH} (see FIG. 11i) stored in capacitor 136. If the sampled value is less than the threshold value, the output of comparator 134 at node C remains low. If, on the other hand, the sampled value exceeds the threshold value, the comparator produces a high output at node C. At a point during the presence of the sampled value, a sample signal ϕ_S (see FIG. 11j) is applied to FET transistor or switch 140. If the

voltage at node C is low at this time, the low value will be applied to the gate of FET transistor of switch 138, which will have no effect on the state of the circuit. If however, the voltage at node C
5 is high, the high voltage will be applied to the gate of the transistor of switch 138, thereby applying the new higher reference value to capacitor 136. The new reference value is equal to the input at node B, thereby causing the output at node C to
10 go low (see FIG. 11k). This process continues, producing a pulse at node C each time a new greater output value is received from the sensor array.

At the start of the sequence, counter 116 was initialized. Each time a new charge packet is
15 read from CCD shift register 30, counter 116 is advanced (see FIG. 7). The pulse train produced by the peak detector circuit 113 at node C is applied to latch circuit 115 which captures and holds the
output of counter 116 whenever a pulse is received
20 from the peak detector circuit 113. After all the charge packets have been read out of the CCD shift register 30, the count held by latch circuit 115 is indicative of the location of the sensor element receiving the greatest illumination from the LED
25 above the threshold level V_{TH} . At this point, the microprocessor 106 retrieves the range data from the latch circuit 115 by interrogating its input port. The range data are used in a known manner to drive an output device 118 such as a range display or a
30 range servo.



CLAIMS

1. A device for finding the range of an object in a scene, including means for projecting a beam of light to illuminate a small area on the object, a plurality of photosensors for producing signals indicative of the amplitude of light incident on them from respective portions of the scene including portions at different ranges along the path of the beam, means for identifying the photosensor upon which is incident light from said small area on the object, said identifying means including charge storage means for storing charge discretely from each photosensor, switching means for selectively connecting the photosensors to the storage means to add charge to the storage means when the light beam is turned on and to remove charge from the storage means when the light beam is turned off, the greatest stored charge after a complete cycle of charge addition and removal being associated with the photosensor upon which light from the said small area is incident, the range of the object being determinable from knowledge of which photosensor has associated with it said greatest stored charge.

2. A device as claimed in claim 1, wherein each photosensor is a photodiode, the charge storage means includes a plurality of diodes, and the switching means includes FET transistors connecting each photodiode to its respective storage diode in a bridge configuration.

3. A device as claimed in claim 1 or 2, wherein the photosensors are disposed in a linear array.

4. A device as claimed in claim 1, 2 or 3, wherein the charge remaining in each storage diode after a complete cycle constitutes a difference signal, the device further including a charge



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coupled device shift register and transfer-gate
means for transferring the difference signals from
the storage diodes in parallel into the shift
register whereby the difference signals delivered
5 from the shift register may be compared to determine
the range of the object.

5. A device as claimed in claim 1 substantially
as hereinbefore described with reference to Figs. 2 to
11 of the accompanying drawings.

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