ABSTRACT

IMPROVEMENTS IN AND RELATING TO MATRIX DISPLAY

A matrix-type display control device suited to large capacity displays while achieving low power consumption operation is provided by improving the display data transfer method.

The module controller 100 of a simple matrix-type liquid crystal display comprises a low frequency oscillator 110, timing signal generator 120, standby circuit (display data refresh detection circuit) 130, high frequency oscillator 140, and a direct memory access (DMA circuit) 150. This low frequency oscillator 110 constantly generates the low frequency clock f_L. Timing signal generator 120 generates the scanstart signal YD required for the LCD module 200, and other signals based on the low frequency clock f_L. Standby circuit 130 generates the intermittent operation start control signal $\overline{ST}$ when the display data in VRAM 12 is updated as determined by monitoring the system bus 14a for communications with the host MPU 10. The high frequency oscillator 140 generates the high frequency clock f_H phase synchronised to the low frequency clock f_L during the intermittent operation start control signal $\overline{ST}$ apply period. The DMA circuit 150 reads the display data from the VRAM 12 over dedicated bus 14b by direct memory access, and transfers the display data over data bus 17 to the frame memories 252-1 ~ 252-N of X drivers 250-1 ~ 250-N during the applied time of the intermittent operation start control signal $\overline{ST}$ using the high frequency clock f_H.

Figure 1