SYSTEM AND METHOD FOR SURFACE REDUCTION, PASSIVATION, CORROSION PREVENTION AND ACTIVATION OF COPPER SURFACE

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BACKGROUND OF THE INVENTION

1. Field of the Invention

[1] The present invention relates generally to damascene semiconductor manufacturing processes, and more particularly, to methods and systems for planarizing features and layers in a semiconductor manufacturing process.

2. Description of the Related Art

[2] In general, the manufacturing of the integrated circuit devices (in the form of semiconductor substrates and wafers) includes the use of plasma etching chambers. The plasma etch chambers are capable of etching selected layers on the substrate as defined by a mask or pattern. The plasma etch chambers are configured to receive processing gases (i.e., etch chemistries) while a radio frequency (RF) power is applied to one or more electrodes of the plasma etch chamber. The pressure inside the plasma etch chamber is also controlled for the particular process. Upon applying the desired RF power to the electrode(s), the process gases in the chamber are activated such that a plasma is created. The plasma is thus configured to perform the desired etching of the selected layers of the semiconductor wafer.

[3] Low volatility byproducts are produced in some prior art plasma etch processes. By way of example, in a copper etch process using chlorine containing gases (e.g., Cl_2, HCl, etc), the byproduct is CuClx. CuClx is non-volatile at room temperature. The low-volatility byproducts typically condense on the chamber walls. During each plasma etch cycle, the byproducts build-up on the chamber walls. Eventually the byproducts build-up to a certain thickness. The byproduct build-up then begins to "flake" off of the chamber walls and is therefore becomes a significant particle source. The particles can contaminate the substrates being etched in the chamber.

[4] The copper etchant chemistries are often corrosive to the surface of the remaining copper. This corrosive action can cause uneven pitting and leave an undesirable residue layer that must be removed before subsequent processing can occur. Typically, the substrate is removed from the plasma etch chamber and is cleaned and/or rinsed.

[5] Figure 1 shows a typical cleaned substrate 100. The substrate 100 has a relatively thick layer of oxide 102 (e.g., copper oxide) on top of the exposed copper device 104. The oxide layer 102 can interfere with subsequent processing (e.g., forming interconnects to the underlying copper device) and therefore must be removed before subsequent processing can be attempted. The substrate 100 can also have a barrier layer 106.

[6] CMP chemistries can cause problems similar to those described above for the etching chemistries. A substrate is typically cleaned and rinsed after a CMP operation. The CMP process itself and/or cleaning and/or the rinsing operation can also cause an oxide layer to form.

[7] In view of the foregoing, what is needed is a system and method of removing the residue layer while substantially eliminating the formation of the oxide layer or any other undesirable terminating layer.

SUMMARY OF THE INVENTION

[8] Broadly speaking, the present invention fills these needs by providing an improved method of passivating an exposed conductive material. It should be appreciated that the present invention can be implemented in numerous ways, including as a process, an apparatus, a system, computer readable media, or a device. Several inventive embodiments of the present invention are described below.

[9] A method of passivating an exposed conductive material includes placing a substrate in a process chamber and injecting a hydrogen species into the process chamber. A hydrogen species plasma is formed in the process chamber. A surface layer species is reduced from a top surface of the substrate is reduced. The reduced surface layer species are purged from the process chamber. The conductive material can include at least one of a group consisting of a copper containing material, elemental copper, alloys such as NiFe, CoFe, elemental Ni, Co, Ru, AlO, Ta, TaN, Pt and Ir.

[10] The passivation process can be performed in situ. The passivation process can be performed ex situ. The passivation process can be performed in situ in an etch process. The passivation process can be performed in situ in a stress free planarization process. The passivation process can be performed ex situ following a CMP operation.

[11] The process chamber can have a temperature of between about 30 and about 400 degrees C. The process chamber can be a small volume plasma chamber. The process chamber can be a capacitively coupled system, an inductively coupled system, an ECR or a microwave powered system. The process chamber can have a pressure of between about 1 mTorr and about 1000 mTorr.

[12] The surface layer species can be an oxide, a halide (e.g., chloride, bromide, fluoride or iodide containing species) and a nitride or combinations thereof. The hydrogen species can include at least one of a group consisting of H_2, HCl, HBr, CH_4 and NH_3. Injecting the hydrogen species can also include injecting a carrier gas such as argon, nitrogen, helium, neon and xenon.

[13] Forming a plasma with the hydrogen species can include volatilizing a residue on at least one of the substrate and an inner wall of the process chamber. Purging the reduced surface layer species from the process chamber can also include purging the volatilized residue.

[14] Reducing the surface layer species from the top surface of the substrate can also include activating the top surface of the substrate and roughening the top surface of the substrate. The exposed conductive material is passivated with a predetermined time. The predetermined time being sufficient to reduce the surface layer species from the top surface of the substrate a desired amount. The predetermined time can be greater than about 15 seconds.

[15] Another embodiment provides a method of passivating an exposed copper interconnect. The method includes placing a substrate in a process chamber and injecting a hydrogen species into the process chamber. The method also includes forming a hydrogen species plasma in the process chamber and reducing a copper oxide from a top surface of the exposed copper interconnect. The reduced copper oxides are purged from the process chamber. Each of several inner surfaces of the process chamber can have a temperature

equal to or greater than about 250 degrees C. Each of the inner surfaces of the process chamber is exposed to the substrate.

[16] Another embodiment provides a method of performing a non-contact planarization on a substrate. The method includes placing a substrate in an etch process chamber and etching the substrate. The method also includes injecting a hydrogen species into the etch process chamber and forming a hydrogen species plasma in the etch process chamber. A surface layer species is reduced from a top surface of the substrate and the reduced surface layer species are purged from the process chamber.

[17] Other aspects and advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[18] The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings, and like reference numerals designate like structural elements.

[19] Figure 1 shows a typical cleaned substrate.

[20] Figure 2A shows a copper matrix, in accordance with one embodiment of the present invention.

[21] Figure 2B shows a passivated copper matrix, in accordance with one embodiment of the present invention.

[22] Figure 3A is a flowchart of the method operations of a CMP process, in accordance with one embodiment of the present invention.

[23] Figure 3B is a flowchart of the method operations of an etch process, in accordance with one embodiment of the present invention.

[24] Figure 4 is a flowchart of the method operations of a passivation process, in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[25] Several exemplary embodiments for passivating and reducing the surface of an etched surface will now be described. It will be apparent to those skilled in the art that the present invention may be practiced without some or all of the specific details set forth herein.

[26] Exposed copper can be vulnerable to corrosion. This is especially true of processed copper when interconnect applications are exposed to various process chemistries (e.g., wet and dry chemistries). Some of these conditions can also employ corrosive chemistries. By way of example, a copper dry etch is typically slow and non-selective due to non-volatility at lower temperatures. Volatile compound formation is feasible in halogen containing chemistries (e.g., chlorine, fluorine, bromine, and iodine chemistries) at high temperatures (i.e., greater than about 200 degrees C). Corrosion is a critical issue due to interaction of residual halogen compounds on the copper surface with moisture or interaction of residual halogen in the process chamber with non-passivated copper surface sites. The latter case may include stress free barrier removal following copper CMP or electropolish. Another example is copper processing for damascene applications that use CMP that employs corrosive alkaline slurries. Corrosion persists in spite of typical wet treatments. Further, the typical wet treatments can introduce additional process modules, additional chemical requirements and thereby increase production costs and production time.

[27] Stable, activated surfaces are important in dual damascene processes for electrical as well as next layer deposition requirements. Typically, the newly exposed copper surface has surface characteristics that are different than that required for further processing. Additional process steps and process modules are required to modify the newly exposed copper surface to meet these needs. Modifications to the newly exposed copper surface include the reduction of the surface copper oxide layer to elemental copper and activation of the copper surface inside vacuum (e.g., less than about 100 mTorr) conditions. Other modifications can include removal of CMP residues that contain many components of the CMP process chemistries (e.g., brighteners, inhibitors, accelerators, etc.), therefore avoiding any wet cleaning processes following the CMP process.

[28] One embodiment provides a system and method for passivating the newly etched surface so as to prevent corrosion. The disclosed system and method can remove the etchant

chemistry residue from the etched substrate. The disclosed system and method can also remove the etchant chemistry residue from the walls of the etching chamber. Further, the disclosed system and method can also substantially eliminate the oxide layer formed after a copper layer is exposed and further formed in a wet cleaning process.

[29] The disclosed system and method can be performed in-situ within a plasma etch chamber. In this embodiment, the in-situ passivation operation can be combined with and in some instances incorporated into other processes that are executed within the plasma etch chamber. In this manner the total processes time within the plasma etch chamber is not significantly changed. By way of example, in one embodiment, the passivation operation requires about 30 seconds concurrently with a chuck declamping operation that requires about 60 seconds, thereby resulting no increase in process time within the plasma chamber.

[30] An alternative embodiment includes an ex-situ process such as following a post CMP cleaning and rinsing operation. By way of example, the substrate undergoes a CMP operation and then a cleaning and rinsing operation. The substrate can then be placed in a plasma chamber where the passivation process can be performed so as to reduce the oxide layer formed during the cleaning and rinsing operation(s). This embodiment is especially useful if the operation to follow is a plasma etch or deposition operation that can occur within the plasma chamber.

[31] An additional benefit of the present invention is that the newly exposed layer is activated. The activated layer exposes the matrix of the conductive material so that subsequent connections can be made to the conductive material. Figure 2A shows a copper matrix 200, in accordance with one embodiment of the present invention. The matrix of the copper molecules 202 is covered by an oxide layer 204. The oxide layer 204 can be several hundreds to several thousands of angstroms in thickness. Figure 2B shows a passivated copper matrix 200', in accordance with one embodiment of the present invention. After the passivation operation, oxide layer 204 is substantially reduced such that the matrix of the copper molecules 202 is fully exposed. The matrix of the copper molecules 202 has a slightly rougher surface. The rougher surface can increase adhesion to a subsequent layer that may be formed on top of the exposed matrix of the copper molecules 202.

[32] The passivation operation includes exposing the newly exposed copper surface to a hydrogen chemistry to reduce the surface oxide, passivate the surface and prevent corrosion in a single operation. A hydrogen gas or other gases generating hydrogen under plasma conditions (e.g., HCl, CH4, NH3, etc.) can be used to obtain the desired result. This plasma process can be used in various types of plasma reactors including inductively or capacitively coupled plasma or microwave reactors. Additional additive gases can include, for example by not limited to argon, oxygen and nitrogen.

[33] Figure 3A is a flowchart of the method operations 300 of a CMP process, in accordance with one embodiment of the present invention. In an operation 305, a bulk removal or planarization or other CMP operation is performed on a substrate. By way of example, the CMP operation can be used to remove an overburden portion of a conductive material such as for a damascene or a dual damascene interconnect structure. The CMP operation exposes the conductive interconnects. The CMP operation can be any type of CMP operation such as a linear belt or rotary or planar table or a low down force CMP operation.

[34] In an operation 310, the substrate is cleaned in a "wet" operation such as a deionized water rinse or similar clean operation. The wet clean operation removes the residual CMP slurry and CMP byproducts from the substrate. The wet clean operation can often be incorporated within the CMP process tool or in a separate process tool or module.

[35] In an operation 315, the cleaned substrate is placed in a process chamber. The process chamber can be any process chamber suitable for plasma operations. In one embodiment, the processing chamber includes a processing chamber capable of having all inner surfaces substantially uniformly heated above a temperature necessary volatilize any residues that may be clinging to the inner surfaces of the process chamber (e.g., about 200 to about 400 degrees C). The inner surfaces include those internal surfaces of the processing chamber that the substrate is exposed to. In one embodiment, the process chamber is a small volume process chamber such as described in co-owned and co-pending U.S. Patent application 10/744,355, filed on December 22, 2003, and entitled "Small Volume Process Chamber with Hot Inner Surfaces". A small volume process chamber have a top electrode and the bottom electrode that are separated by a distance of between about 0.5 cm to about 5 cm.

[36] In an operation 340, the surface of the exposed conductive interconnect structures are passivated. The surface passivation is described in more detail in Figure 4 below. As described in Figure 3A, the surface passivation operation 340 is an ex-situ operation from the CMP operation 305.

[37] Figure 3B is a flowchart of the method operations 320 of an etch process, in accordance with one embodiment of the present invention. In an operation 325, a substrate is placed in a processing chamber suitable for plasma operations. The substrate can be placed within the processing chamber for other operations. By way of example, the other operations can include operations such as a plasma etching process or a deposition process (e.g., chemical vapor deposition).

[38] In an operation 330, a process (e.g., a plasma etch process) is applied to the substrate in the processing chamber. The process can be any capable of being performed in the processing chamber. In one embodiment the process is a stress free plasma etch process such as described in U.S. Patent Application No. 10/390,117 filed on March 14, 2003 and entitled "System, Method and Apparatus For Improved Global Dual-Damascene Planarization" and U.S. Patent Application No. 10/390,520 filed on March 14, 2003 and entitled "System, Method and Apparatus For Improved Local Dual-Damascene Planarization." The plasma etch process exposes a conductive interconnect or device structures.

[39] In an operation 340, the surface of the exposed conductive interconnect structures are passivated. The surface passivation is described in more detail in Figure 4 below. As described in Figure 3B, the surface passivation operation 340 is an in-situ operation capable of being performed within the same process chamber as another previous or subsequent operation.

[40] Figure 4 is a flowchart of the method operations 340 of a passivation process, in accordance with one embodiment of the present invention. In an operation 405, a hydrogen containing species is injected into the plasma chamber. The plasma chamber is heated to a range of about 75 degrees C and about 300 degrees C. The pressure of the plasma chamber is within a range of about 1 mTorr and about 100 mTorr. In one embodiment, hydrogen is injected at a flow rate of between about 20 sccm (standard cubic centimeters per minute) and

about 200 sccm. The hydrogen can be carried on an inert carrier gas (e.g., argon) at a flow rate of about 20 to about 2000 sccm.

[41] In an operation 410, a plasma is formed with the hydrogen species. The high energy of the plasma and the relatively high temperature (e.g., about 75 to about 300 degrees C or more) can cause the majority of the residue materials (e.g., CMP residues or etchant residues) on the substrate to become volatile. Desirable temperature range for the substrate is about 200 to about 400 degrees C. Similarly the etchant residues on the inner surfaces of the processing chamber also become volatile. Desirable temperature range for the process chamber is about 200 to about 400 degrees C. The volatilized residue materials can be purged in an operation 420 below. The plasma can be formed in any type of plasma chamber (e.g., inductive, capacitive, etc.). By way of example, in an exemplary inductive plasma chamber, a power applied to top is between about 500 to about 3000 watts of power. The bottom electrode can have a power applied of between about 0 to about 100 watts of power. Similarly in a capacitive plasma chamber, system power in the range of about 500 to about 5000W can be applied to the bottom and/or top electrode(s). The RF power supply can be affected with either a single or dual frequency.

[42] In an operation 415, the oxide layer is reduced. By way of example, the hydrogen plasma causes the oxygen atoms in the oxide surface layer to disassociate with the conductive material (e.g., copper) and to combine with the hydrogen to form water molecules. Any remaining hydrogen atoms, any oxygen atoms disassociated from the conductive material and the formed water molecules can be purged in an operation 420 below. The oxide layer reduction and the volatilized residue materials are completed in about 15 seconds to about 2 minutes. While no maximum time is indicated, the majority of the oxide layer and volatilizing the residue materials can be accomplished in less than about 2 minutes. In an operation 420, the oxides, hydrogen, water vapor and volatilized residue materials are purged from the processing chamber and the method operations end.

[43] By way of example in one embodiment, a substrate is loaded in a capacitively coupled plasma etch chamber. The plasma etch chamber is heated to a temperature of about 250 degrees C, at a pressure of about 20 mTorr. The top electrode of the plasma etch chamber has about 1000 watts applied and zero power is applied to the bottom electrode. About 100 sccm of H_2 and about 100 sccm of argon is injected into the plasma etch chamber

to generate a hydrogen species plasma. The substrate is exposed to the hydrogen plasma for about 60 seconds to reduce the oxides in the top surface of the substrate.

[44] While the above-described embodiments are described in terms of copper device and interconnect structures, the embodiments are not limited to only copper. Etching magnetic materials (NiFe, CoFe, AlO, etc.) and electrode materials (Ta, TaN, Pt, Ir, etc.) can also be performed by similar processes.

[45] It will be further appreciated that the instructions represented by the operations in any of the above figures are not required to be performed in the order illustrated, and that all the processing represented by the operations may not be necessary to practice the invention. Further, the processes described in any of the above figures can also be implemented in software stored in any one of or combinations of the RAM, the ROM, or the hard disk drive.

[46] Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

What is claimed is:

Claims

1. A method of passivating an exposed conductive material comprising:
placing a substrate in a process chamber;
injecting a hydrogen species into the process chamber;
forming a hydrogen species plasma in the process chamber;
reducing a surface layer species from a top surface of the substrate; and
purging the reduced surface layer species from the process chamber.

2. The method of claim 1, wherein the conductive material includes at least one of a group consisting of a copper containing material, elemental copper, NiFe, CoFe, elemental Ni, Co, Ru, AlO, Ta, TaN, Pt and Ir.

3. The method of claim 1, wherein the passivation process is performed in situ.

4. The method of claim 1, wherein the passivation process is performed ex situ.

5. The method of claim 1, wherein the passivation process is performed in situ in an etch process.

6. The method of claim 5, wherein the passivation process is performed in situ in a stress free planarization process.

7. The method of claim 1, wherein the passivation process is performed ex situ following a CMP operation.

8. The method of claim 1, wherein the process chamber has a temperature of between about 30 and about 400 degrees C.

9. The method of claim 1, wherein the process chamber is a small volume plasma chamber.

10. The method of claim 1, wherein the process chamber includes at least one of an inductively coupled system, an ECR and a microwave powered system.

11. The method of claim 1, wherein the process chamber has a pressure of between about 1 mTorr and about 500 mTorr.

12. The method of claim 1, wherein the process chamber is a capacitively coupled system.

13. The method of claim 1, wherein the hydrogen species includes at least one of a group consisting of H_2, HCl, HBr, CH_4 and NH_3.

14. The method of claim 1, wherein injecting the hydrogen species includes injecting a carrier gas.

15. The method of claim 14, wherein the carrier gas includes at least one of a group consisting of argon, nitrogen, helium, neon and xenon.

16. The method of claim 1, wherein the surface layer species includes at least one of an oxide, a halide and a nitride.

17. The method of claim 1, wherein forming a plasma with the hydrogen species includes volatilizing a residue on at least one of the substrate and an inner wall of the process chamber and wherein purging the reduced surface layer species from the process chamber includes purging the volatilized residue.

18. The method of claim 1, wherein reducing the surface layer species from the top surface of the substrate includes:

activating the top surface of the substrate; and

roughening the top surface.

19. The method of claim 1, wherein the exposed conductive material is passivated with a predetermined time, the predetermined time being sufficient to reduce the surface layer species from the top surface of the substrate a desired amount.

20. The method of claim 1, wherein the predetermined time is greater than about 15 seconds.

21. A method of passivating an exposed copper interconnect comprising:
placing a substrate in a process chamber;
injecting a hydrogen species into the process chamber;
forming a hydrogen species plasma in the process chamber;
reducing a copper oxide from a top surface of the exposed copper interconnect; and
purging the reduced copper oxide from the process chamber.

22. The method of claim 21, wherein each of a plurality of inner surfaces of the process chamber has a temperature equal to or greater than about 250 degrees C, wherein each of the plurality of inner surfaces of the process chamber is exposed to the substrate.

23. A method of performing a non-contact planarization on a substrate comprising:
placing a substrate in an etch process chamber;
etching the substrate;
injecting a hydrogen species into the etch process chamber;
forming a hydrogen species plasma in the etch process chamber;
reducing a surface layer species from a top surface of the substrate; and
purging the reduced surface layer species from the process chamber.