

The invention relates to a circuit arrangement for the electronic level adjustment of signals in discrete steps with the aid of a digitally driveable C-MOS-switch.

Because of their space-saving and also cheap design, such switches are being used to an increasing extent in audio equipment. In high-quality audio equipment, such as for example CD players or digital audio tape devices, or also tape decks with integrated high-quality noise reduction systems, signal-to-noise ratios exceeding 90 db are reached. Extremely low, non-linear distortion factors are attained in particular in the case of digital sound recording. However, there is little point in providing such optimal data levels for hifi devices if weak points cancel out these data again. Such weak points reside in electronic volume controllers of known type and also C-MOS switches which for example in case of the stepped adjustment of the volume of an audio signal give rise to clicks which are particularly disturbing in the lower frequency range of an audio signal. Up until now it has not been possible to obtain a switch which gives rise to no clicks when it also fulfils the requirements regarding non-linear distortion factor and signal-to-noise ratio.

An arrangement for the suppression of clicks in the adjustment of the volume of LF amplifiers is known wherein switch-over noises are eliminated in that a longitudinal regulator arranged in the signal path develops a high resistance with the result that a time delay of the corresponding switching processes is introduced and therefore the effect diminishes after a given length of time. Thus a gradual change in the level occurs. Additionally, a transverse regulator is provided which is opposed in its effect to the longitudinal regulator. Here no compensation takes place, but the resultant overall change in the variable which is to be influenced takes place in the same direction, i.e. the influence of the transverse regulator is double-inverted, firstly by the fact that this is a transverse regulator and secondly by the oppositely

directed driving. Thus if for example in the case of upwards adjustment, the longitudinal regulator develops low resistance and the transverse regulator develops high resistance, and thus the signal increases with the time constant of the RC elements, simultaneous compensation does not take place (DE-A-30 08 033).

In an article entitled "Stepped Volume Control", the magazine "Elektor Electronics", Vol, 14, No. 158 July/August 1988, page 58, London, GB, describes a circuit arrangement which uses a MOS switch corresponding to that referred to in the preamble of the Claim. However, this article does not refer to the suppression of interference noises.

The aim of the invention is to supplement a switch subject to clicks, in such manner that it can also be used for hifi devices without producing disturbances. This aim is fulfilled by the measures described in Claim 1. Further advantageous developments of the invention are described in the sub-claims.

In the following the invention will be explained in the form of an exemplary embodiment and in terms of its mode of operation making reference to the drawing.

In the drawing:

Figure 1 is a block circuit diagram of the invention;

Figure 2 represents diagrams of the mode of operation of the invention;

Figure 3 illustrates a detailed circuitry example of the invention.

In Figure 1, S designates an electronic switch (C-MOS technology), at the input E of which an audio signal AS occurs, which can be tapped from the output A in changeable fashion by means of this switch, e.g. in 1-db-steps. The stepped changing of the signal AS is effected by an incremental transmitter IG which in the event of adjustment emits pulses I which, in accordance with the direction of operation, generate signals in the BCD code, with which the switch S is driven. At the output A voltage jumps of the

signal AS occur in db-steps. As already mentioned in the foregoing, these jumps are unpleasantly audible in particular in the lower frequency range of the signal AS. Therefore the switch S is connected to an arrangement R which influences the output signal AS in opposition to its change and this to an extent corresponding to the step produced by the switch S. If, as assumed, the switch S changes the input signal by 1 db, the arrangement R likewise influences the output signal of the switch S by 1 db, but in opposing fashion. When the signal is increased, with each step of the switch S of +1 db, the arrangement is switched to -1 db at the start of the step. The arrangement R influences the signal from this setting in a continuously decreasing fashion after a predeterminable time constant to 0db, so that from this time onwards the entire step set by the switch S can take effect. This process is illustrated in Figure 2. Figure 2a illustrates an audio signal AS which at the time t_0 is set at a value increased by 1 db. This signal jump produces the unpleasant clicking in the playback device. Figure 2b shows the stepped signal jumps of the output signal of the switch S. Figure 2c shows how initially the arrangement R is set at -1 db which compensates the voltage jump. The arrangement R is automatically adjusted in continuously reducing fashion to the value 0 db so that after the time constant T, at the time t_1 the full step can take effect. At the time t_2 a new step is produced. At the same time the arrangement R is adjusted to -1 db etc. Figure 2d shows the curve of the signal at the output 0 of the arrangement R. Figures 2e, f and g illustrate the mode of operation of the arrangement in the opposite direction, without making reference to the signal diagram in Figure 2a.

The invention will be described in the example of a technical embodiment making reference to Figure 3. Here S again designates the C-MOS switch for the digital level adjustment of the signal AS which is fed to said switch via

an input amplifier V and a coupling capacitor C1. The C-MOS switch S is wired in a manner known per se to resistors RS which can be switched on or off in accordance with an item of information supplied to the BCD input by the incremental transmitter IG, so that the output signal can be tapped from the output A of the C-MOS switch S in discrete steps of for example 1 db. This signal is fed to the non-inverting input of an operational amplifier OP which is provided in the arrangement R and the output O of which is fed back via the negative feedback resistor RG. The inverting input of the operational amplifier OP is connected to two parallel-connected arms which cause the respective increase or reduction in the signal in the case of the stepped change in level by the C-MOS switch. One arm comprises the resistor R1, which is connected to the reference potential via the drain-source path of an electronic switch F1 and whose gate electrode on the one hand is connected to reference potential via a timer R2, C2 and on the other hand can be connected to a positive potential via a switching stage T1. The other arm comprises the resistor R4 which is connected to reference potential via the drain-source path of a further electronic switch F2 and whose gate electrode is connected on the one hand to a positive potential via a resistor R3 and on the other hand to reference potential via a capacitor C3. The resistor R3 and the capacitor C3 form a further timer. A switching stage T2 is arranged in parallel to the capacitor C3. The wiring is such that when the gate is positive the respective switch F1 or F2 is driven conductive. With a different type of wiring, the potentials would of course need to be opposed. The switching stages T1 and T2 are in each case temporarily closed at the start of a change in level at the output A of the C-MOS switch S. This process can be carried out via a microprocessor uP by software in that either the switching stage T1 for example in the case of a reduction in level, or T2 for example in the case of an increase in

level, is temporarily actuated by a pulse I1 or I2 respectively. Here the switching stages T1 and T2 have been represented only symbolically as transistor switches. Other possibilities of closing the switches F1 and F2 are also conceivable.

When the arrangement R is in the rest state, the switch F1 has a high resistance and the switch F2 has a low resistance so that the operational amplifier OP possesses a determinate amplification of for example +1 db defined by the resistors R_G and R₄, corresponding to one step width of the switch S. In the case of a stepped increase in the level at the output A, the switching stage T2 is temporarily closed so that the capacitor C3 of the timer R3/C3 is discharged. The switch F2 develops a high resistance and the amplification of the operational amplifier OP is thus reduced. The reduction is set by the resistor R_G to be such that it corresponds to the amount of the step of the level increase, and thus compensates the latter from +1 db to 0 db. At the end of the time constant predetermined by the timer R3/C3, the switch F2 has a low resistance again so that the amplification of the operational amplifier OP again amounts to + 1db.

In the case of a stepped reduction in the level at the output A, the switching stage T1 is temporarily closed so that the capacitor C2 is charged and the switch F1 has a low resistance. As a result the resistor R1 is connected in parallel to the resistor R₄ and the overall resistance is reduced in relation to the reference potential. The divider ratio of R_G to R1 in parallel to R₄ is set such that the amplification of the operational amplifier OP is increased by 1 db to +2 db. The capacitor C2 is discharged via the resistor R2 so that after the time constant R2C2 the switch F1 has a high resistance again and thus the operational amplifier OP again reaches the amplification level of +1 db predetermined by the resistors R_G, R₄.

It should be expressly pointed out that the arrangement R can also be constructed differently than described making reference to Figure 3. It is only essential that the arrangement should initially compensate the step caused by the switch S and that the compensation should be discontinued again in a constantly reducing fashion. The invention has been explained in the example with steps of in each case one db. It will be clear that the invention can also be employed when the steps possess a different size. The arrangement R should be dimensioned accordingly in order that these steps can also be compensated.

Claims

1. A circuit arrangement for the electronic level adjustment of signals (AS) in discrete steps with the aid of a digitally driveable C-MOS switch (S), characterised in that the output of the C-MOS switch (S) is connected to an arrangement (R) which generates a compensating variable which initially compensates the discrete steps produced by the C-MOS switch (S), and that the compensating variable is continuously reduced to cause the discrete steps to take full effect after a predeterminable time constant.
2. A circuit arrangement as claimed in Claim 1, characterised in that the arrangement (R) consists of an operational amplifier (OP), the non-inverting input of which is supplied with the signal from the switching stage (S) and the output (O) of which is connected via a first resistor (RG) to the inverting input, and that the inverting input is connected to earth potential via a second resistor (R4) with a first electronic switch (F2) arranged in series therewith, where the first electronic switch (F2) is conductively biased in the rest state and the second resistor (R4) and the first resistor (RG) are dimensioned such that the operational amplifier (OP) possesses the amplification of one switch step.
3. A circuit arrangement as claimed in Claim 2, characterised in that the bias voltage (+) is connected via a third resistor (R3) to the control electrode of the first electronic switch (F2), which control electrode is connected to reference potential via a first capacitor (C3), and that the first capacitor (C3) can be bridged by means of a second switch (T2).
4. A circuit arrangement as claimed in Claim 2, characterised in that in parallel to the second resistor (R4) a fourth resistor (R1) in series with a third electronic switch (F1) is connected to earth potential, where the third electronic switch (F1) has high resistance



in the rest state, and that the control electrode of the third electronic switch (F1) is connected to earth potential via the parallel arrangement of a second capacitor (C2) with a fifth resistor (R2), and that the control electrode of the third electronic switch (F1) can be temporarily connected by means of a fourth switch (T1) to a bias voltage (+) which switches the third electronic switch (F1) conductive.

5. A circuit arrangement as claimed in Claim 1, 2, 3 or 4, characterised in that the time constant of the timing elements (R2, C2; R3, C3) is selected such that it is smaller than the interval of time between two consecutive pulses of an incremental transmitter (IG) which drives the switching stage (S).

