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(54) **Title**: METHOD AND APPARATUS FOR MEMORY POWER AND/OR AREA REDUCTION

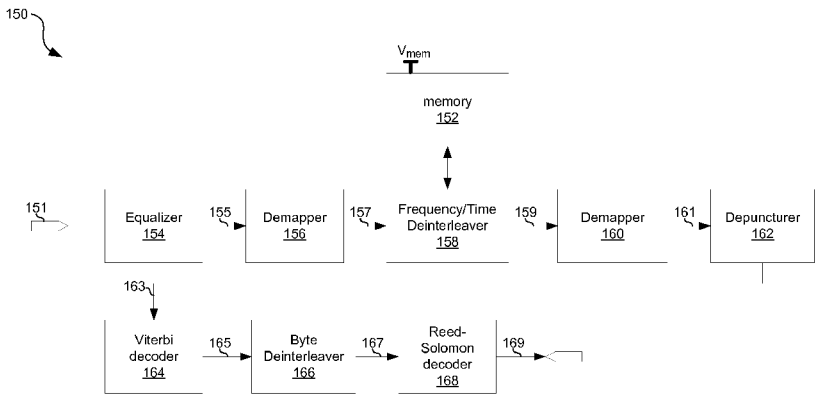

FIG. 1B

(57) **Abstract**: A method and apparatus for memory power and/or area reduction. An array of memory cells may be scanned to detect faulty memory cells, if any, in the array. A supply voltage V_{mem} applied to the array of memory cells may be controlled based on a result of the scan, and based on a sensitivity coefficient of one, or more, of the array of memory cells. The sensitivity coefficient may indicate an impact that the one, or more, of the array of memory cells being faulty may have on the performance of a device that reads and writes data to the memory array. Additionally or alternatively, the physical dimensions of the memory cells may be determined based on the sensitivity coefficient(s) and/or based on a number of faulty memory cells that can be tolerated in the array of memory cells.

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