WHAT IS CLAIMED IS:

1. A storage device set comprising:

a reconfigurable logic chip; and

a storage device configured to communicate with a host via a first port, and to communicate with the reconfigurable logic chip via a second port, such that the reconfigurable logic chip is indirectly connected to the host via the storage device, ~~including a controller configured to generate encrypted input data by encrypting data; and~~

wherein the~~a~~ reconfigurable logic chip is configured to,

receive ~~the~~ encrypted input data from the storage device,

generate processed data by decrypting the encrypted input data to produce decrypted input data, processing the decrypted~~encrypted~~ input data according to a configuration to generate the processed data, and

generate encrypted output data by encrypting the processed data; and

the storage device includes,

a buffer memory configured to store data provided from the host via the first port, and to store the encrypted output data provided by the reconfigurable logic chip; and

a controller configured to,

read the data from the buffer memory,

generate the encrypted input data by encrypting the data,

transmit, via the second port, the encrypted input data to the reconfigurable logic chip,

receive, via the second port, the encrypted output data from the reconfigurable logic chip, and

transmit, via the first port, decrypted output data to the host, the decrypted output data being generated by decrypting the encrypted output data stored in the buffer memory.

2. The storage device set of claim 1, ~~wherein the storage device further includes a buffer memory, and~~ wherein the controller is further configured to,

~~receive the encrypted output data from the reconfigurable logic chip, and~~

buffer, in the buffer memory, the encrypted input data or the encrypted output data.

3. The storage device set of claim 2, wherein the controller is further configured to,

receive the data and a host command from the host,

generate the encrypted input data by encrypting the data, and

load the encrypted input data into the buffer memory.

4. The storage device set of claim 2, wherein the storage device further includes a non-volatile memory configured to store the data, and the controller is further configured to,

read the data from the non-volatile memory, in response to a host command received from the host,

generate the encrypted input data by encrypting the data read from the non-volatile memory, and

load the encrypted input data into the buffer memory.

5. The storage device set of claim 3 or claim 4, wherein, the controller is further configured to transmit a command to the reconfigurable logic chip, in response to completion of loading the encrypted input data into the buffer memory, the command commanding processing of the encrypted input data.

6. The storage device set of any one of claims 2 to 5, wherein the controller is implemented in a first chip, and the buffer memory is implemented in a second chip.

7. The storage device set of any one of claims 2 to 5, wherein the controller and the buffer memory are implemented in a same chip.

8. The storage device set of any one of claims 2 to 7, wherein the controller is further configured to,

generate the decrypted output data by decrypting the encrypted output data, and

buffer, in the buffer memory, the data or the decrypted output data.

9. The storage device set of any one of claims 1 to 8, wherein~~further comprising~~:

the~~a~~ first port is configured to communicate with the host according to a first interface protocol; and

the~~a~~ second port is configured to communicate with the reconfigurable logic chip according to a second interface protocol.

10. The storage device set of claim 9, wherein the controller is further configured to,

transmit the encrypted output data ~~or decrypted output data~~ to the host via the first port~~, the decrypted output data being generated by decrypting the encrypted output data, and~~

~~exchange the encrypted input data or the encrypted output data with the reconfigurable logic chip via the second port~~.

11. The storage device set of any one of claims 1 to 10, wherein the storage device and the reconfigurable logic chip are mounted in a same board.

12. The storage device set of any one of claims 1 to 10~~11~~, wherein the storage device and the reconfigurable logic chip are embodied as a package-on-package (PoP).

13. The storage device set of any one of claims 1 to 12, wherein the reconfigurable logic chip is a field-programmable gate array (FPGA) chip.

14. A storage system comprising:

a host;

a reconfigurable logic chip; and

a storage device configured to,

communicate with the host via a first port, and

communicate with the reconfigurable logic chip via a second port such that the reconfigurable logic chip is indirectly connected to the host via the storage device, wherein the storage device includes,

a buffer memory configured to store data provided from the host via the first port, and to store encrypted output data provided by the reconfigurable logic chip; and

a controller ~~is~~ configured to,

read the data from the buffer memory,

generate encrypted input data by encrypting the data,

transmit the encrypted input data to the reconfigurable logic chip via the second port, ~~and~~

receive the encrypted output data from the reconfigurable logic chip via the second port, and

transmit decrypted output data to the host via the first port, the decrypted output data being generated by decrypting the encrypted output data stored in the buffer memory.

15. The storage system of claim 14, wherein the reconfigurable logic chip is configured to,

receive the encrypted input data from the storage device,

generate processed data by decrypting the encrypted input data to produce decrypted input data, processing the decrypted~~encrypted~~ input data according to a configuration to generate the processed data,

generate the encrypted output data by encrypting the processed data, and

transmit the encrypted output data to the storage device.

~~16. The storage system of claim 14 or claim 15, wherein the storage device is further configured to generate the encrypted input data by encrypting data and transmit the encrypted input data to the reconfigurable logic chip.~~

16~~17~~. The storage system of ~~any one of~~ claim~~s~~ 14 or~~to~~ claim 15~~16~~, wherein the ~~storage device includes a~~ buffer memory is configured to buffer the encrypted input data or the encrypted output data.

17~~18~~. A method of operating a storage device configured to communicate with a host via a first port, and communicate with a reconfigurable logic chip via a second port, such that the reconfigurable logic chip is indirectly connected to the host via the storage device, the method comprising:

receiving, via thea first port of the storage device, a host command from thea host, the host command including a data processing request;

storing, in a buffer memory, write data provided from the host via the first port;

generating, encrypted write data by encrypting the write data;

transmitting, encrypted write data and a command to thea reconfigurable logic chip via thea second port of the storage device, the command commanding data processing with respect to the encrypted write data; and

receiving, via the second port of the storage device, encrypted processed data from the reconfigurable logic chip,

storing, in the buffer memory, the encrypted processed data provided by the reconfigurable logic chip, and

transmitting, via the first port of the storage device, decrypted output data to the host, the decrypted output data being generated by decrypting the encrypted processed data stored in the buffer memory.

1819. The method of claim 1718, further comprising:

receiving the write data from the host via the first port of the storage device; and

encrypting the write data to generate encrypted write data, and

wherein the transmitting transmits the encrypted write data to the reconfigurable logic chip.

1920. The method of claim 1819, further comprising:

loading the encrypted write data into thea buffer memory, and

wherein the transmitting of the encrypted write data and the command to the reconfigurable logic chip includes,

transmitting the command to the reconfigurable logic chip, in response to completion of the loading; and

transmitting the encrypted write data to the reconfigurable logic chip, in response to a read command received from the reconfigurable logic chip.