



Communications controller for transponder

The invention concerns a method according to the introductory part of claim 1 as well as a communications controller according to the introductory part of claim 6.

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Background of the invention

The background of the invention is the wireless payment of charges for the use of roads (road toll) by vehicles. Systems provided for this purpose have been delivered by the Q-Free ASA company since many years. Nowadays these systems are used under the term
10 "Q-Free-box". In this connection the term "box" is related to the module of this system attached to an individual vehicle, that is to say to a so-called transponder. This transponder receives data from a main station of the transponder system and as an answer on this transmits individual data back to the roadside.

Meanwhile the technological development in this field has turned to transponders which -
15 contrary to transponders formerly used in this field - are being operated not passive, but active and for the operation of which microwave radiation with frequencies in the range of 5,8 GHz is applied. With this known transponder system the radiation received by the transponder is amplitude modulated for the transmission of data, while the microwave radiation transmitted by the transponder for the transmission of data is phase modulated.

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The modulated input signal obtained in the transponder by the reception of the microwave radiation initially is demodulated for obtaining a binary input data sequence (of an input data frame). Then this input data sequence is fed to a digital processor (microcontroller) operated by a processing clock of preset clock frequency for decoding and further
25 processing of the received data as well as for generating of a binary output data sequence (output data frame). During a certain duration from the output data sequence as an answer to the input signal an output signal is formed in the transponder, which as modulated microwave radiation of certain frequency is irradiated over the antenna of the microcontroller. These active transponders are as energy source provided with a battery.

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With the known transponder systems the succeeding transactions (transaction sequences) between the main station of the transponder system and the individual transponder are carried out on the basis of an advanced communications protocol (HDLC - High Level Data Link Control) and usually contain the processing of data sequences and control fields.



Furthermore there is a considerable need for the security of the transactions which are to be carried out. To the most common security algorithms belong DES (Data Encrypting Standard System) and Trippel-DES. However the application of these security algorithms usually means that with this the processing of data by the transponder becomes very time
5 consuming.

To this day the most common solution for a transponder of the transponder system is a solution, with which a serial processor is applied as microcontroller. With this solution there is available flexibility for changes and it is possible to achieve satisfying transaction
10 speed with the use of processors, which operate with a system clock rate with a clock frequency of 10 MHz and higher.

The greatest problem which consists with microcontrollers applied as communications controllers until now is that there from the relatively high clock frequency of the system
15 clock results a relatively high load for the battery of the transponder, and this in view of the average height and the duration of the current (integral over the current pulses over the time withdrawn with the frequency of the system clock) as well as in view of the fact, that the pulse-like occurring current withdrawal represents an exceptional
load for the battery. Even if this current withdrawal does not mean so much for the life time
20 of the components of the transponder, so a current withdrawal of such an extent and in an especially pulse-like occurring way is problematical particularly at relatively low temperatures where the internal resistance of the battery is high.

Finally the microcontroller applied for the transponder until now is a serially operating
25 processor. This means that such a processor is not ideal in view of the processing of data which can be processed parallel, especially not then when on the one hand processing-wise extensible actions (decoding) are necessary in the processor and on the other hand within a shortest possible duration after receipt of the input signal an output signal shall be emitted from the transponder.

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Object

The invention has the object on the one hand to considerably reduce the mentioned load of the battery for extending its life time and for improving its operability and on the other hand

to enable the transponder to emit an output signal onto the received input signal within a relatively short duration. Further objects will appear from the following description of examples.

5 **Invention**

For achieving the aforementioned aim the invention according to the characterizing part of claim 1 and 6 respectively is proposed.

Further advantageous and suitable procedural steps or measures are indicated in claims 2-5
10 and 7-9.

On the basis of the knowledge that with the transponder system in question the structure of the content of the data sequences received and transmitted by the transponder at least at a considerable amount allows a parallel and particularly bit-by-bit occurring processing, the
15 solution for carrying out procedural steps according the invention indicated in claim 1 compared to the nowadays state-of-the-art offers the advantage of a considerable reduced load of the battery of the transponder by pulse-like occurring current withdrawal together with a relatively short duration until irradiation of an answer onto the received input signal.

20 An advantageous feature of the invention according claim 1 is indicated in claim 2. With a parallel processing of data of the decoded input data sequence carried out correspondingly it is possible to realize this processing with a system clock rate with only a fraction of the clock frequency usual until now and nevertheless compared to the previous solution to considerable shorten the duration between the receiving of the input signal up till the the
25 forming of the output signal. For that only the extent of the processing of data of the input data sequence now occurring has to exceed the extent of the reduction of the clock frequency in its impact onto the mentioned duration.

For generating of such a - compared to the state-of-the-art "slower" - processing rate a
30 corresponding oscillator can be applied in the transponder.

Advantageously the procedural step according to claim 3 is applied. This solution is useful in view of the fact, that the symbol clock is that clock within the transponder system, which has the lowest clock frequency, namely a considerably lower clock frequency compared to

the previous system clock. The application of a separate oscillator within the transponder for generation of the system clock for the processor can be done without. This also has a positive effect on the load of the battery.

- 5 By retrieving the symbol clock and the following use of it as system clock an ideal solution for the current withdrawal from the battery is obtained. The symbol clock is that clock with the absolutely lowest clock frequency which can be obtained in the transponder system without introduction of additional buffers or the like. - A microcontroller solution, which is based on a plurality of processor modules, which are being operated with this system clock,
- 10 enables bit-by-bit occurring decoding of the data reaching the transponder. This forms a contrast to a microcontroller solution, with which at first the data sequence (the data frame) has to be stored and thereafter the processing of the data can be started.

Claim 4 indicates a preferred solution for forming of a clock frequency derived from the

15 clock frequency of the symbol clock timing generator or corresponding to this clock frequency.

In view of the aforementioned knowledge of a processibility of the mentioned data in a more or less parallel occurring mode claim 5 indicates a particularly useful procedure.

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The claims 6-9 concern a communications controller or useful design of it as it can be applied with advantage in connection with the method according to the invention.

Examples

- 25 In the following the invention will be described more detailed with the aid of Fig. 1 and 2 of the drawing.

Fig. 1 shows in connection with the invention an essential part of a communications controller of a transponder according to the state-of-the-art and as a block diagram, and

Fig. 2 shows essential parts of a communications controller as it is applied in connection

30 with the invention and as a block diagram.

Fig. 1 shows a communication controller 11 of a transponder not shown in further detail according to the state-of-the-art. The system clock for the communications controller 1 is being delivered by an oscillator 12. Over a line 13 incoming input data are being stored in a receiving memory (buffer) 14. When the complete data sequence (data frame) is being
 5 received and stored, the processor core 15 will start the processing of the input data and prepare an answer of the transponder onto the input data. This happens with a system clock with a clock frequency of about 10 MHz or with a still higher clock frequency. - After the answer is completed it will be laid down in a transmission buffer 16, and as soon as the transmission buffer 16 is filled with data the transmission of data can be started and the
 10 answer can be irradiated over the antenna of the transponder in the form of a phase modulated microwave radiation.

Fig. 2 shows essential parts of a communications controller 17 according to the invention. This communications controller 17 is based on a completely different "architecture"
 15 compared to the known communications controller 1 according to Fig. 1. With the communications controller 17 according to Fig. 2 the system clock is delivered from a symbol clock retrieving circuit 18 which the system clock achieved in this way delivers to all processor modules 19-22 integrated for a parallel occurring processing of data.

20 A data decoder indicated with numeral 23 delivers decoded data to the processor modules 19-22, which after each reception of data over the line indicated with numeral 24 will decode these data, process them and form answers. Immediate after the last bit of the received data sequence (data frame) has been decoded the transmission of answering data over the line indicated with numeral 25 can be started. In this way not only the duration
 25 between the reception of the input signal and the irradiation of the output signal of the transponder is considerably shortened, but - because of the considerably reduced clock frequency of the system clock of the transponder - also the load of the battery of the transponder is reduced in a considerable extent.

CLAIMS

1. Method for processing of encoded information by a battery-powered active transponder, which particularly is provided for the application within a transponder system for the
5 wireless payment of road toll, whereby the transponder over an antenna receives modulated microwave radiation of preset frequency for obtaining an input signal which is demodulated for obtaining a binary input data sequence, which then is fed to a digital processor (microcontroller) operated by a processing clock of preset clock frequency for decoding and generating of a binary output data sequence, from which within a certain duration as an
10 answer to the received input signal an output signal is formed, which is transmitted over the antenna of the transponder, **characterized in** that for reducing the load of the battery of the transponder by the pulse-like occurring current demand of the processor with at the same time a relative short duration between the receiving of the input signal and the irradiating of the output signal data, the decoded input data sequence are processed by the processor
15 parallel and with a relative low clock frequency.
2. Method according to claim 1, **characterized in** that the parallel occurring processing of data of the decoded input data sequence is realized with a much lower clock frequency, preferably only a fraction of that clock frequency, compared to a clock frequency of about
20 10 MHz and higher with a serial occurring processing according to the state-of-the-art.
3. Method according to claim 1 or 2, **characterized in** that the parallel occurring processing of data of the decoded input data sequence is realized with a clock frequency which is derived from the clock of the symbol timing generator by retrieving of a plurality of
25 succeeding timing pulses of the symbol clock from the input data sequence and which preferably corresponds to the clock frequency of the symbol clock.
4. Method according to claim 3, **characterized in** that for forming of a clock frequency either derived from the clock frequency of the symbol clock or corresponding to this clock
30 frequency an electronic PLL-circuit (phase locked loop) is applied.
5. Method according to claim 1, **characterized in** that the parallel occurring processing of data of the decoded input data sequence is realized bit-by-bit.

6. Communications controller (17) for a battery-powered active transponder, which particularly is provided for the application within a transponder system for the wireless payment of road toll, whereby the transponder over an antenna receives modulated microwave radiation of preset frequency for obtaining an input signal which is demodulated
- 5 for obtaining a binary input data sequence, which then is fed to a digital processor (17) (microcontroller) operated by a processing clock of preset clock frequency for decoding and generating of a binary output data sequence, from which within a certain duration as an answer to the received input signal an output signal is formed, which is transmitted over the antenna of the transponder, **characterized by** a plurality of processor modules (19-22) of
- 10 the processor (17), which are integrated to a processing unit realizing the parallel occurring processing of data of the decoded input data sequence and are operated by a timing generator (symbol clock retrieving circuit 18) with a relative low clock frequency of the processing clock rate.
- 15 7. Communications controller (17) according to claim 6, **characterized in** that as timing generator for generating a processing clock rate for the mentioned processor modules (19-22) an electronic circuit is provided for retrieving the clock frequency of the symbol clock from the input signal.
- 20 8. Communications controller (17) according to claim 7, **characterized in** that for generating of a processing clock rate for the mentioned processor modules (19-22) with a clock frequency derived from the clock frequency of the symbol clock, preferably corresponding to the symbol clock, a PLL-circuit (phase locked loop) is applied.
- 25 9. Communications controller (17) according to claim 6, **characterized in** that the processor modules (19-22) are dimensioned for a bit-by-bit processing of data of the decoded input data sequence.