FIG. 1

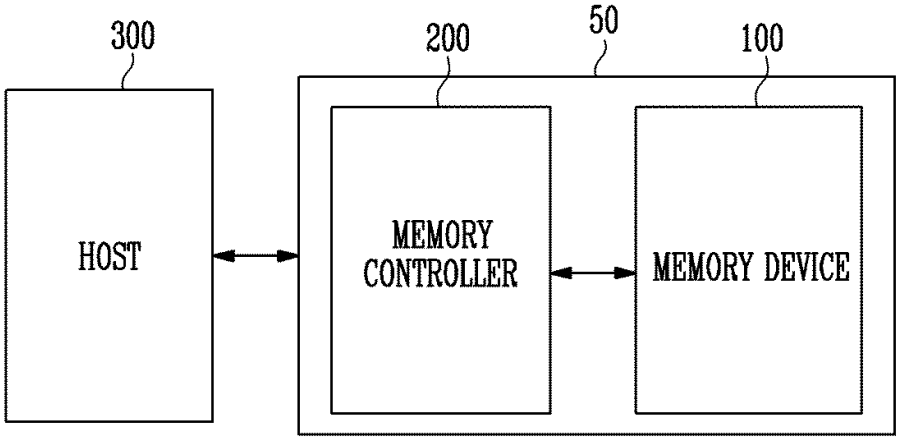


FIG. 2

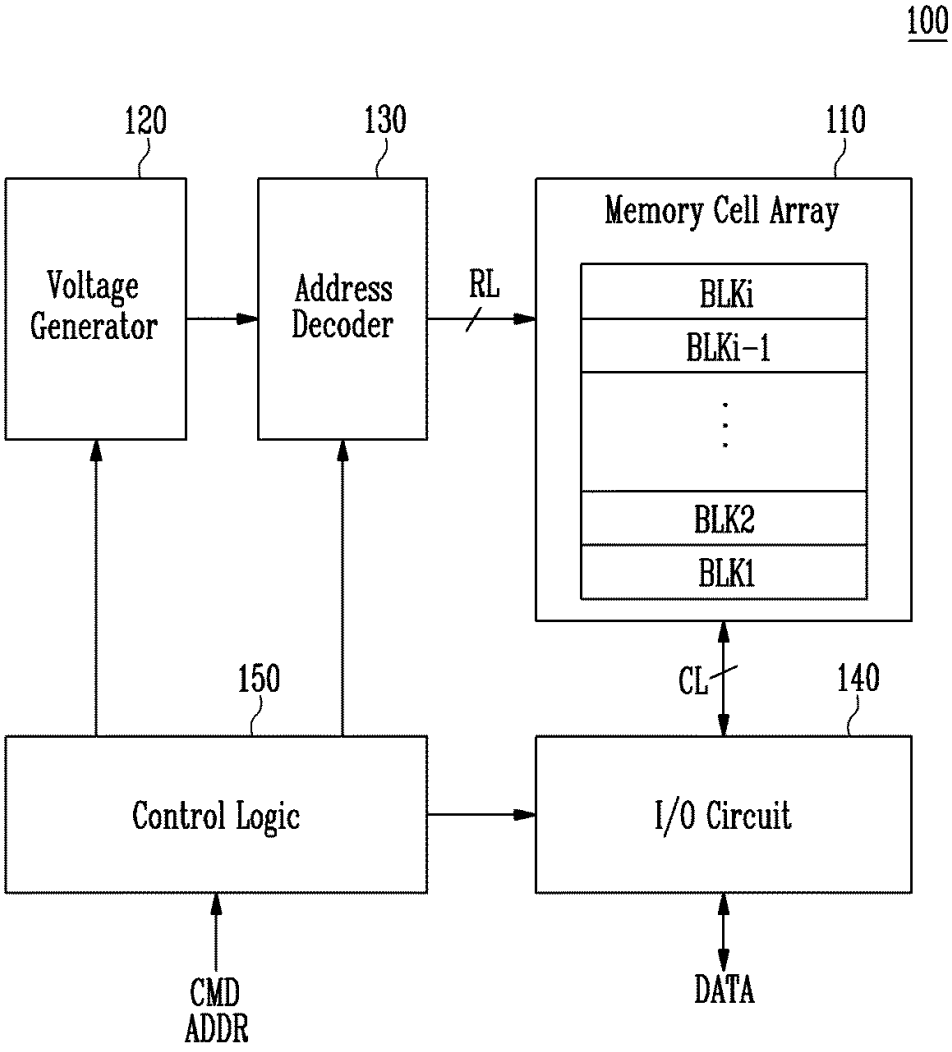

100
120
130
110
Voltage Generator
Address Decoder
RL
Memory Cell Array
BLKi
BLKi-1
BLK2
BLK1
150
CL
140
Control Logic
I/O Circuit
CMD
ADDR
DATA

FIG. 3

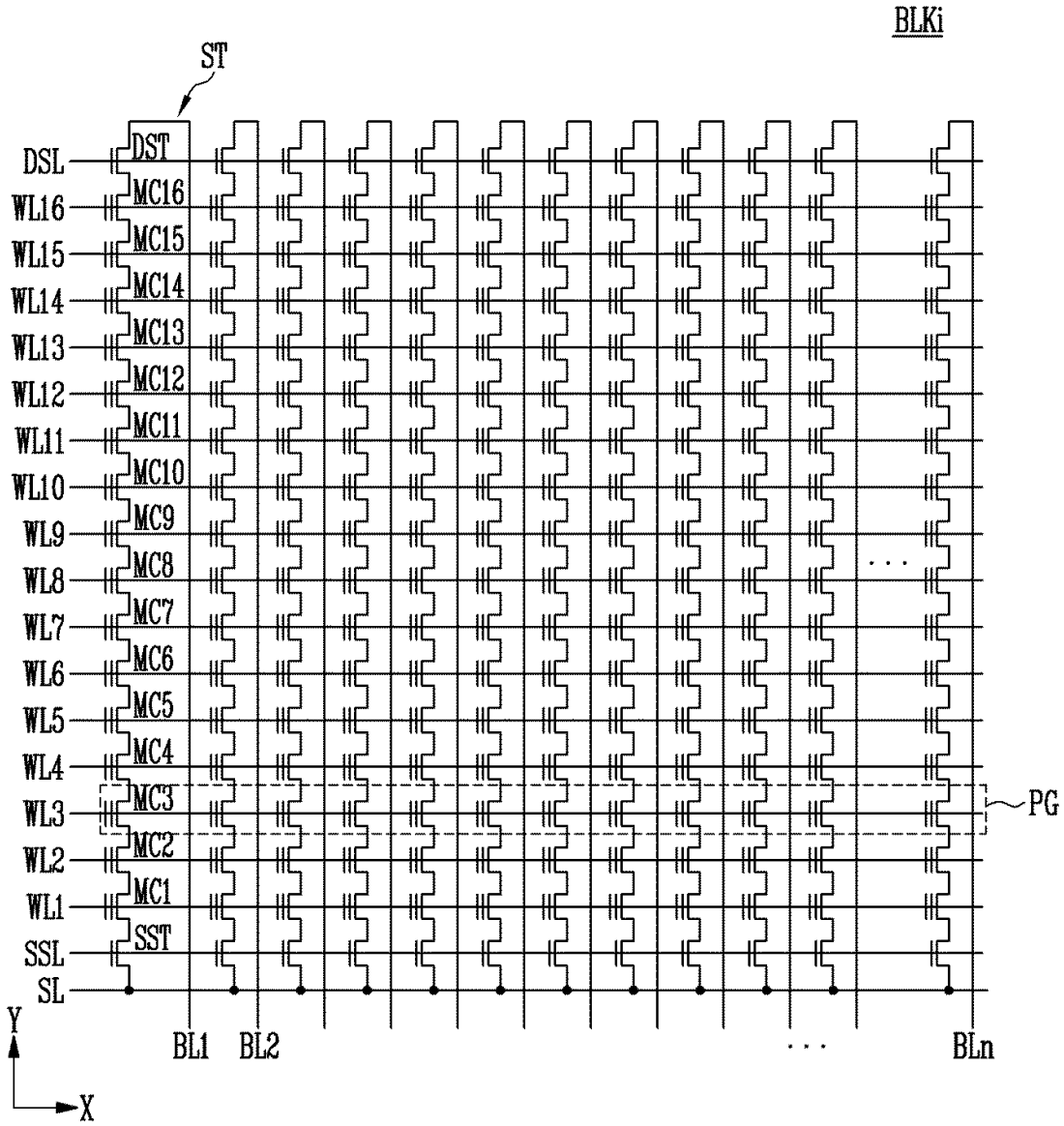

BLKi
ST
DST
DSL
MC16
WL16
MC15
WL15
MC14
WL14
MC13
WL13
MC12
WL12
MC11
WL11
MC10
WL10
MC9
WL9
MC8
WL8
MC7
WL7
MC6
WL6
MC5
WL5
MC4
WL4
MC3
WL3
MC2
WL2
MC1
WL1
SST
SSL
SL
PG
BL1
BL2
BLn
Y
X

FIG. 4A

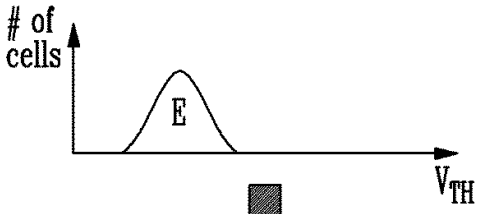


FIG. 4B

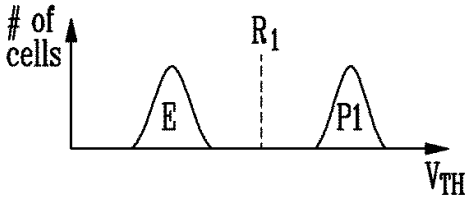


FIG. 5A

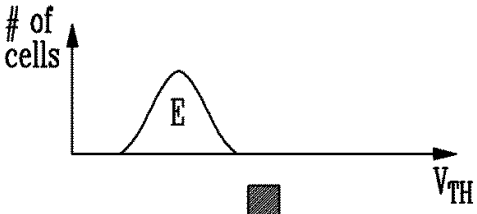


FIG. 5B

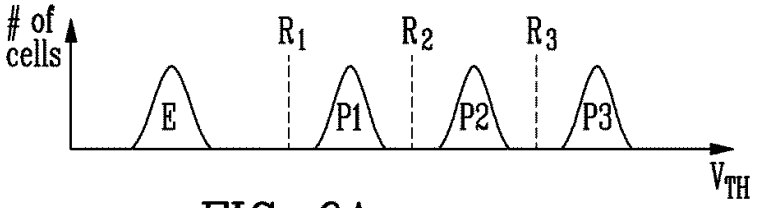


FIG. 6A

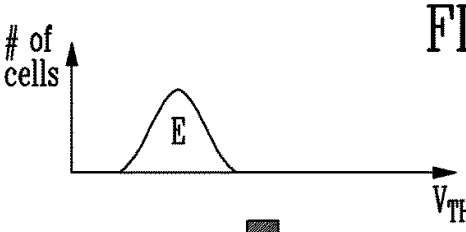
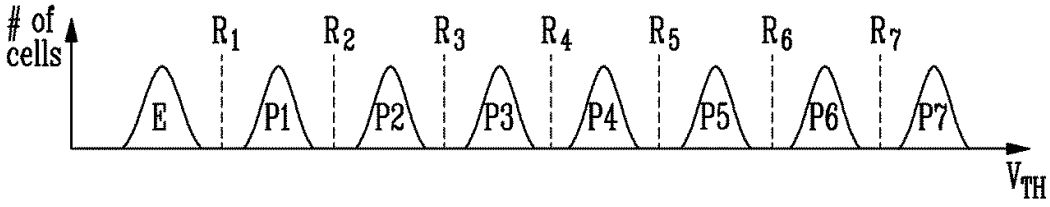


FIG. 6B



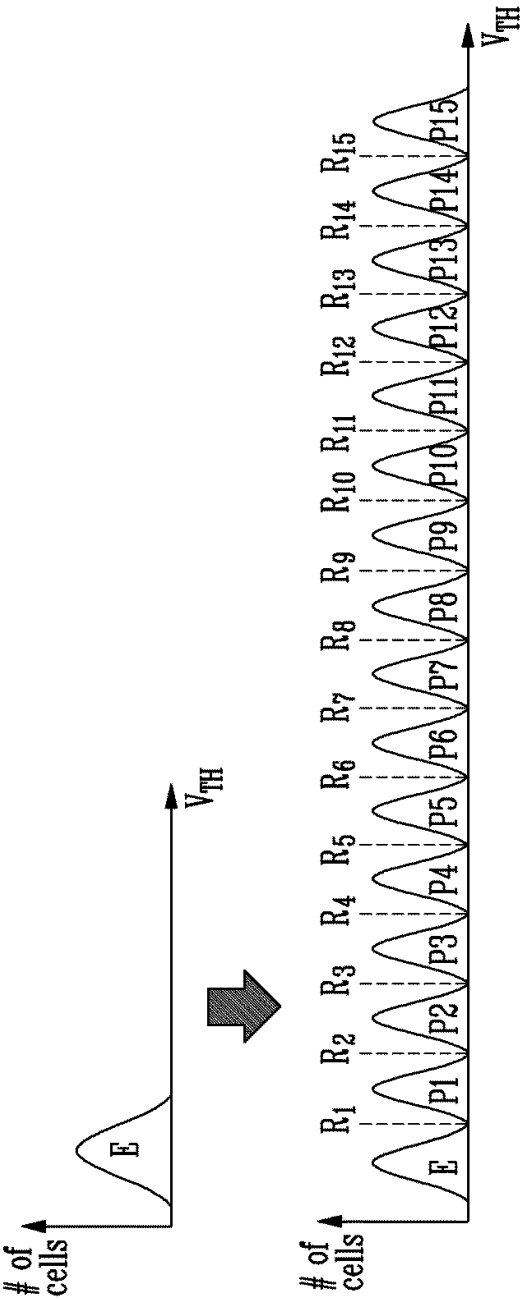

E
# of cells
V_{TH}
E
R_1 R_2 R_3 R_4 R_5 R_6 R_7 R_8 R_9 R_{10} R_{11} R_{12} R_{13} R_{14} R_{15}
P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15
# of cells
V_{TH}

FIG. 7A

FIG. 7B

FIG. 8

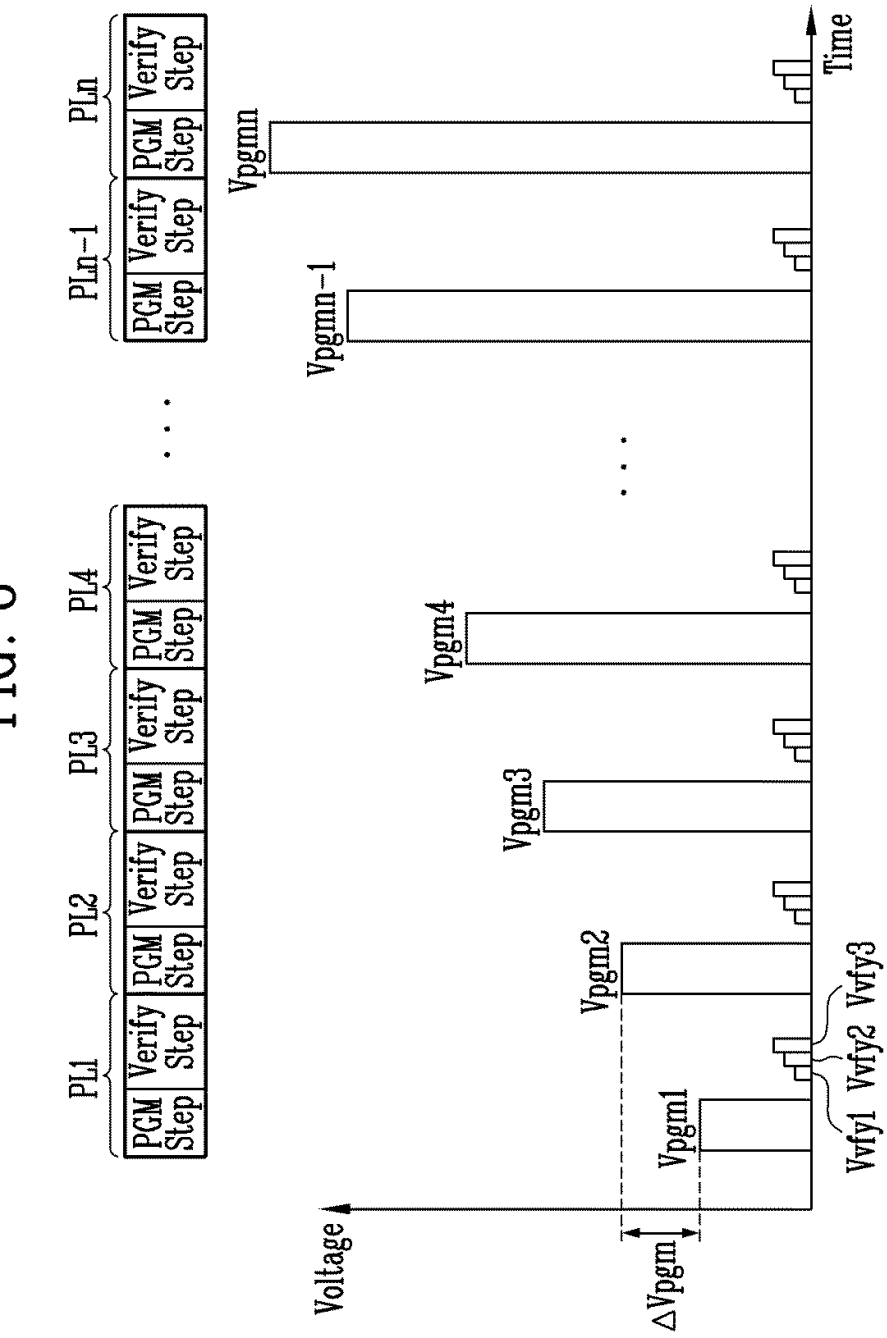

PL1
PL2
PL3
PL4
PLn-1
PLn
PGM Step
Verify Step
Voltage
Time
Vpgm1
Vpgm2
Vpgm3
Vpgm4
Vpgmn-1
Vpgmn
ΔVpgm
Vvfy1
Vvfy2
Vvfy3

FIG. 9

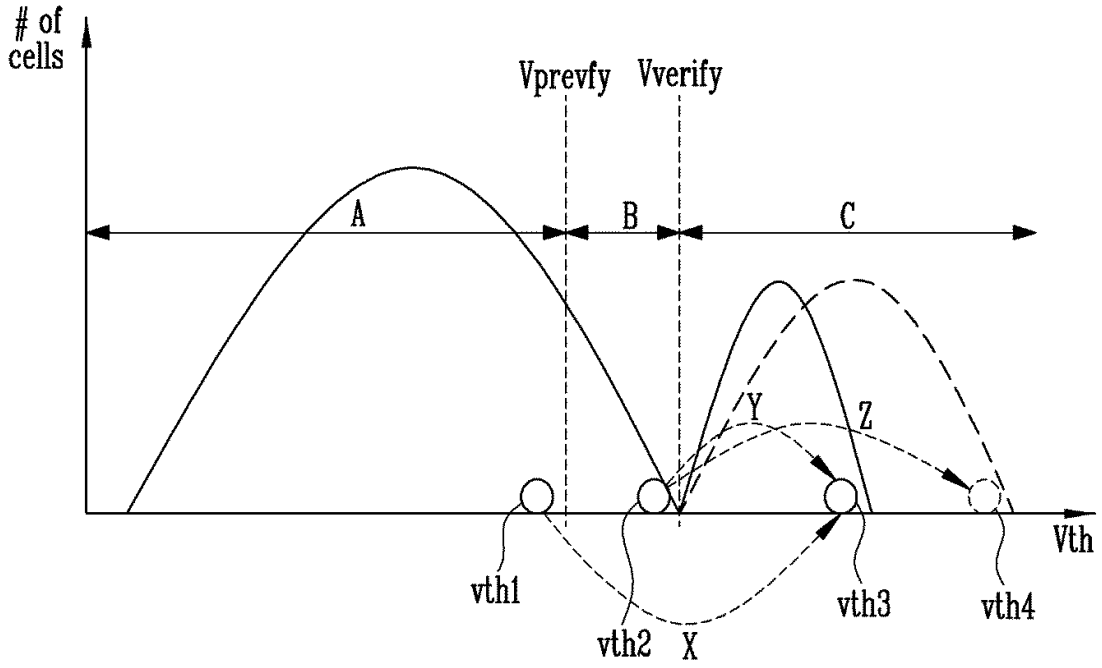

# of cells
Vprevfy
Vverify
A
B
C
Y
Z
Vth
vth1
vth2
X
vth3
vth4

FIG. 10

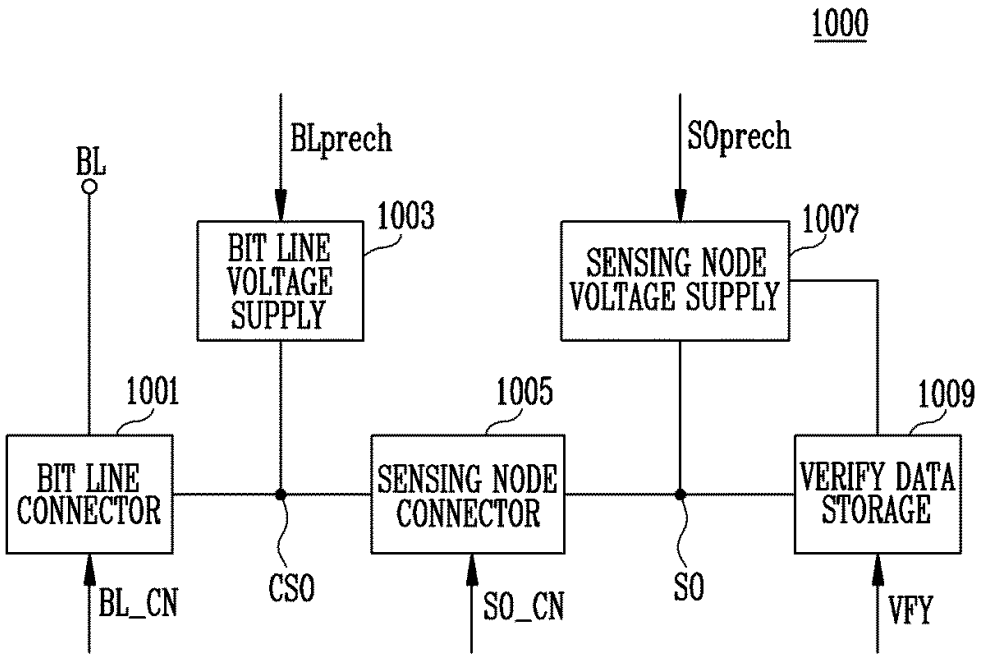

1000
BL
BLprech
1003
BIT LINE VOLTAGE SUPPLY
SOprech
1007
SENSING NODE VOLTAGE SUPPLY
1001
1005
1009
BIT LINE CONNECTOR
SENSING NODE CONNECTOR
VERIFY DATA STORAGE
BL_CN
CSO
SO_CN
SO
VFY

FIG. 11

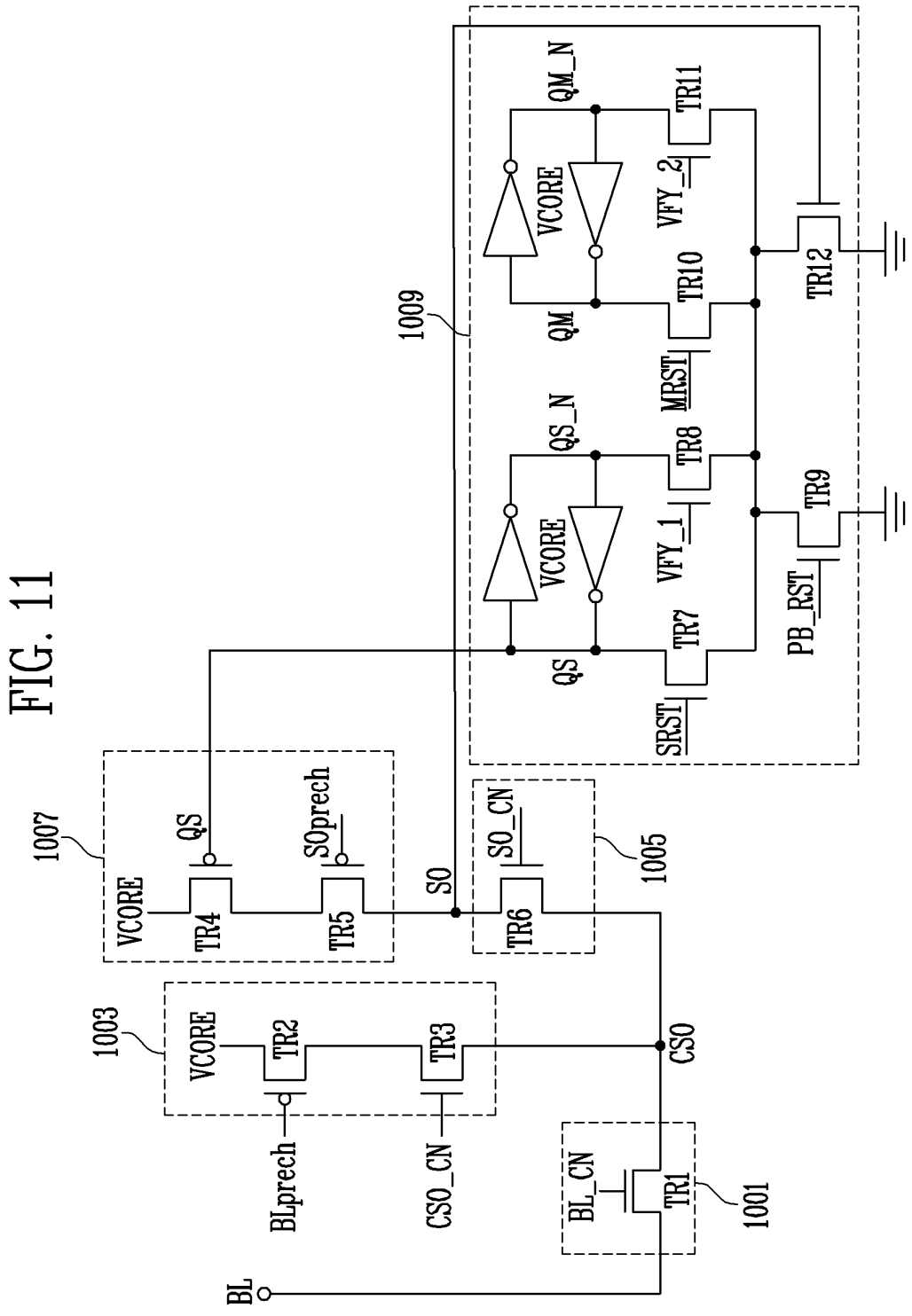

1009
QM_N
TR11
VCORE
VFY_2
TR12
QM
TR10
MRST
QS_N
TR8
VCORE
VFY_1
TR9
QS
TR7
SRST
PB_RST
1007
QS
SOprech
VCORE
TR4
TR5
SO
SO_CN
1005
TR6
1003
VCORE
TR2
TR3
CSO
BLprech
CSO_CN
BL_CN
TR1
1001
BL

FIG. 12

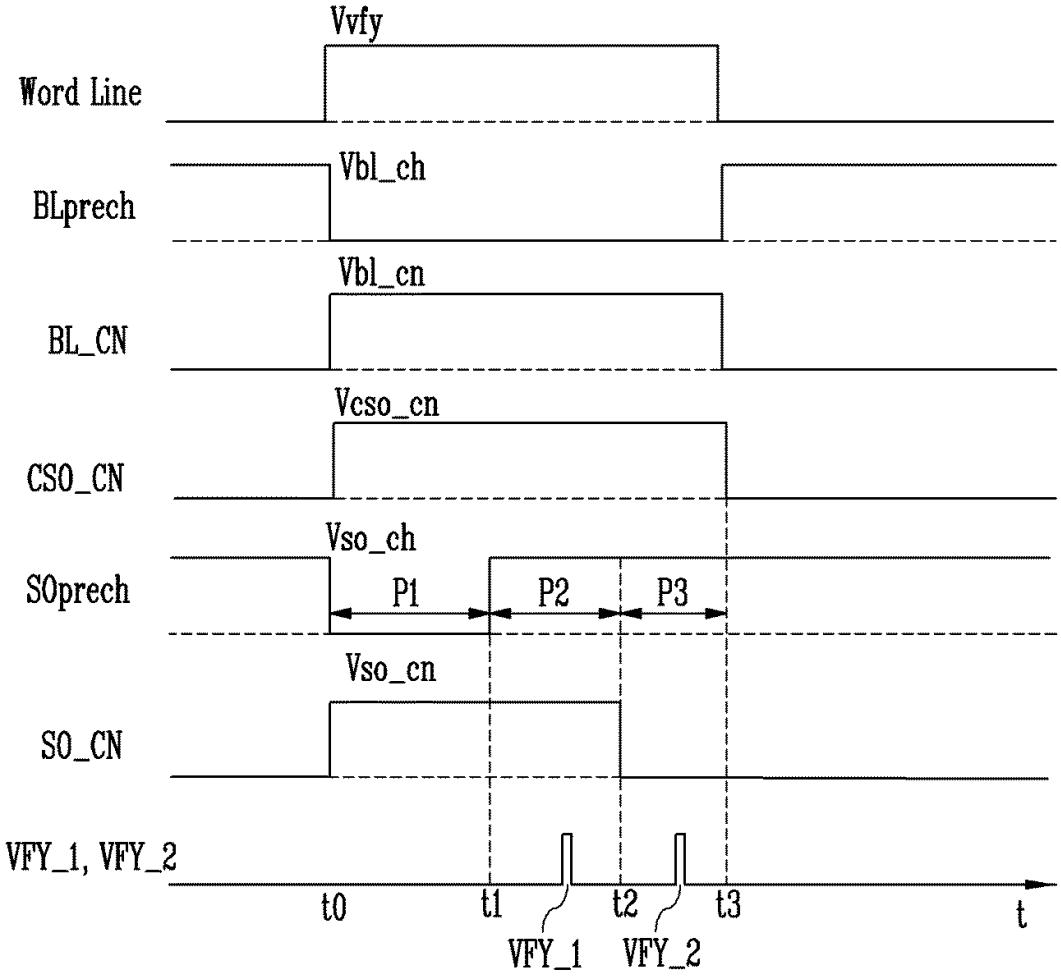

Vvfy
Word Line
Vbl_ch
BLprech
Vbl_cn
BL_CN
Vcso_cn
CSO_CN
Vso_ch
SOprech
P1
P2
P3
Vso_cn
SO_CN
VFY_1, VFY_2
t0
t1
t2
t3
t
VFY_1
VFY_2

FIG. 13

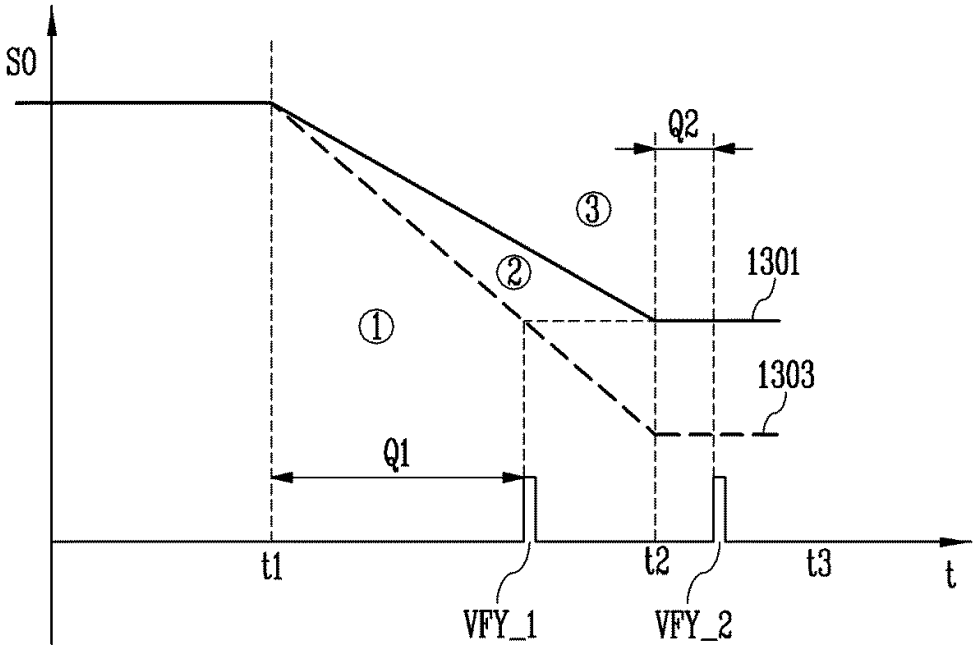

S0
Q2
③
②
①
1301
1303
Q1
t1
t2
t3
t
VFY_1
VFY_2

FIG. 14

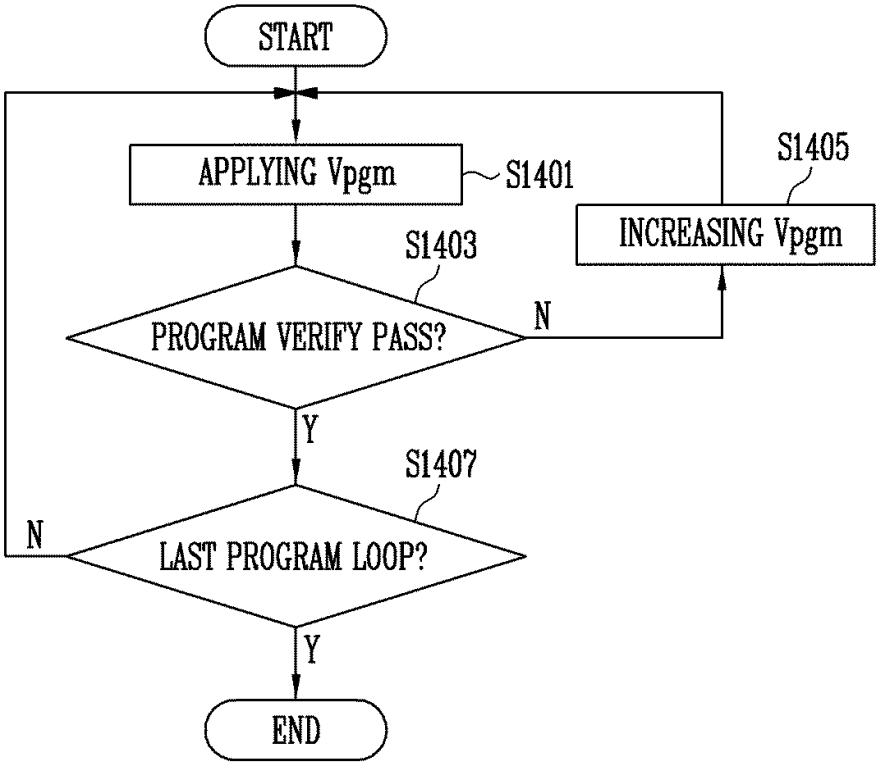

START
APPLYING Vpgm
S1401
S1405
INCREASING Vpgm
S1403
PROGRAM VERIFY PASS?
N
Y
S1407
N
LAST PROGRAM LOOP?
Y
END

FIG. 15

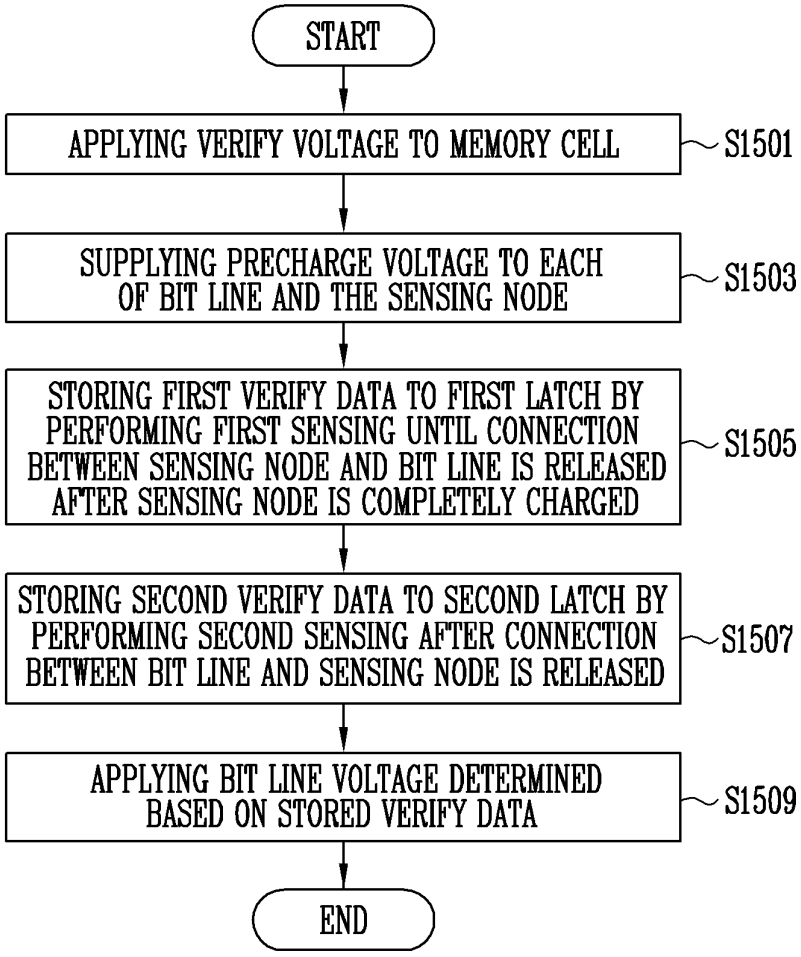

START
APPLYING VERIFY VOLTAGE TO MEMORY CELL
S1501
SUPPLYING PRECHARGE VOLTAGE TO EACH OF BIT LINE AND THE SENSING NODE
S1503
STORING FIRST VERIFY DATA TO FIRST LATCH BY PERFORMING FIRST SENSING UNTIL CONNECTION BETWEEN SENSING NODE AND BIT LINE IS RELEASED AFTER SENSING NODE IS COMPLETELY CHARGED
S1505
STORING SECOND VERIFY DATA TO SECOND LATCH BY PERFORMING SECOND SENSING AFTER CONNECTION BETWEEN BIT LINE AND SENSING NODE IS RELEASED
S1507
APPLYING BIT LINE VOLTAGE DETERMINED BASED ON STORED VERIFY DATA
S1509
END

FIG. 16

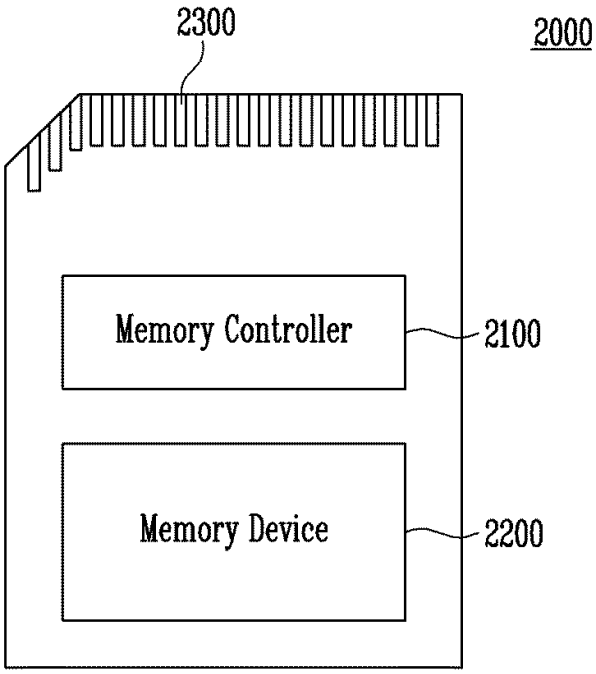


FIG. 17

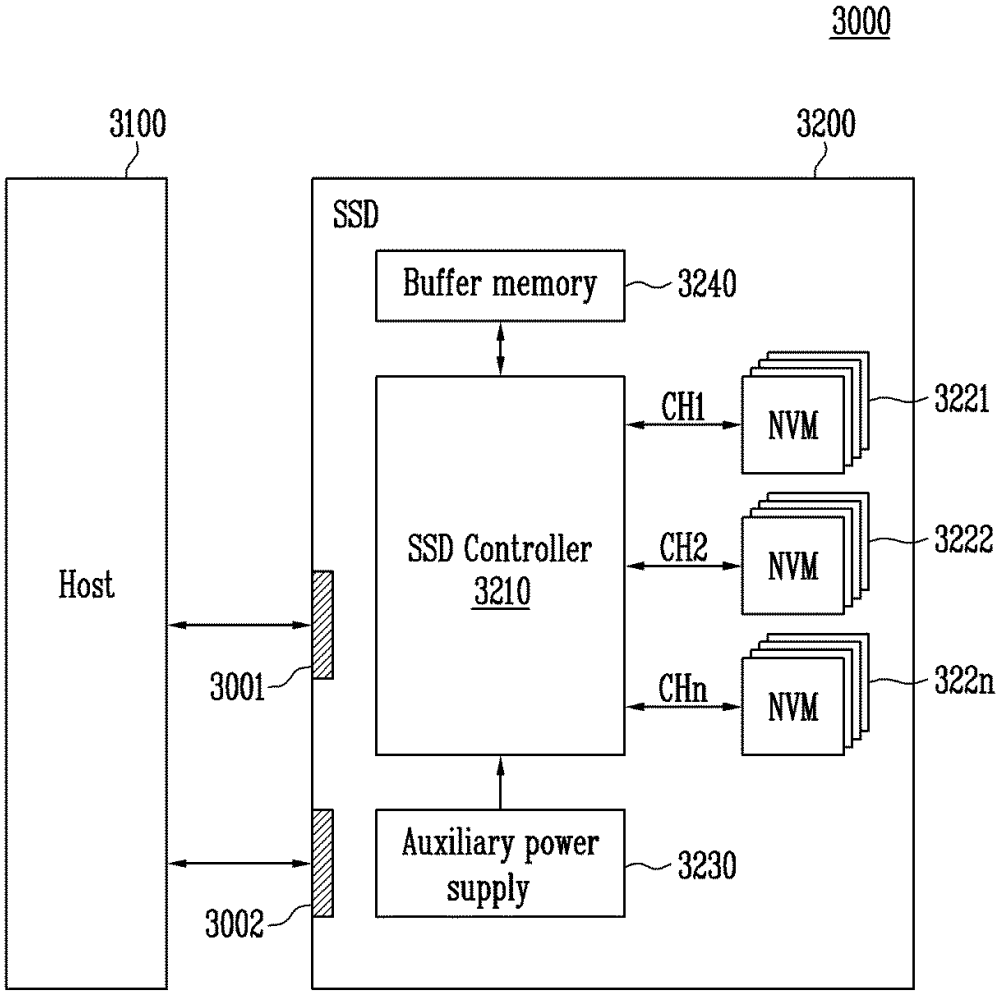
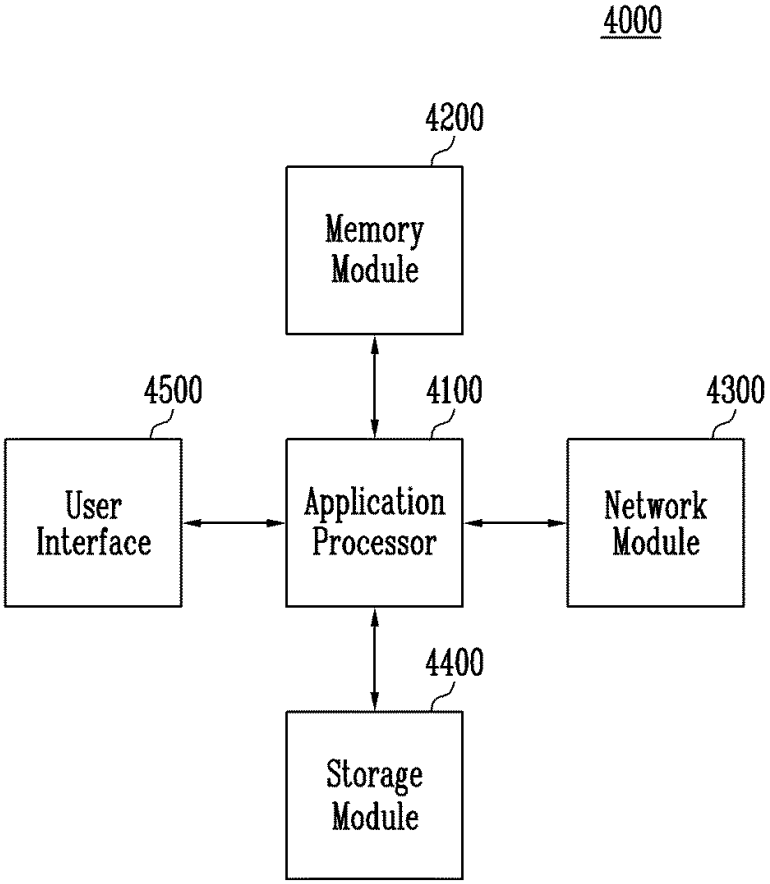

3000
3100
3200
SSD
Buffer memory
3240
SSD Controller
3210
CH1
CH2
CHn
NVM
NVM
NVM
3221
3222
322n
Host
3001
3002
Auxiliary power
supply
3230

FIG. 18


4000
4200
Memory Module
4500
4100
4300
User Interface
Application Processor
Network Module
4400
Storage Module