MEMORY DEVICE WITH SWITCHING GLASS LAYER

[0001] This application is a continuation-in-part of U.S. Patent Application Ser. No. 10/916,421, filed August 12, 2004, entitled PCRAM Device With Switching Glass Layer, and is also a continuation-in-part of U.S. Patent Application Ser. No. 10/893,299, filed July 19, 2004, entitled Resistance Variable Memory Device and Method of Fabrication. The entirety of each of these applications is hereby incorporated by reference herein.

FIELD OF THE INVENTION

[0002] The invention relates to the field of random access memory (RAM) devices formed using a resistance variable material.

BACKGROUND

[0003] Resistance variable memory elements, which include Programmable Conductive Random Access Memory (PCRAM) elements, have been investigated for suitability as semi-volatile and non-volatile random access memory devices. In a typical PCRAM device, the resistance of a chalcogenide glass backbone can be programmed to stable lower conductivity (i.e., higher resistance) and higher conductivity (i.e., lower resistance) states. An unprogrammed PCRAM device is normally in a lower conductivity, higher resistance state.

[0004] A conditioning operation forms a conducting channel of a metal-chalcogenide in the PCRAM device, which supports a conductive pathway for altering the conductivity/resistivity state of the device. The conducting channel remains in the glass backbone even after the device is erased. After the conditioning operation, a write operation will program the PCRAM device to a higher conductivity state, in which metal ions accumulate along the conducting channel(s). The PCRAM device may be read by applying a voltage of a lesser magnitude than required to program it; the current or resistance across the memory device is sensed as higher or lower to define the logic "one" and "zero" states. The PCRAM may be erased by applying a reverse voltage (opposite bias) relative to the write voltage, which disrupts the conductive pathway, but typically leaves the conducting channel intact. In this way, such a device can function as a variable resistance memory having at least two conductivity states, which can define two respective logic states, i.e., at least a bit of data.

[0005] One exemplary PCRAM device uses a germanium selenide (i.e., Ge_xSe_{100-x}) chalcogenide glass as a backbone. The germanium selenide glass has, in the prior art, incorporated silver (Ag) by (photo or thermal) doping or co-deposition. Other exemplary PCRAM devices have done away with such doping or co-deposition by incorporating a metal-chalcogenide material as a layer of silver selenide (e.g., Ag_2Se), silver sulfide (AgS), or tin selenide (SnSe) in combination with a metal layer, proximate

a chalcogenide glass layer, which during conditioning of the PCRAM provides material to form a conducting channel and a conductive pathway in the glass backbone.

[0006] Extensive research has been conducted to determine suitable materials and stoichiometries thereof for the glass backbone in PCRAM devices. Germanium selenide having a stoichiomety of about $Ge_{40}Se_{60}$ (i.e., Ge_2Se_3), as opposed to $Ge_{23}Se_{77}$ or $Ge_{30}Se_{70}$, for example, has been found to function well for this purpose. A glass backbone of $Ge_{40}Se_{60}$, with an accompanying metal-chalcogenide (e.g., typically silver selenide) layer, enables a conducting channel to be formed in the glass backbone during conditioning, which can thereafter be programmed to form a conductive pathway. The metal-chalcogenide is incorporated into chalcogenide glass layer at the conditioning step. Specifically, the conditioning step comprises applying a potential (about 0.20 V) across the memory element structure of the device such that metal-chalcogenide material is incorporated into the chalcogenide glass layer, thereby forming a conducting channel within the chalcogenide glass layer. It is theorized that Ag_2Se is incorporated onto the glass backbone at Ge-Ge sites via new Ge-Se bonds, which allows silver (Ag) migration into and out of the conducting channel during programming. Movement of metal (e.g., typically silver) ions into or out of the conducting channel during subsequent programming and erasing forms or dissolves a conductive pathway along the conducting channel, which causes a detectible conductivity (or resistance) change across the memory device.

[0007] It has been determined that $Ge_{40}Se_{60}$ works well as the glass backbone in a PCRAM device because this stoichiometry makes for a glass that is rigid and incorporates thermodynamically unstable germanium-germanium (Ge-Ge) bonds. The presence of another species, such as silver selenide provided from an accompanying layer, can, in the presence of an applied potential, break the Ge-Ge bonds and bond with the previously homopolar bonded Ge to form conducting channels. These characteristics make this "40/60" stoichiometry optimal when using a germanium selenide chalcogenide glass with respect to the formation of a conducting channel and conductive pathway.

[0008] While germanium-chalcogenide (e.g., $Ge_{40}Se_{60}$) glass layers are highly desirable for PCRAM devices, other glasses may be desirable to improve switching properties or thermal limitations of the devices.

SUMMARY

[0009] The invention provides embodiments of a method of determining suitable glass backbone material, which may be used in place of $Ge_{40}Se_{60}$ glass in a resistance variable memory device, such as a PCRAM, with other materials, a method of forming memory devices with such materials, and devices constructed in accordance with these methods.

[0010] The chalcogenide glass material may be represented by A_xB_{100-x}, where A is a non-chalcogenide material selected from Groups 3-15 of the periodic table and B is a chalcogenide material from Group 16. The method of selecting a glass material includes: (1) selection of a non-chalcogenide component A from Groups 3-15 that will exhibit homopolar bonds; (2) selection of a chalcogenide component B from Group 16 for which component A will have a bonding affinity, relative to the A-A homopolar bonds; (3) selection of a stoichiometry (i.e., x of A_xB_{100-x}) that will allow the homopolar A-A bonds to form; and (4) confirmation that the glass A_xB_{100-x}, at the selected stoichiometry (i.e., x), will allow a conducting channel and a conductive pathway to form therein upon application of a conditioning voltage (when a metal-chalcogenide layer and metal ions are proximate the glass).

[0011] An exemplary memory device constructed in accordance with an embodiment of the invention uses a germanium telluride glass backbone having a Ge_xTe_{100-x} stoichiometry and a metal-chalcogenide layer proximate thereto for a memory cell. In a specific exemplary embodiment, x is between about 44 and about 53. Also, the metal-chalcogenide layer can be a tin selenide with a stoichiometry of about SnSe. Other layers may also be associated with this glass backbone and metal-chalcogenide layer.

[0012] The above and other features and advantages of the invention will be better understood from the following detailed description, which is provided in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIGs. 1-3 show graphs of Raman shift analysis of germanium selenide glass, which may be used in selecting glass backbone materials in accordance with the invention;

[0014] FIG. 4 shows an exemplary embodiment of a memory device in accordance with the invention;

[0015] FIG. 5 shows an exemplary embodiment of a memory device in accordance with the invention;

[0016] FIGs. 6-11 show a cross-section of a wafer at various stages during the fabrication of a device in accordance with an embodiment of the invention;

[0017] FIG. 12 shows a resistance-voltage curve of a first (conditioning) write and second (programming) write for a 0.13 μm device in accordance with the invention;

[0018] FIG. 13 shows an exemplary processor-based system incorporating memory devices in accordance with the invention;

[0019] FIGs. 14a-14h are graphs showing experimental results of thermal testing conducted with devices fabricated in accordance with exemplary embodiments of the invention; and

[0020] FIG. 15 shows a graph of Raman shift analysis of germanium telluride glass.

DETAILED DESCRIPTION

[0021] In the following detailed description, reference is made to various specific embodiments of the invention. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that other embodiments may be employed, and that various structural, logical and electrical changes may be made without departing from the spirit or scope of the invention.

[0022] The term "substrate" used in the following description may include any supporting structure including, but not limited to, a semiconductor substrate that has an exposed substrate surface. A semiconductor substrate should be understood to include silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. When reference is made to a semiconductor substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor

or foundation. The substrate need not be semiconductor-based, but may be any support structure suitable for supporting an integrated circuit, including, but not limited to, metals, alloys, glasses, polymers, ceramics, and any other supportive materials as is known in the art.

[0023] The term "chalcogenide" is intended to include various alloys, compounds, and mixtures of chalcogens (elements from Group 16 of the periodic table, e.g., sulfur (S), selenium (Se), tellurium (Te), polonium (Po), and oxygen (O)).

[0024] Embodiments of the invention provide a method of selecting a glass backbone material for use in a resistance variable memory device, such as a PCRAM. The backbone material (i.e., backbone glass layer 18 of FIGs. 4 and 5) may be represented by the formula A_xB_{100-x}, where A is a non-chalcogenide material selected from Groups 3-15, and preferably 13, 14, and 15, of the periodic table and B is a chalcogenide material. The glass backbone may also be represented by the formula $(A_xB_{100-x})C_y$, where C represents one or more additional, optional components, which may be present in some glass formulations, but which may be omitted; therefore, the description hereafter will focus on two components (A and B) for simplicity sake. The ultimate choice for the material A_xB_{100-x} depends, in part, on the make up of an adjacent metal-chalcogenide layer (e.g., layer 20 of FIGs. 4 and 5) with which it operationally engages. The component A should have an affinity for the chalcogenide component B, and preferably for the chalcogenide material (which is preferably also component B) of

the metal-chalcogenide layer. Since $Ge_{40}Se_{60}$ glass has been experimentally observed to have good glass backbone properties in PCRAM devices, a backbone material represented by the formula A_xB_{100-x} should have properties similar to $Ge_{40}Se_{60}$ glass, such as homopolar bond properties and affinity of the non-chalcogenide component, e.g., Ge, for the chalcogenide component in the metal-chalcogenide layer.

[0025] Taking these characteristics into consideration, a primary consideration in selecting components A and B and the stoichiometry for a glass backbone material is that the resulting material contain thermodynamically unstable homopolar bonds of component A, meaning that the non-chalcogenide component A may form a bond with another component A in the glass, as initially formed, only if there is an insufficient amount of component B to satisfy the coordination number requirement for component A, which allows for the formation homopolar A-A bonds. The A-A homopolar bonds in such a glass material are thermodynamically unstable and will themselves break when the device is programmed and a conducting channel is formed in the glass backbone by the metal-chalcogenide layer when the chalcogenide component for the metal-chalcogenide layer bonds to the component A participating in the homopolar bonds. This property is dependent on the stoichiometry of the material A_xB_{100-x} in that excess chalcogenide component B will inhibit the formation of homopolar A-A bonds.

[0026] What "excess" chalcogenide component B means in relation to the material A_xB_{100-x} and its stoichiometry may be determined by whether the material

exhibits the homopolar bonds or not. Raman spectroscopy can be a useful analytical tool for determining the presence of homopolar bonds when selecting a material A_xB_{100-x} for the glass backbone in PCRAM devices. Raman Spectroscopy is based on the Raman effect, which is the inelastic scattering of photons by molecules. A plot of Raman intensity (counts) vs. Raman shift (cm^{-1}) is a Raman spectrum, which is the basis for FIGs. 1-3.

[0027] Referring now to FIG. 1, which is a Raman spectrum for bulk $Ge_{23}Se_{77}$ glass, it can be observed by the Raman Shift peaks at about 200 cm^{-1} and at about 260 cm^{-1} that the glass incorporates Ge-Se bonds and Se-Se (i.e., chalcogenide) bonds. This is an undesirable stoichiometry for the glass backbone since it lacks the homopolar Ge-Ge (i.e., non-chalcogenide) bonds desirable for switching in a device comprising a germanium selenide glass. Compare FIG. 1 to FIG. 2, the latter of which is a Raman spectrum for bulk $Ge_{40}Se_{60}$ glass, which shows a Raman Shift peak at about 175 cm^{-1} that corresponds to Ge-Ge homopolar bonds and a peak at about 200 cm^{-1} that corresponds to Ge-Se bonds. The prevalence of non-chalcogenide (i.e., Ge-Ge) homopolar bonds found in $Ge_{40}Se_{60}$ is a characteristic sought in materials for the glass backbone in PCRAM. This characteristic may also be seen in a thin film of $Ge_{40}Se_{60}$ using Raman spectra, as shown in FIG. 3. Similar comparisons of Raman spectra may be made for other materials A_xB_{100-x} of varying stoichiometries to find spectra showing peaks

demonstrating homopolar bonding of the non-chalcogenide component (i.e., A-A) in the material, which indicates that it has suitable properties for a glass backbone.

[0028] Taking the aforementioned desired characteristics into consideration, the method of detecting a suitable glass backbone may be performed by the following steps: (1) selection of a non-chalcogenide component A from Groups 3-15 that will exhibit homopolar bonds; (2) selection of a chalcogenide component B from Group 16 for which component A will have a bonding affinity, relative to the A-A homopolar bonds; (3) selection of a stoichiometry (i.e., x of A_xB_{100-x}) that will provide for a thermodynamically unstable glass and will allow the homopolar A-A bonds to form; and (4) confirmation that the glass A_xB_{100-x}, at the selected stoichiometry (i.e., x), will allow a conducting channel and a conductive pathway to form therein upon application of a conditioning voltage (when a metal-chalcogenide, e.g., M_yB_{100-y}, and metal ions are proximate the glass).

[0029] Using the above-discussed methodology for selecting glass backbone materials A_xB_{100-x}, at least four have been found preferable for use in PCRAM devices. These materials include arsenic selenide, represented by formula $As_{50}Se_{50}$, tin selenide, represented by formula $Sn_{50}Se_{50}$, antimony selenide, represented by formula Sb_xSe_{100-x}, and germanium telluride, represented by formula Ge_xTe_{100-x}. As shown by FIG. 15, the Raman shift peaks for germanium telluride glass are at about 140 counts/cm^{-1} (for Ge-Ge bonds) and about 180 counts/cm_{-1} (for Te-Te bonds), demonstrating at least one

favorable characteristic of the glass for PCRAM. Although each of these exemplary materials include selenium or tellurium for component B, other chalcogenides may be used as well.

[0030] The invention is now explained with reference to the other figures, which illustrate exemplary embodiments and throughout which like reference numbers indicate like features. FIG. 4 shows an exemplary embodiment of a memory device 100 constructed in accordance with the invention. The device 100 shown in FIG. 4 is supported by a substrate 10. Over the substrate 10, though not necessarily directly so, is a conductive address line 12, which serves as an interconnect for the device 100 shown and for a plurality of other similar devices of a portion of a memory array of which the shown device 100 is a part. It is possible to incorporate an optional insulating layer (not shown) between the substrate 10 and address line 12, and this may be preferred if the substrate 10 is semiconductor-based. The conductive address line 12 can be any material known in the art as being useful for providing an interconnect line, such as doped polysilicon, silver (Ag), gold (Au), copper (Cu), tungsten (W), nickel (Ni), aluminum (Al), platinum (Pt), titanium (Ti), and other materials.

[0031] Over the address line 12 is a first electrode 16, which can be defined within an insulating layer 14 (or may be a common blanket electrode layer; not shown), which is also over the address line 12. This electrode 16 can be any conductive material that will not migrate into chalcogenide glass, but is preferably tungsten (W). The

insulating layer 14 should not allow the migration of metal ions and can be an insulating nitride, such as silicon nitride (Si_3N_4), a low dielectric constant material, an insulating glass, or an insulating polymer, but is not limited to such materials.

[0032] A memory element, i.e., the portion of the memory device 100 which stores information, is formed over the first electrode 16. In the embodiment shown in FIG. 4, a chalcogenide glass layer 18 is provided over the first electrode 16. The chalcogenide glass layer 18 has the stoichiometric formula A_xB_{100-x}, with A being a non-chalcogenide component and B being a chalcogenide component as discussed above. The material A_xB_{100-x} may be many materials with the appropriate characteristics (e.g., homopolar bonds, homopolar bond strength, thermodynamic instability, etc.) and an appropriate stoichiometry, as discussed above, but is preferably be selected from $Sn_{50}Se_{50}$, Sb_xSe_{100-x}, $As_{50}Se_{50}$, and Ge_xTe_{100-x}, which have been found to be suitable by following the methodology discussed above. Germanium telluride with a formula Ge_xTe_{100-x}, where x is between about 44 and 53, is the preferred material for layer 18. More preferably, x is between 46 and 51 and most preferably, x is about 47. This may be written as $Ge_{46}Te_{54}$ to $Ge_{51}Te_{49}$. Germanium telluride is a particularly good selection for the chalcogenide glass layer 18 because, as shown by the Raman data in FIG. 15, it exhibits the Ge-Ge homopolar bonds desirable for such glass. Also, when used with a metal-chalcogenide layer 20 of tin selenide (SnSe), the tin selenide allows for the

formation of a Ge-Se bond and the development of a channel for metal (e.g., Ag) ion migration during operation of the memory device.

[0033] The layer of chalcogenide glass 18 is preferably between about 100 Å and about 1000 Å thick, most preferably about 300 Å thick. Layer 18 need not be a single layer of glass, but may also be comprised of multiple sub-layers of chalcogenide glass having the same or different stoichiometries. This layer of chalcogenide glass 18 is in electrical contact with the underlying electrode 16.

[0034] Over the chalcogenide glass layer 18 is a layer of metal-chalcogenide 20, which may be any combination of metal component M, which may be selected from any metals, and chalcogenide component B, which is preferably the same chalcogenide as in the glass backbone layer 18, and may be represented by the formula M_yB_{100-y}. As with the glass backbone layer 18 material, other components may be added, but the metal-chalcogenide will be discussed as only two components M and B for simplicity sake. The metal-chalcogenide may be, for example, silver selenide (Ag_ySe, y being about 20) or, preferably, tin selenide ($Sn_{10+/-y}Se$, where y is between about 10 and 0). The metal-chalcogenide layer 20 is preferably about 500 Å thick; however, its thickness depends, in part, on the thickness of the underlying chalcogenide glass layer 18. The ratio of the thickness of the metal-chalcogenide layer 20 to that of the underlying chalcogenide glass layer 18 should be between about 5:1 and about 1:1, more preferably about 2.5:1.

[0035] Still referring to FIG. 4, a metal layer 22 is provided over the metal-chalcogenide layer 20, with the metal of layer 22 preferably incorporating some silver, if not being exclusively silver. The metal layer 22 should be about 500 Å thick. The metal layer 22 assists the switching operation of the memory device 100. Over the metal layer 22 is a second electrode 24. The second electrode 24 can be made of the same material as the first electrode 16, but is not required to be so. In the exemplary embodiment shown in FIG. 4, the second electrode 24 is preferably tungsten (W). The device(s) 100 may be isolated by an insulating layer 26.

[0036] FIG. 5 shows another exemplary embodiment of a memory device 101 constructed in accordance with the invention. Memory device 101 has many similarities to memory device 100 of FIG. 4 and layers designated with like reference numbers are preferably the same materials and have the same thicknesses as those described in relation to the embodiment shown in FIG. 4. For example, the first electrode 16 is preferably tungsten. The chalcogenide glass layer 18 material A_xB_{100-x} is selected according to the methodology detailed above and can be germanium telluride; it is preferably about 150 Å thick. As with device 100 of FIG. 4, the metal-chalcogenide layer 20 may be any combination M_yB_{100-y}, but can be tin selenide; it is preferably about 470 Å thick. The metal layer 22 preferably contains some silver, but can be mostly or wholly silver; it is preferably about 200 Å thick. The primary difference between device

100 and device 101 is the addition to device 101 of additional second and third chalcogenide layers 18a and 18b.

[0037] The second chalcogenide glass layer 18a is formed over the metal-chalcogenide layer 20 and is preferably about 150 Å thick. Over this second chalcogenide glass layer 18a is metal layer 22. Over the metal layer 22 is a third chalcogenide glass layer 18b, which is preferably about 100 Å thick. The third chalcogenide glass layer 18b provides an adhesion layer for subsequent electrode formation. As with layer 18 of FIG. 4, layers 18a and 18b are not necessarily a single layer, but may be comprised of multiple sub-layers. Additionally, the second and third chalcogenide layers 18a and 18b may be a different glass material from the first chalcogenide glass layer 18 or from each other. Glass material preferred for layers 18a and 18b is germanium selenide (Ge_xSe_{100-x}), more preferably Ge_2Se_3, but other materials may be useful as well, including germanium telluride (Ge_xTe_{100-x}), arsenic selenide (As_xSe_{100-x}), tin selenide (Sn_xSe_{100-x}), antimony selenide (Sb_xSe_{100-x}), , germanium sulfide (Ge_xS_{100-x}), and combinations of germanium (Ge), silver (Ag), and selenium (Se). The second electrode 24 is preferably tungsten (W), but may be other metals also.

[0038] As shown by FIGs. 14a-14h, PCRAM devices in accordance with the above-discussed embodiment (FIG. 5) were experimentally tested for memory operation under varied thermal conditions. Each chart (FIGs. 14a-14h) represents a set of thermal tests on a respective PCRAM device. Similar to the device shown in FIG. 5,

each tested device had a tungsten (W) first electrode (e.g., layer 16), a 300Å germanium telluride (Ge_xTe_{100-x}, $x \cong 44$ to 53) layer (e.g., layer 18) thereover, a 900Å tin selenide (SnSe) layer (e.g., layer 20) thereover, a 150Å germanium selenide (Ge_2Se_3) layer (e.g., layer 18a) thereover, a 500Å silver (Ag) layer (e.g., layer 22) thereover, a 100Å germanium selenide (Ge_2Se_3) layer (e.g., layer 18b) thereover, and a tungsten (W) second electrode (e.g., layer 24).

[0039] The testing was conducted by positioning wafers, which supported the PCRAM devices, on a temperature-controllable chuck and DC programming ten (10) devices at the temperatures shown on the charts in FIGs. 14a-14h. The DC probing procedure was conducted on each device as follows: (1) sweep potential from 0 to 800 mV and read resistance of cell at 10 mV to determine the initial resistance (Ri); (2) sweep the potential from 0 to 10 mV and record the resistance at 10 mV to obtain the write resistance (Rw1); (3) sweep the device from 0 to -1 V and record the potential at which the device erased and the current at that erase potential to determine the erase voltage and erase current; (4) sweep the device from 0 to 800 mV and read the resistance at 10 mV (this is the Rerase) and record the potential at which the device switched (i.e., was written; the Vw2); and (5) sweep the potential from 0 to 10 mV and record the resistance at 10 mV (this is the Rw2). The charts of FIGs. 14a-14h show these measured parameters (i.e., Vw1, Vw2, Ri, erase current, erase voltage, Rw1, Rw2, Rerase) for 10 experimental devices constructed in accordance with the invention at the

temperatures shown along the x-axis of the charts. The results show that germanium tellurium based PCRAM cells have thermal tolerances suitable for use in memory devices.

[0040] The above-discussed embodiments are exemplary embodiments of the invention; however, other exemplary embodiments may be used which combine the first electrode layer 16 and address line layer 12. Another exemplary embodiment may use blanket layers (e.g., layers 16, 18, 20, and 22 of FIG. 4) of the memory cell body, where the memory cell is defined locally by the position of the second electrode 24 over the substrate 10. Another exemplary embodiment may form the memory device within a via. Additional layers, such as barrier layers or alloy-controlling layers, not specifically disclosed in the embodiments shown and discussed above, may be added to the devices in accordance with the invention without departing from the scope thereof.

[0041] FIGs. 6-11 illustrate a cross-sectional view of a wafer during the fabrication of a memory device 100 as shown by FIG. 1. Although the processing steps shown in FIGs. 6-11 most specifically refer to memory device 100 of FIG. 1, the methods and techniques discussed may also be used to fabricate memory devices of other embodiments (e.g., device 101 of FIG. 5) as would be understood by a person of ordinary skill in the art.

[0042] As shown by FIG. 6, a substrate 10 is provided. As indicated above, the substrate 10 can be semiconductor-based or another material useful as a supporting structure as is known in the art. If desired, an optional insulating layer (not shown) may be formed over the substrate 10; the optional insulating layer may be silicon nitride or other insulating materials used in the art. Over the substrate 10 (or optional insulating layer, if desired), a conductive address line 12 is formed by depositing a conductive material, such as doped polysilicon, aluminum, platinum, silver, gold, nickel, but preferably tungsten, patterning one or more conductive lines, for instance with photolithographic techniques, and etching to define the address line 12. The conductive material may be deposited by any technique known in the art, such as sputtering, chemical vapor deposition, plasma enhanced chemical vapor deposition, evaporation, or plating.

[0043] Still referring to FIG. 6, over the address line 12 is formed an insulating layer 14. This layer 14 can be silicon nitride, a low dielectric constant material, or many other insulators known in the art that do not allow metal (e.g., silver, copper, or other metal) ion migration, and may be deposited by any method known in the art. An opening 14a in the insulating layer is made, for example, by photolithographic and etching techniques, thereby exposing a portion of the underlying address line 12. Over the insulating layer 14, within the opening 14a, and over the address line 12 is formed a conductive material, preferably tungsten (W). A chemical mechanical polishing step

may then be utilized to remove the conductive material from over the insulating layer 14, to leave it as a first electrode 16 over the address line 12, and planarize the wafer.

[0044] FIG. 7 shows the cross-section of the wafer of FIG. 6 at a subsequent stage of processing. A series of layers making up the memory device 100 (FIG. 4) are blanket-deposited over the wafer. A chalcogenide glass layer 18 is formed to a preferred thickness of about 300Å over the first electrode 16 and insulating layer 14. The chalcogenide glass layer 18 is Ge_xTe_{100-x}, where x is between about 44 to 53, but may also be selected from other materials such as $As_{50}Se_{50}$, $Sn_{50}Se_{50}$, and Sb_xSe_{100-x}, and as described above, may be selected from many materials A_xB_{100-x} with appropriate characteristics and of an appropriate stoichiometry for memory function.

[0045] The steps in selecting a chalcogenide glass layer 18 material are: (1) selection of a non-chalcogenide component A from Groups 3-15 that will exhibit homopolar bonds; (2) selection of a chalcogenide component B from Group 16 for which component A will have a bonding affinity, relative to the A-A homopolar bonds; (3) selection of a stoichiometry (i.e., x of A_xB_{100-x}) that will provide for thermodynamically unstable homopolar A-A bonds; and (4) confirmation that the glass A_xB_{100-x}, at the selected stoichiometry (i.e., x), will allow a conducting channel and a conductive pathway to form therein upon application of a conditioning voltage when a metal-chalcogenide layer 20 is proximate the glass layer 18. Once the materials are selected, deposition of the chalcogenide glass layer 18 may be accomplished by any

suitable method, such as evaporative techniques or chemical vapor deposition; however, the preferred technique utilizes either sputtering or co-sputtering.

[0046] Still referring to FIG. 7, a metal-chalcogenide layer 20, e.g., M_yB_{100-y}, is formed over the chalcogenide glass layer 18. The metal-chalcogenide layer 20 is preferably tin selenide (SnSe), particularly when germanium telluride is used as the chalcogenide glass layer 18. Physical vapor deposition, chemical vapor deposition, co-evaporation, sputtering, or other techniques known in the art may be used to deposit layer 20 to a preferred thickness of about 500 Å. Again, the thickness of layer 20 is selected based, in part, on the thickness of layer 18 and the ratio of the thickness of the metal-chalcogenide layer 20 to that of the underlying chalcogenide glass layer 18 is preferably from about 5:1 to about 1:1, more preferably about 2.5:1. It should be noted that, as the processing steps outlined in relation to FIGs. 6-11 may be adapted for the formation of other devices in accordance the invention, e.g., the layers may remain in blanket-deposited form, a barrier or alloy-control layer may be formed adjacent to the metal-chalcogenide layer 20, on either side thereof, or the layers may be formed within a via.

[0047] Still referring to FIG. 7, a metal layer 22 is formed over the metal-chalcogenide layer 20. The metal layer 22 preferably incorporates at least some silver (Ag), if not exclusively being silver (Ag), but may be other metals as well, such as

copper (Cu) or a transition metal, and is formed to a preferred thickness of about 300 Å. The metal layer 22 may be deposited by any technique known in the art.

[0048] Still referring to FIG. 7, over the metal layer 22, a conductive material is deposited for a second electrode 24. Again, this conductive material may be any material suitable for a conductive electrode, but is preferably tungsten; however, other materials may be used such as titanium nitride or tantalum, for example.

[0049] Now referring to FIG. 8, a layer of photoresist 28 is deposited over the top electrode 24 layer, masked and patterned to define the stacks for the memory device 100, which is but one of a plurality of like memory devices of a memory array. An etching step is used to remove portions of layers 18, 20, 22, and 24, with the insulating layer 14 used as an etch stop, leaving stacks as shown in FIG. 9. The photoresist 30 is removed, leaving a substantially complete memory device 100, as shown by FIG. 9. An insulating layer 26 may be formed over the device 100 to achieve a structure as shown by FIGs. 4, 10, and 11. This isolation step can be followed by the forming of connections (not shown) to other circuitry of the integrated circuit (e.g., logic circuitry, sense amplifiers, etc.) of which the memory device 100 is a part, as is known in the art.

[0050] As shown in FIG. 10, a conditioning step is performed by applying a voltage pulse of about 0.20 V to incorporate material from the metal-chalcogenide layer 20 into the chalcogenide glass layer 18 to form a conducting channel 30 in the chalcogenide glass layer 18. The conducting channel 30 will support a conductive

pathway 32, as shown in FIG. 11, upon application of a programming pulse of about 0.17 V during operation of the memory device 100.

[0051] The embodiments described above refer to the formation of only a few possible resistance variable memory device structures (e.g., PCRAM) in accordance with the invention, which may be part of a memory array. It must be understood, however, that the invention contemplates the formation of other memory structures within the spirit of the invention, which can be fabricated as a memory array and operated with memory element access circuits.

[0052] FIG. 12 shows a resistance-voltage curve of a first write, which corresponds to a conditioning voltage, and a second write, which corresponds to a programming voltage, for a 0.13 μm device such as device 100 or 101 shown in FIGs. 4 and 5, respectively. The device represented by the curve of FIG. 12 has an $As_{50}Se_{50}$ chalcogenide glass layer 18 (See FIGs. 4 and 5). FIG. 12 shows that the first write is at a slightly higher potential than the second write (i.e., about 0.2 V. compared to about 0.17 V, respectively). This is because the first write conditions the device in accordance with the processing shown at FIG. 10 by forming a conducting channel 30, which remains intact after this first write. The second write requires less voltage because the stable conducting channel 30 is already formed by the conditioning write and the conductive pathway 32 is formed more easily. Application of these write voltages programs the device to a non-volatile higher conductivity, lower resistivity, memory state. These

observed programming parameters utilizing a chalcogenide glass layer 18 selected in accordance with the invention show that the tested devices work as well as when $Ge_{40}Se_{60}$ is used as the glass backbone.

[0053] The erase potential for a device having an $As_{50}Se_{50}$ chalcogenide glass layer (e.g., layer 18) is also similar to a device having $Ge_{40}Se_{60}$ glass. This erase voltage curve is not shown in FIG. 12; however, the erase potential is about -0.06 V, which returns the device to a non-volatile higher resistance, lower conductivity memory state.

[0054] FIG. 13 illustrates a typical processor system 400 which includes a memory circuit 448, e.g., a PCRAM device, which employs resistance variable memory devices (e.g., devices 100 and 101) fabricated in accordance with an embodiment the invention. A processor system, such as a computer system, generally comprises a central processing unit (CPU) 444, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 446 over a bus 452. The memory circuit 448 communicates with the CPU 444 over bus 452 typically through a memory controller.

[0055] In the case of a computer system, the processor system may include peripheral devices such as a floppy disk drive 454 and a compact disc (CD) ROM drive 456, which also communicate with CPU 444 over the bus 452. Memory circuit 448 is preferably constructed as an integrated circuit, which includes one or more resistance

variable memory devices, e.g., device 100. If desired, the memory circuit 448 may be combined with the processor, for example CPU 444, in a single integrated circuit.

[0056] The above description and drawings should only be considered illustrative of exemplary embodiments that achieve the features and advantages of the invention. Modification and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

[0057] What is claimed as new and desired to be protected by Letters Patent of the United States is:

CLAIMS

1. A method of forming a memory device, comprising:

providing a first electrode and a second electrode;

providing a metal-chalcogenide layer between said first and second electrodes

providing a germanium telluride glass between said first and second electrodes and in contact with said metal-chalcogenide layer.

2. The method of claim 1, wherein said metal-chalcogenide layer is between said chalcogenide glass layer and said second electrode.

3. The method of claim 1, wherein said metal-chalcogenide layer comprises silver selenide.

4. The method of claim 1, wherein said metal-chalcogenide layer comprises tin selenide.

5. The method of claim 4, further comprising providing a metal layer between said metal-chalcogenide layer and said second electrode.

6. The method of claim 5, wherein said metal layer comprises silver.

7. The method of claim 5, further comprising providing a first chalcogenide glass layer between said metal-chalcogenide layer and said metal layer.

8. The method of claim 9, further comprising providing a second chalcogenide glass layer between said metal layer and said second electrode.

9. The method of claim 1, wherein said germanium telluride layer has a stoichiometric formula Ge_xTe_{100-x}, where x is about 44 to about 53.

10. The method of claim 1, wherein said germanium telluride layer has a stoichiometric formula Ge_xTe_{100-x}, where x is about 46 to about 51.

11. The method of claim 1, wherein said germanium telluride layer has a stoichiometric formula Ge_xTe_{100-x}, where x is about 47.

12. A method of forming a memory cell, comprising:

forming a first electrode over a substrate;

forming a memory body over said first electrode, said memory body comprising a germanium telluride glass layer and a tin selenide layer;

forming a chalcogenide glass layer over said memory body;

forming a silver-containing layer over said chalcogenide glass layer;

forming an adhesion layer over said silver-containing layer; and

forming a second electrode over said adhesion layer.

13. The method of claim 12, wherein said germanium telluride glass layer has a stoichiometric formula Ge_xTe_{100-x}, where x is about 44 to about 53.

14. The method of claim 12, wherein said germanium telluride glass layer has a stoichiometric formula Ge_xTe_{100-x}, where x is about 46 to about 51.

15. The method of claim 12, wherein said germanium telluride glass layer has a stoichiometric formula Ge_xTe_{100-x}, where x is about 47.

16. The method of claim 12, wherein said germanium telluride glass layer is in contact with said first electrode.

17. The method of claim 12, wherein the various layers of said memory cell are arranged vertically.

18. The method of claim 12, wherein said chalcogenide glass layer is Ge_2Se_3.

19. The method of claim 12, wherein said adhesion layer is Ge_2Se_3.

20. A method of forming a memory cell, comprising

providing a substrate;

forming a first tungsten electrode over said substrate;

forming a germanium telluride layer over said first tungsten electrode, wherein said germanium telluride layer has a stoichiometric formula Ge_xTe_{100-x}, x being between about 44 and about 53;

forming a tin selenide layer over said germanium telluride layer;

forming a first germanium selenide layer over said tin selenide layer;

forming a silver-containing layer over said first germanium selenide layer;

forming a second germanium selenide layer over said silver-containing layer;

forming a second tungsten electrode over said second germanium selenide layer; and

forming a conducting channel in said germanium telluride layer.

21. A memory device, comprising:

a first electrode;

a second electrode;

a memory element between said first and said second electrodes, said memory element comprising a germanium telluride layer and a metal-chalcogenide layer between said germanium telluride layer and said second electrode.

22. The memory device of claim 21, wherein said germanium telluride layer has a stoichiometric formula Ge_xTe_{100-x}, where x is about 44 to about 53.

23. The memory device of claim 21, wherein said germanium telluride layer has a stoichiometric formula Ge_xTe_{100-x}, where x is about 46 to about 51.

24. The memory device of claim 21, wherein said germanium telluride layer has a stoichiometric formula Ge_xTe_{100-x}, where x is about 47.

25. The memory device of claim 21, further comprising a conducting channel within said germanium telluride layer, said conducting channel comprising said metal-chalcogenide material.

26. The memory device of claim 25, further comprising a conductive pathway associated with said conducting channel, said conductive pathway being provided when said memory device is programmed to a first memory state.

27. The memory device of claim 21, wherein said metal-chalcogenide material comprises tin selenide.

28. The memory device of claim 21, further comprising a metal layer between said metal-chalcogenide layer and said second electrode.

29. The memory device of claim 28, further comprising a chalcogenide glass layer between said metal-chalcogenide layer and said metal layer.

30. The memory device of claim 29, further comprising a second chalcogenide glass layer between said metal layer and said second electrode.

31. The memory device of claim 21, wherein said memory device is part of a processor system.

32. A memory cell, comprising:

a first electrode over a substrate;

a germanium telluride layer over said first electrode;

a tin selenide layer over said germanium telluride layer;

a first germanium selenide layer over said tin selenide layer;

a silver-containing layer over said first germanium selenide layer;

a second germanium selenide layer over said silver-containing layer; and

a second electrode over said second germanium selenide layer.

33. The memory cell of claim 32, wherein said germanium telluride layer has a stoichiometric formula Ge_xTe_{100-x}, where x is about 44 to about 53.

34. The memory cell of claim 32, wherein said germanium telluride layer has a stoichiometric formula Ge_xTe_{100-x}, where x is about 46 to about 51.

35. The memory cell of claim 32, wherein said germanium telluride layer has a stoichiometric formula Ge_xTe_{100-x}, where x is about 47.

36. The memory cell of claim 32, further comprising a conducting channel within said germanium telluride layer, said conducting channel comprising said metal-chalcogenide material.

37. The memory cell of claim 36, further comprising a conductive pathway associated with said conducting channel, said conductive pathway being provided when said memory device is programmed to a first memory state.

38. The memory cell of claim 32, wherein said first and second germanium selenide layers comprise Ge_2Se_3.

39. The memory cell of claim 32, wherein said layers making up said cell are stacked vertically.

40. The memory cell of claim 32, wherein said layers making up said cell are in contact with one another.

41. A PCRAM memory cell, comprising:

a substrate;

a first tungsten electrode over said substrate;

a germanium telluride layer over said first tungsten electrode, wherein said germanium telluride layer has a stoichiometric formula Ge_xTe_{100-x}, x being between about 44 and about 53;

a tin selenide layer over said germanium telluride layer;

a first germanium selenide layer over said tin selenide layer;

a silver-containing layer over said first germanium selenide layer;

a second germanium selenide layer over said silver-containing layer;

a second tungsten electrode over said second germanium selenide layer; and

a conducting channel in said germanium telluride layer.

42. A processor system, comprising:

a processor and a memory device; wherein said memory device comprises:

a first electrode;

a second electrode;

a memory element between said first and said second electrodes, said memory element comprising a germanium telluride layer and a metal-chalcogenide layer between said germanium telluride layer and said second electrode.

43. The processor system of claim 42, wherein said germanium telluride layer has a stoichiometric formula Ge_xTe_{100-x}, where x is about 44 to about 53.

44. The processor system of claim 42, wherein said germanium telluride layer of said memory device has a stoichiometric formula Ge_xTe_{100-x}, where x is about 46 to about 51.

45. The processor system of claim 42, wherein said germanium telluride layer of said memory device has a stoichiometric formula Ge_xTe_{100-x}, where x is about 47.

46. The processor system of claim 42, further comprising a conducting channel within said germanium telluride layer of said memory device, said conducting channel comprising said metal-chalcogenide material.

47. The processor system of claim 42, further comprising a conductive pathway associated with said conducting channel, said conductive pathway being provided when said memory device is programmed to a first memory state.

48. The processor system of claim 42, wherein said metal-chalcogenide material of said memory device comprises tin selenide.

49. The processor system of claim 42, further comprising a metal layer between said metal-chalcogenide layer and said second electrode of said memory device.

50. The processor system of claim 49, further comprising a chalcogenide glass layer between said metal-chalcogenide layer and said metal layer of said memory device.

51. The processor system of claim 50, further comprising a second chalcogenide glass layer between said metal layer and said second electrode of said memory device.