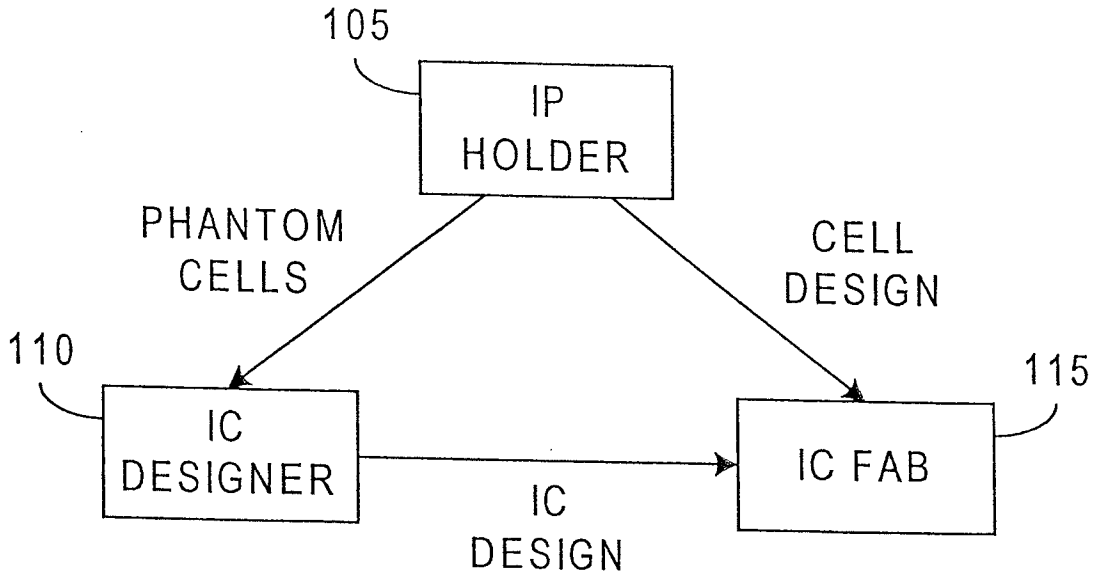


Figure 1

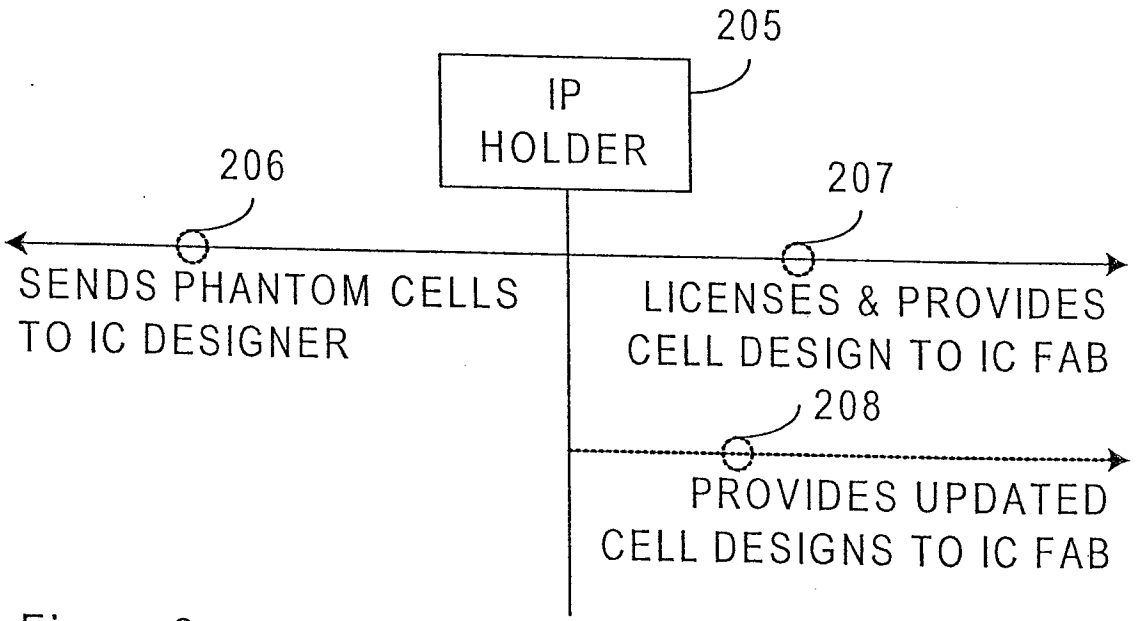


Figure 2a

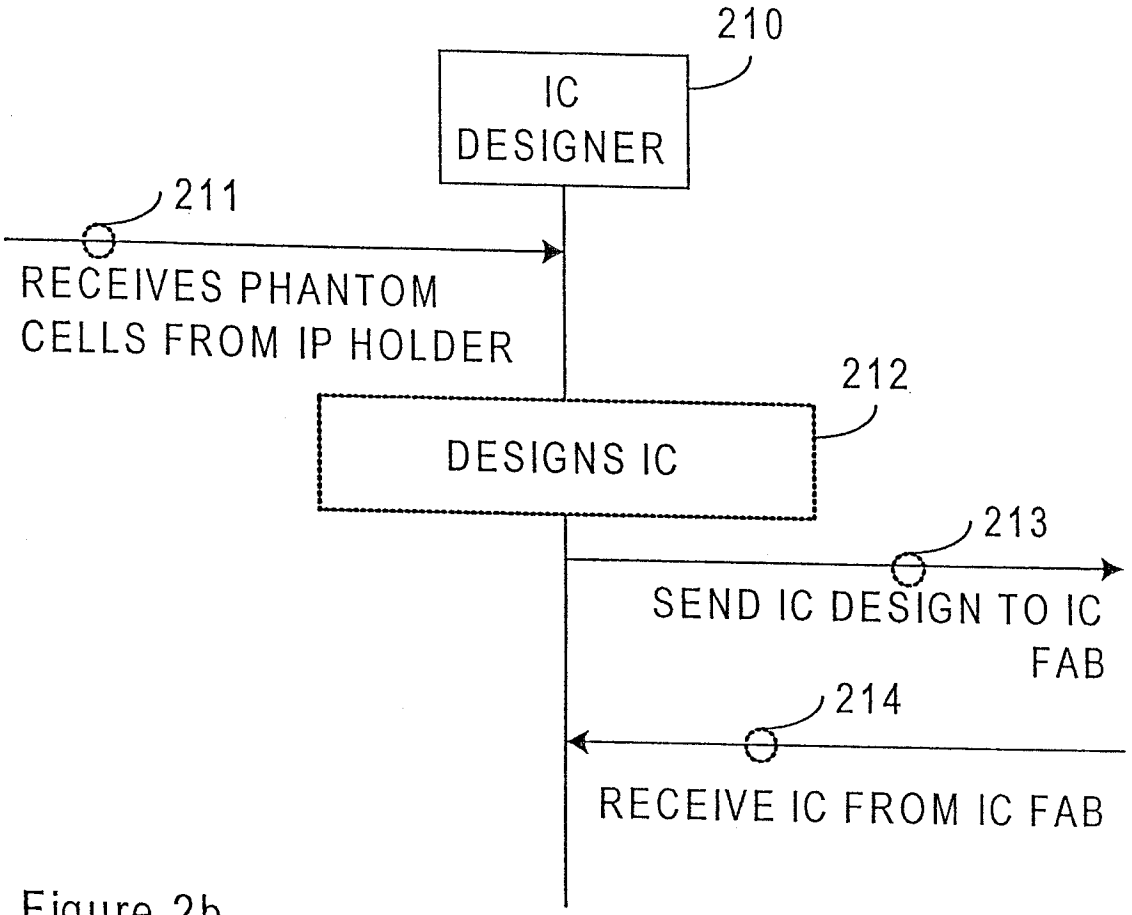

210
IC DESIGNER
211
RECEIVES PHANTOM CELLS FROM IP HOLDER
212
DESIGNS IC
213
SEND IC DESIGN TO IC FAB
214
RECEIVE IC FROM IC FAB

Figure 2b

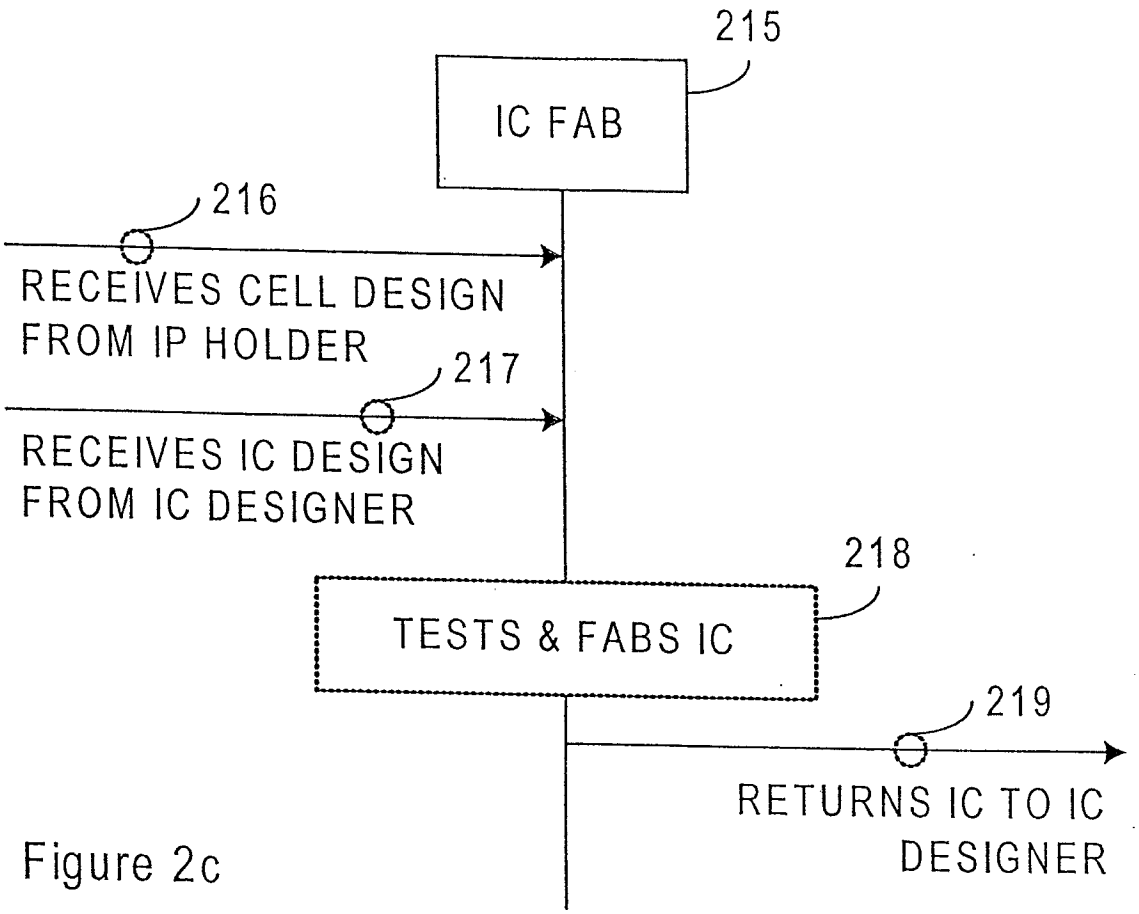


Figure 2c

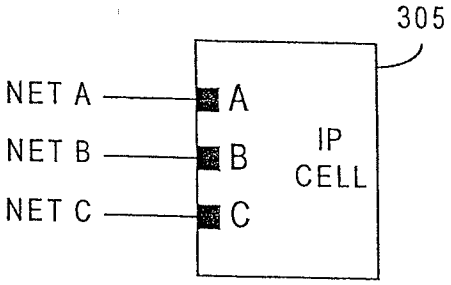


Figure 3a

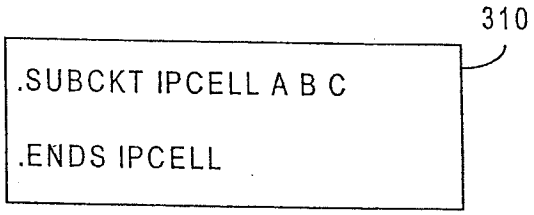


Figure 3b

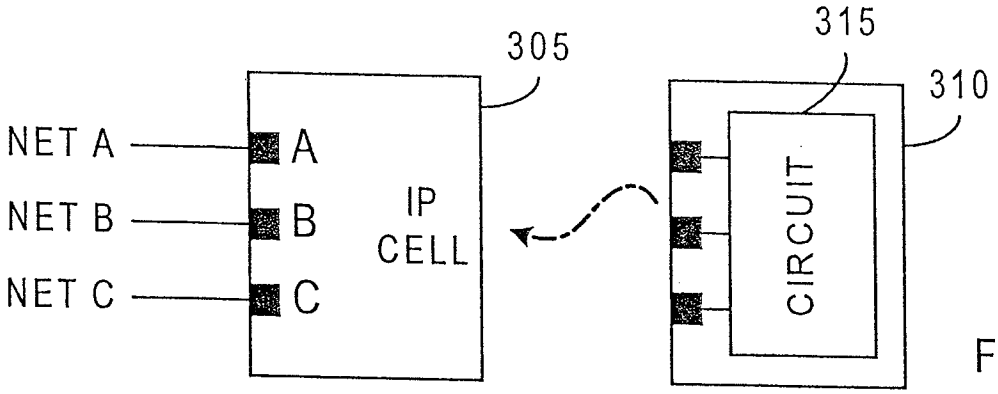


Figure 3c

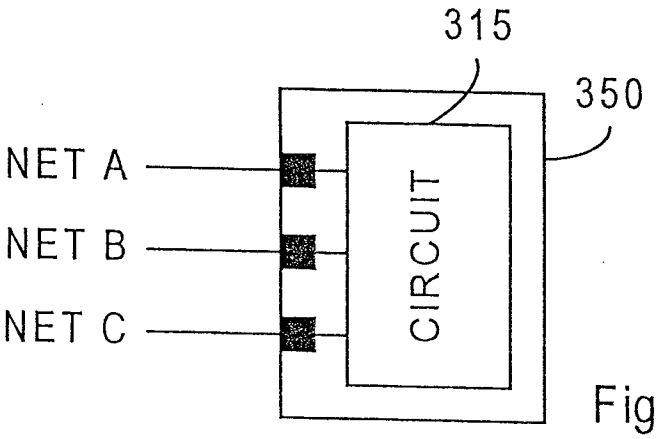


Figure 3d

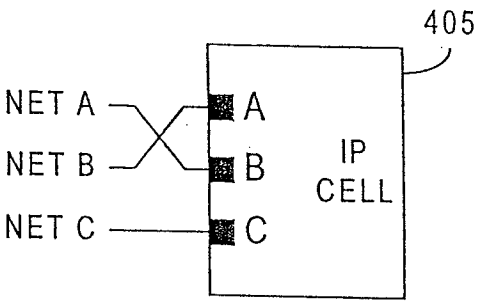


Figure 4

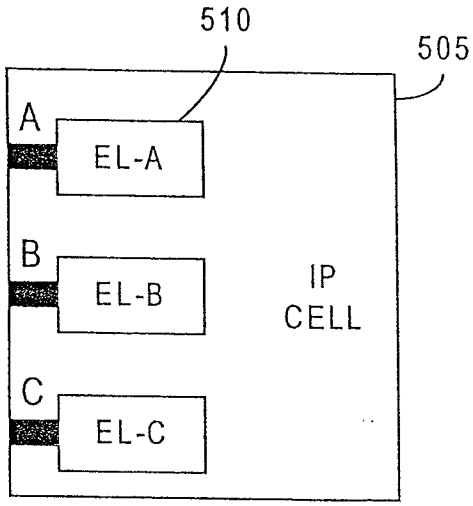


Figure 5

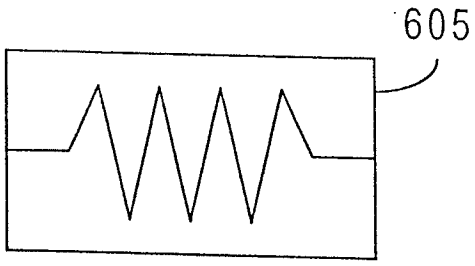


Figure 6a

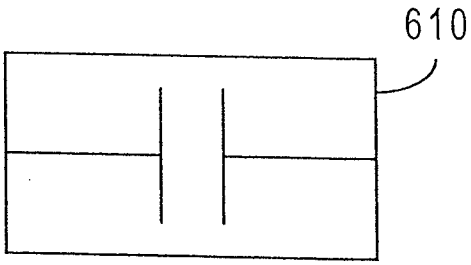


Figure 6b

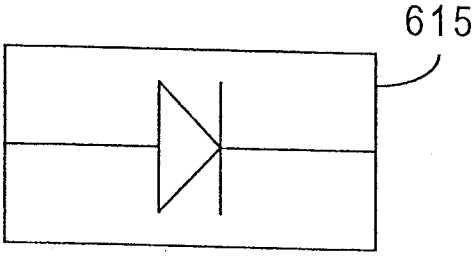


Figure 6c

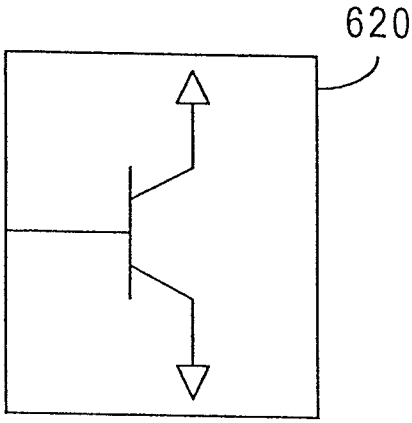


Figure 6d

```
.SUBCKT IPCELL A B C
RA A NODE1 5K
RB B NODE2 6K
RC C NODE3 7K


.ENDS IPCELL
```

705

Figure 7

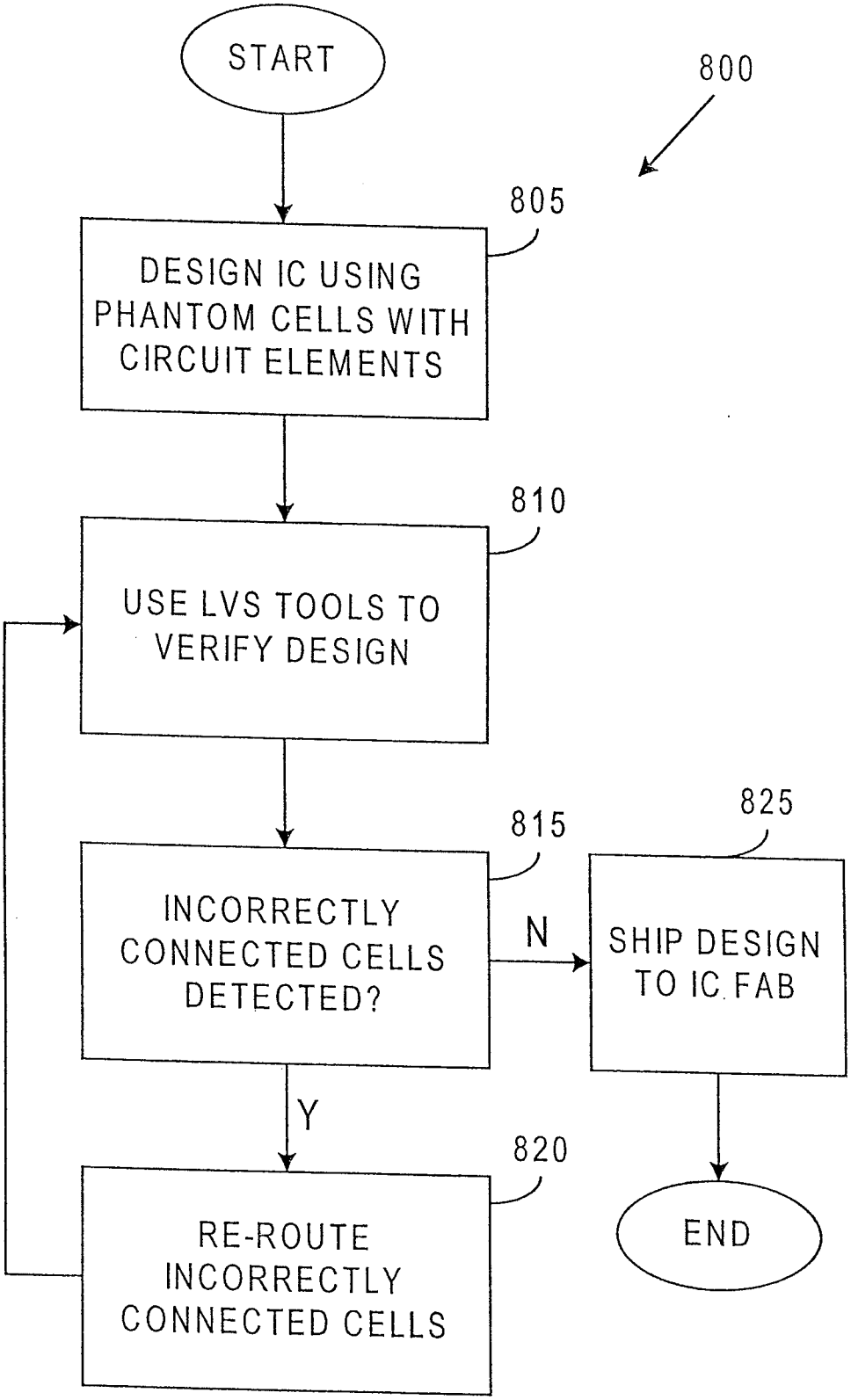

START
800
805
DESIGN IC USING PHANTOM CELLS WITH CIRCUIT ELEMENTS
810
USE LVS TOOLS TO VERIFY DESIGN
815
INCORRECTLY CONNECTED CELLS DETECTED?
N
825
SHIP DESIGN TO IC FAB
Y
820
RE-ROUTE INCORRECTLY CONNECTED CELLS
END

Figure 8