FIG. 1

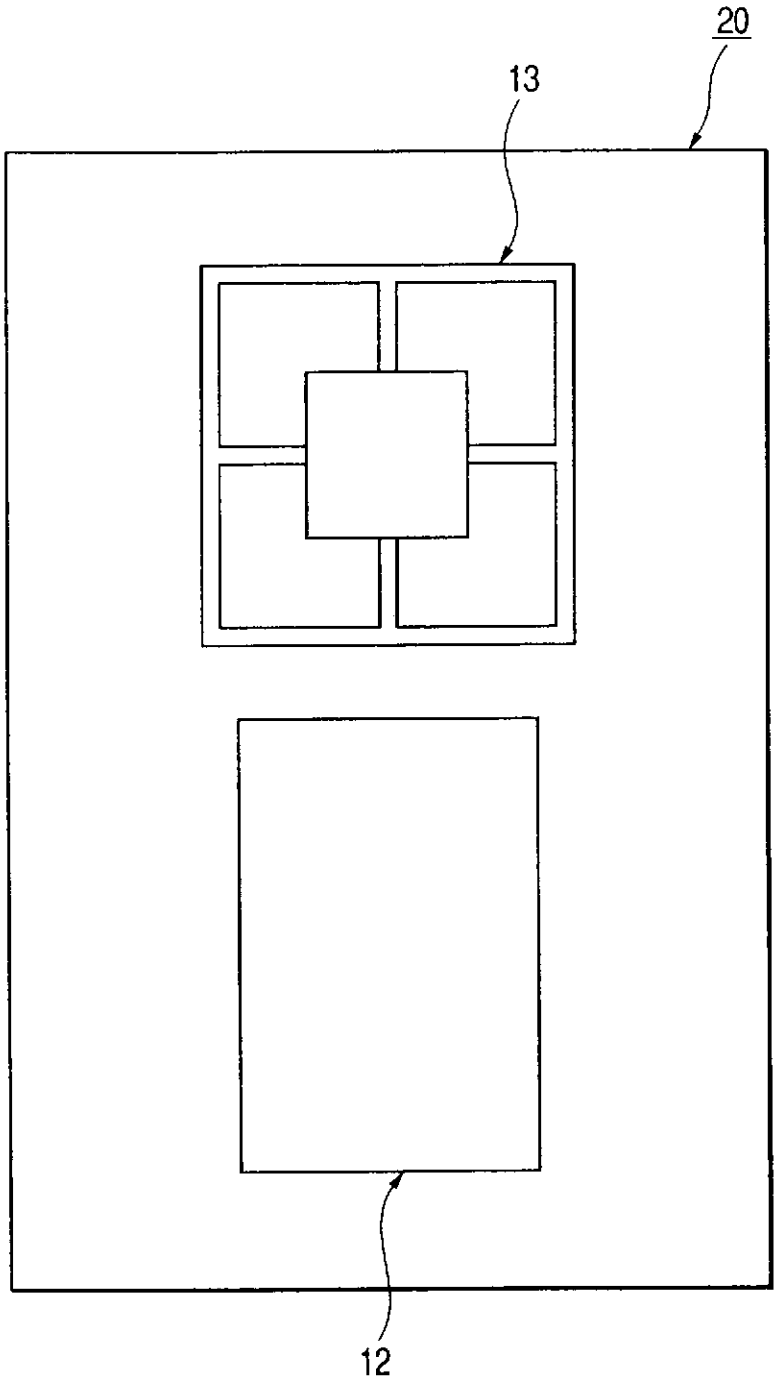


FIG. 2

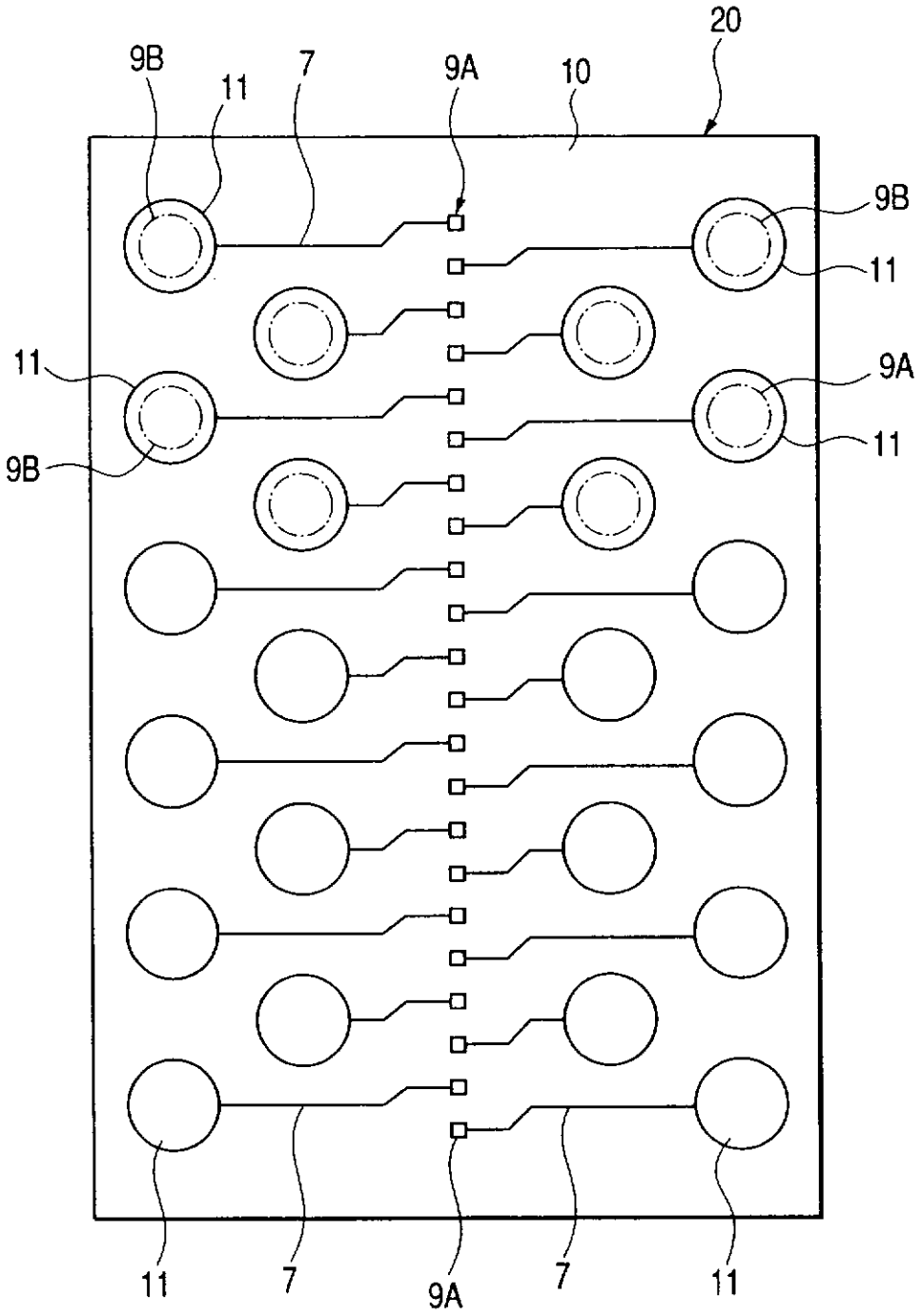


FIG. 3

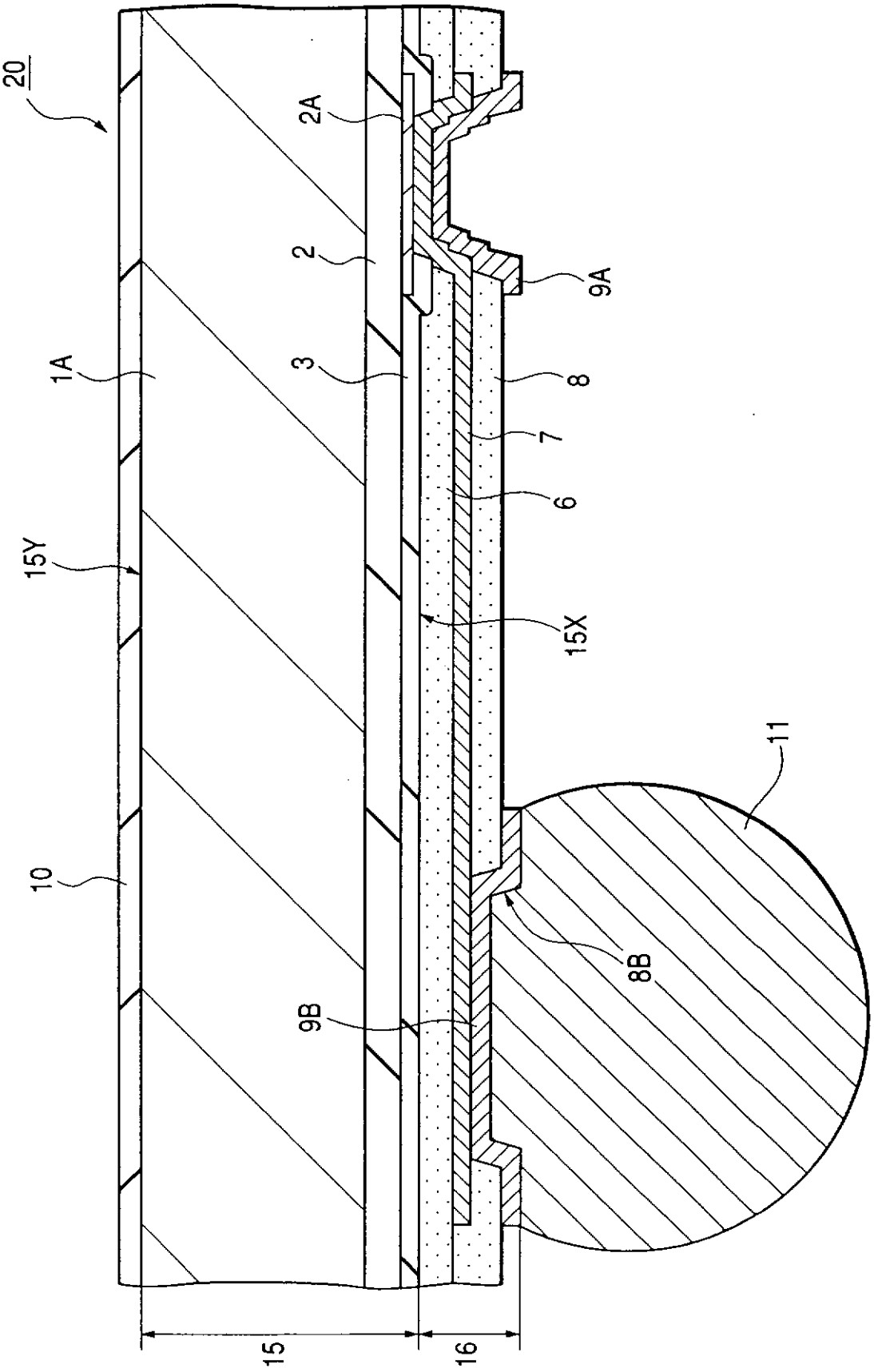


FIG. 4

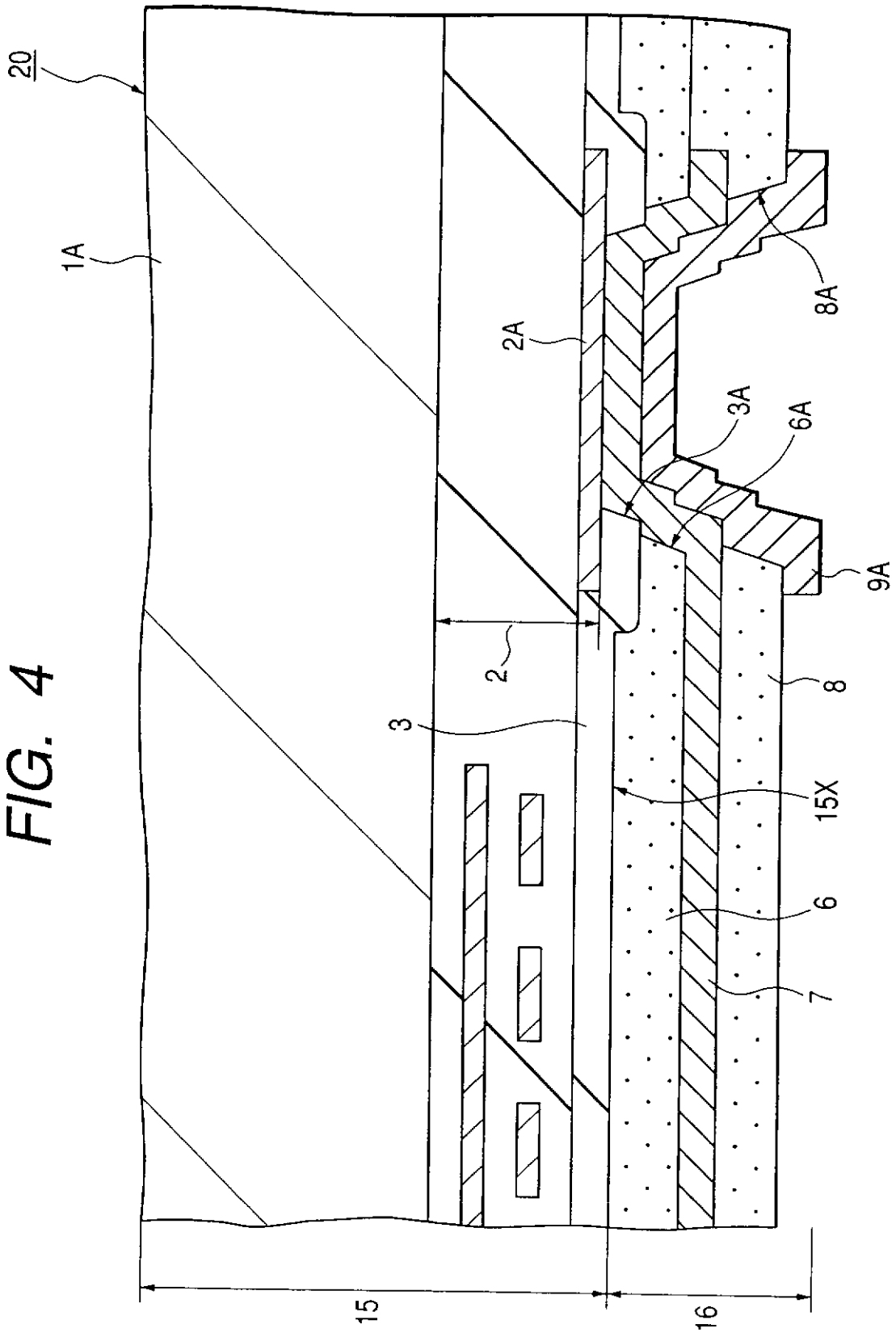


FIG. 5

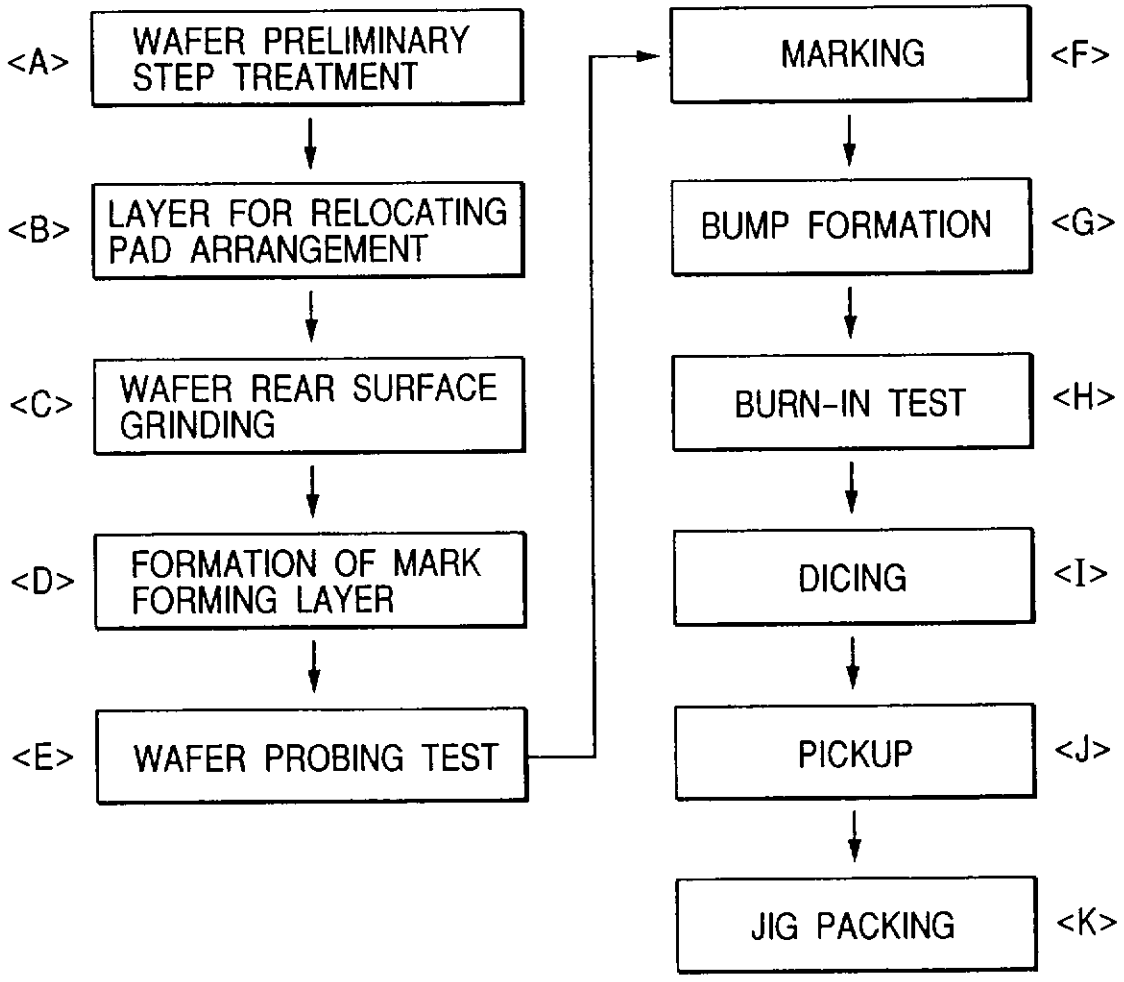

<A>
WAFER PRELIMINARY STEP TREATMENT
<B>
LAYER FOR RELOCATING PAD ARRANGEMENT
<C>
WAFER REAR SURFACE GRINDING
<D>
FORMATION OF MARK FORMING LAYER
<E>
WAFER PROBING TEST
MARKING
<F>
BUMP FORMATION
<G>
BURN-IN TEST
<H>
DICING
<I>
PICKUP
<J>
JIG PACKING
<K>

FIG. 6

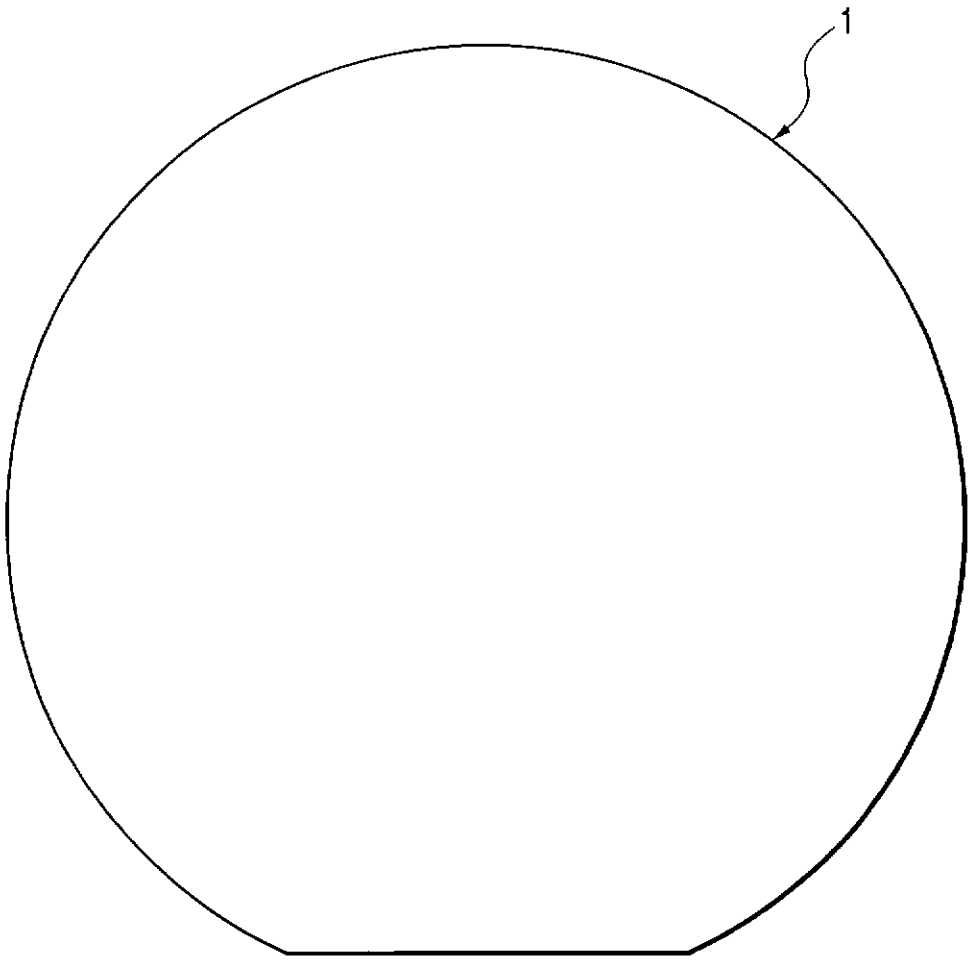


FIG. 7

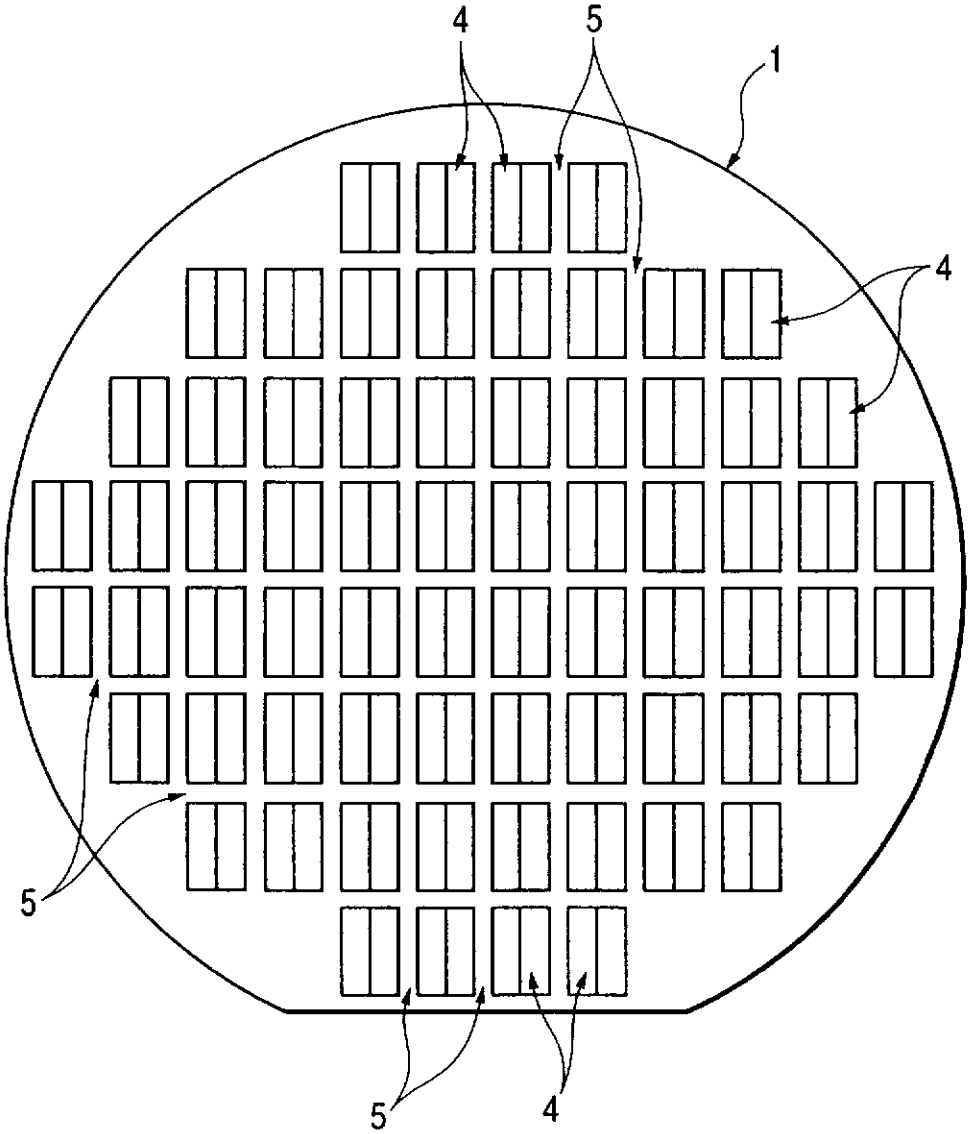


FIG. 8

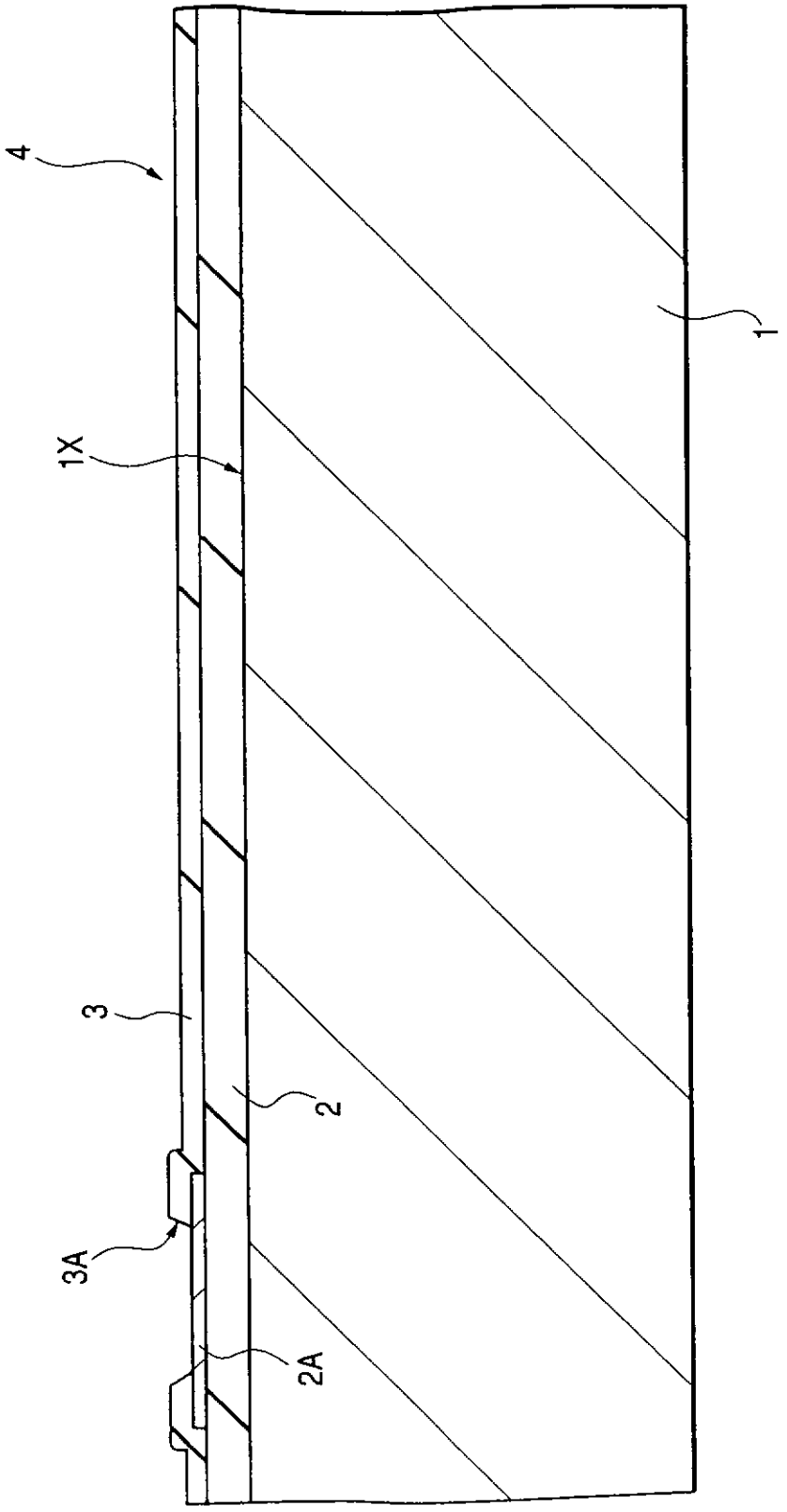


FIG. 9

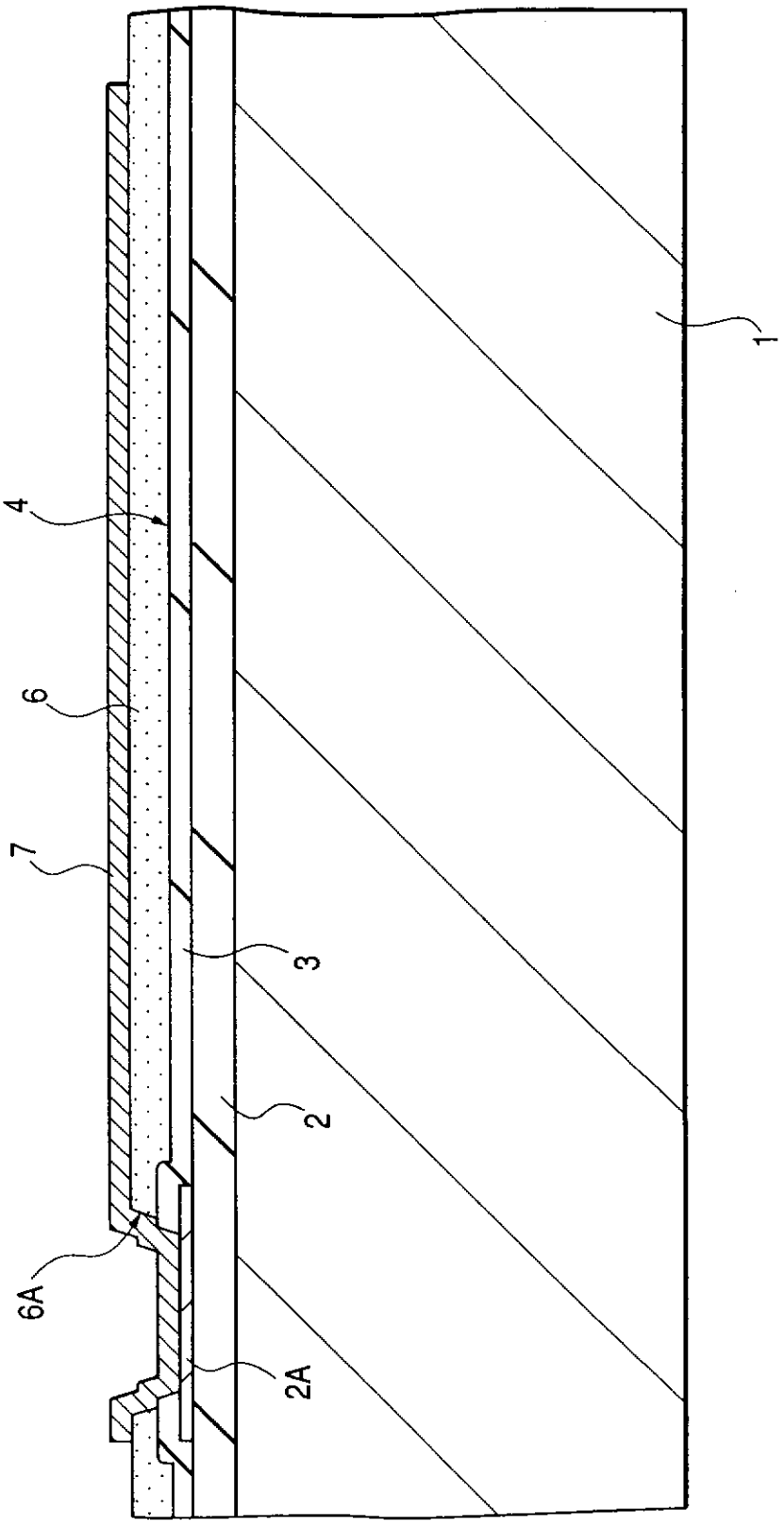


FIG. 10

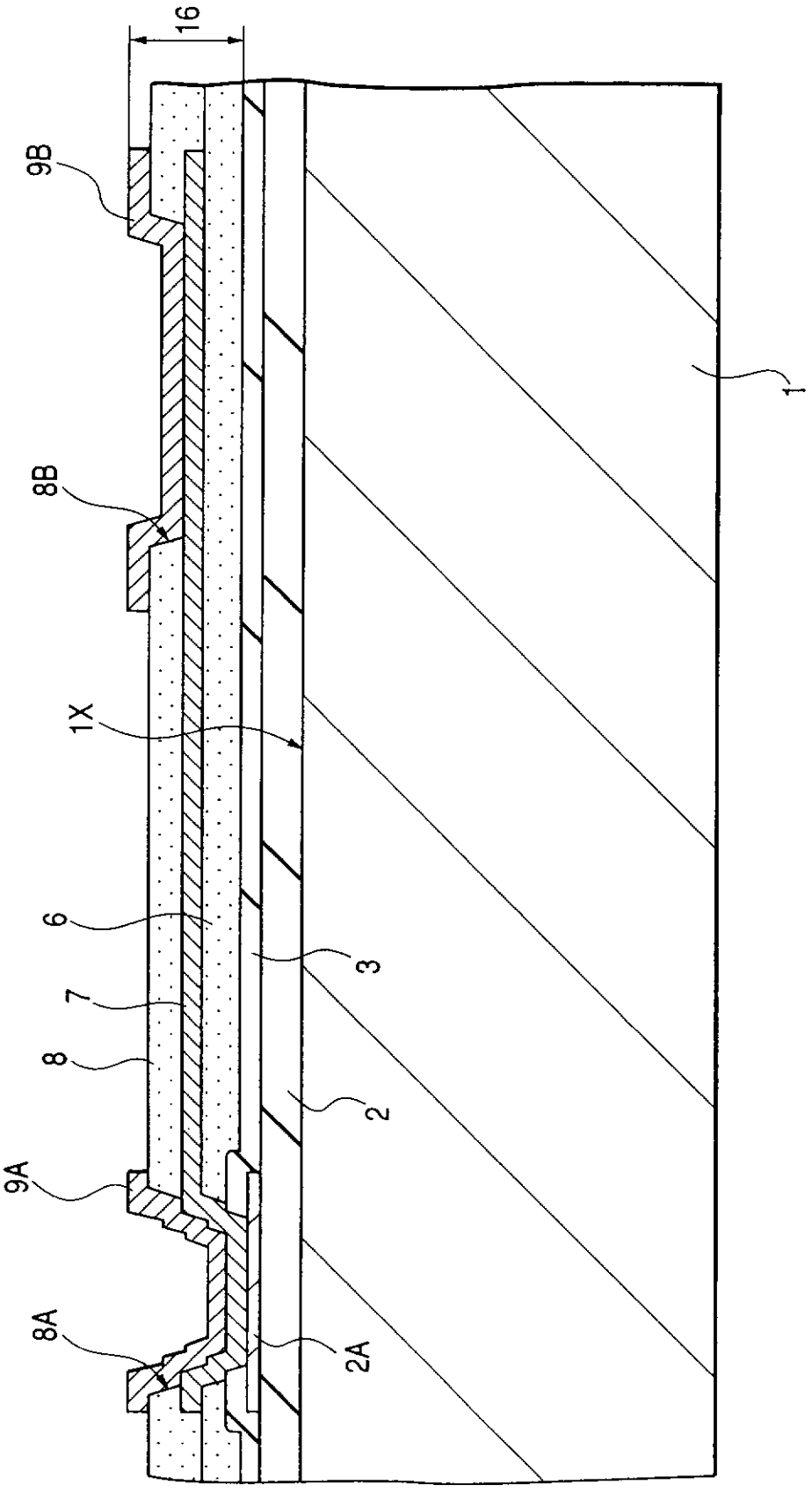


FIG. 11

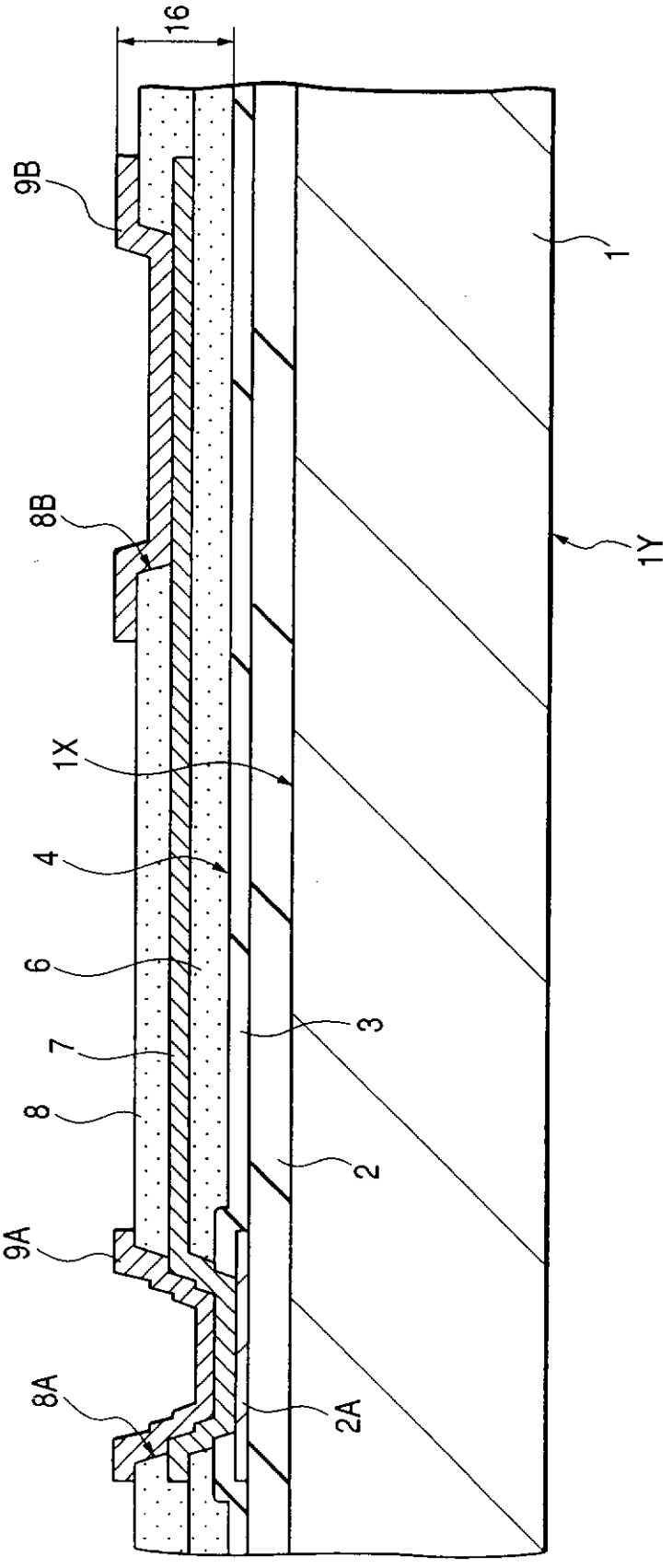


FIG. 12

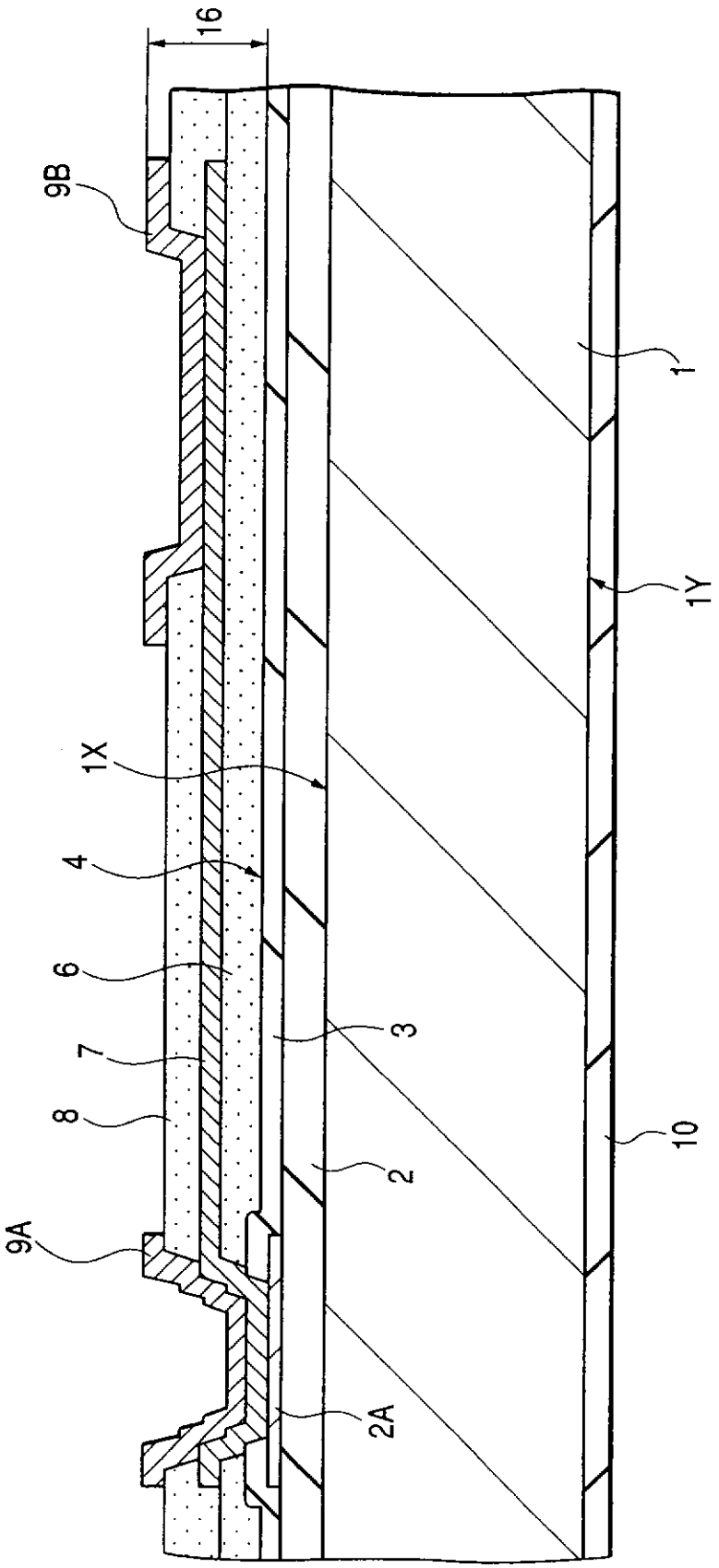


FIG. 13

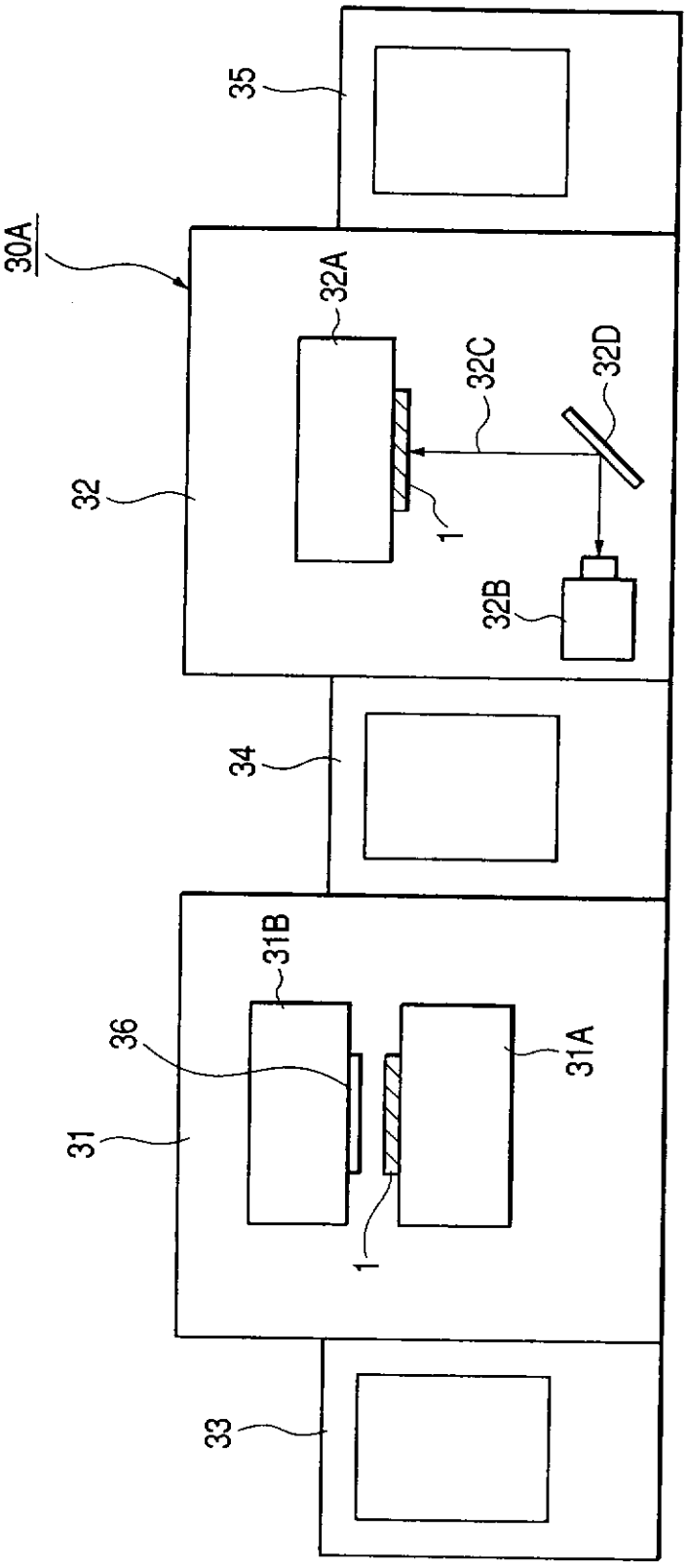


FIG. 14

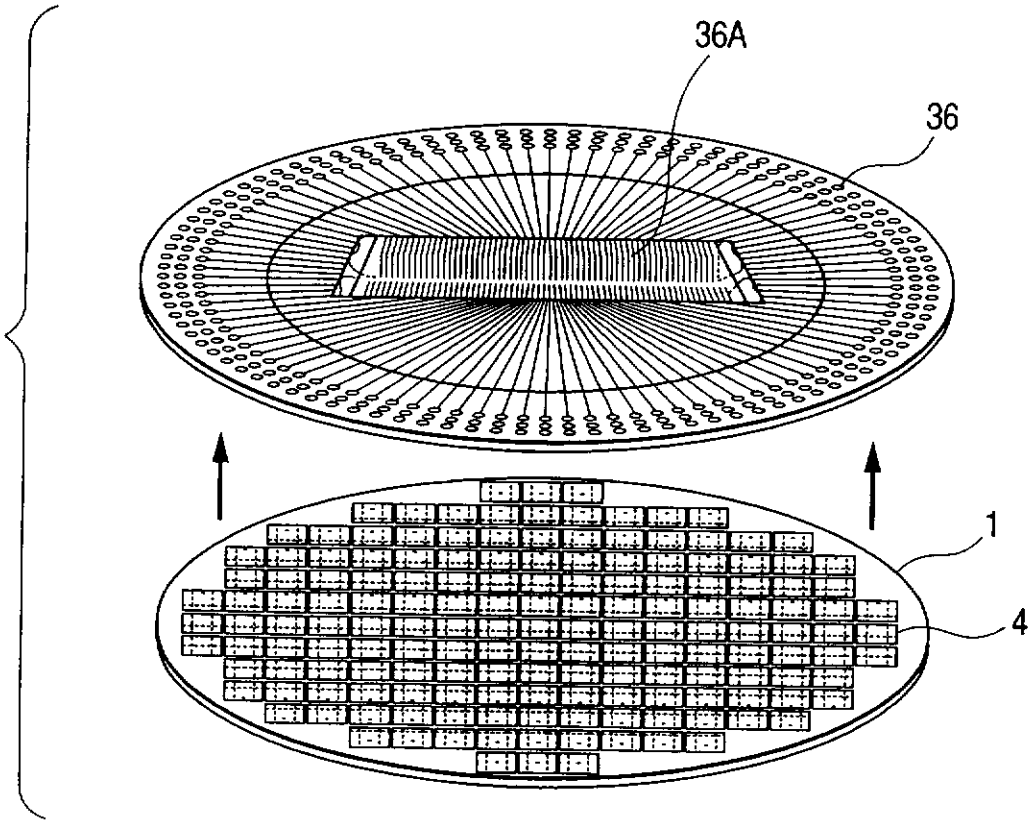


FIG. 15

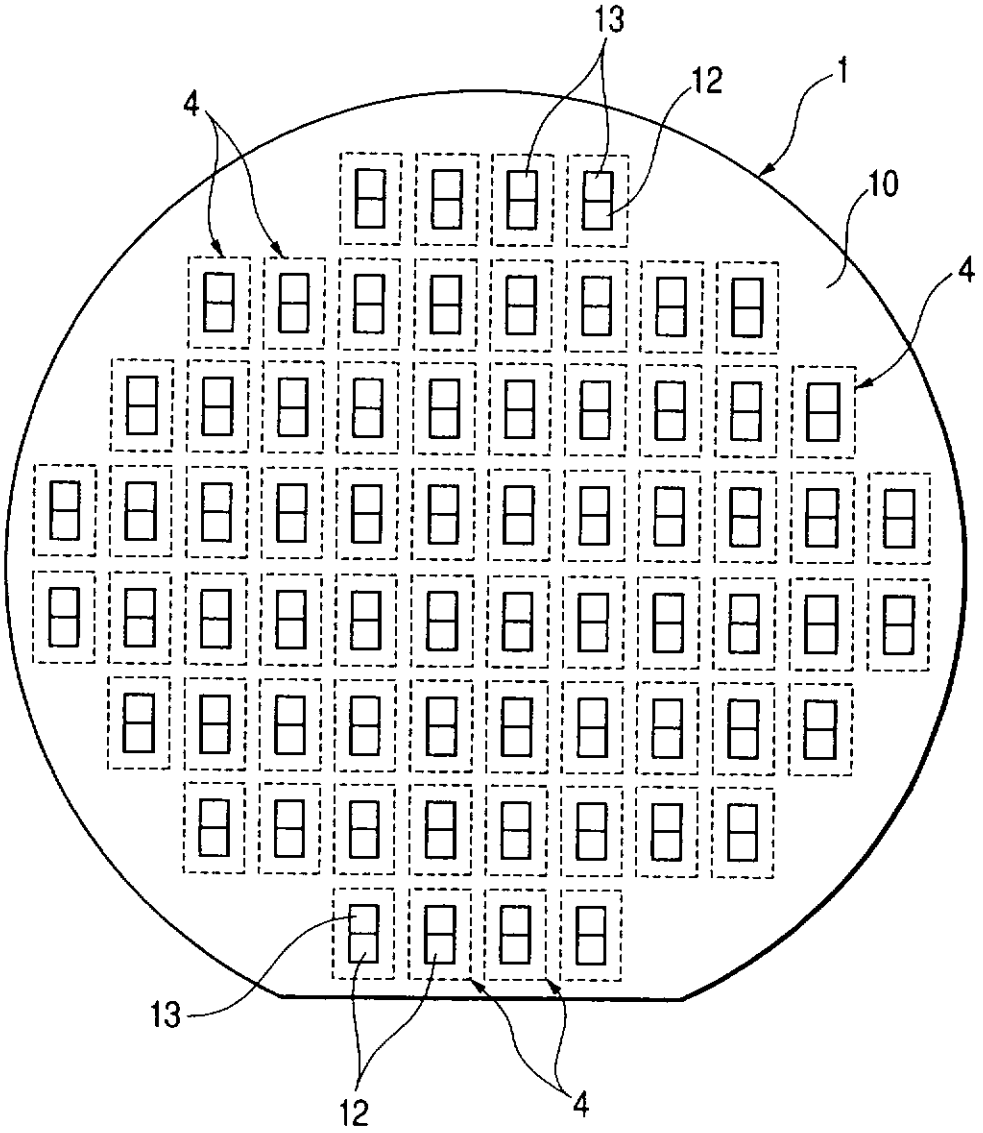


FIG. 16

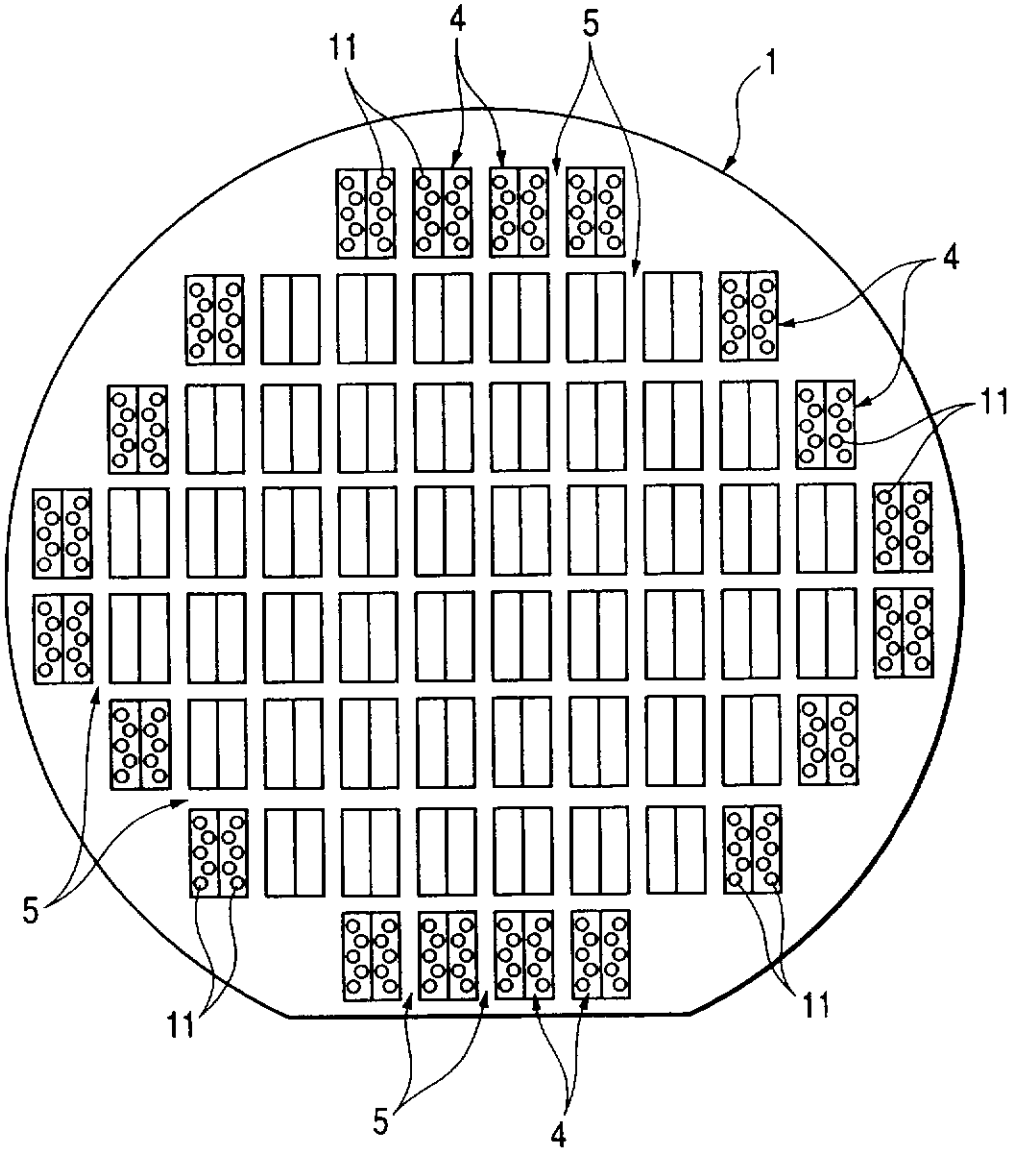


FIG. 17

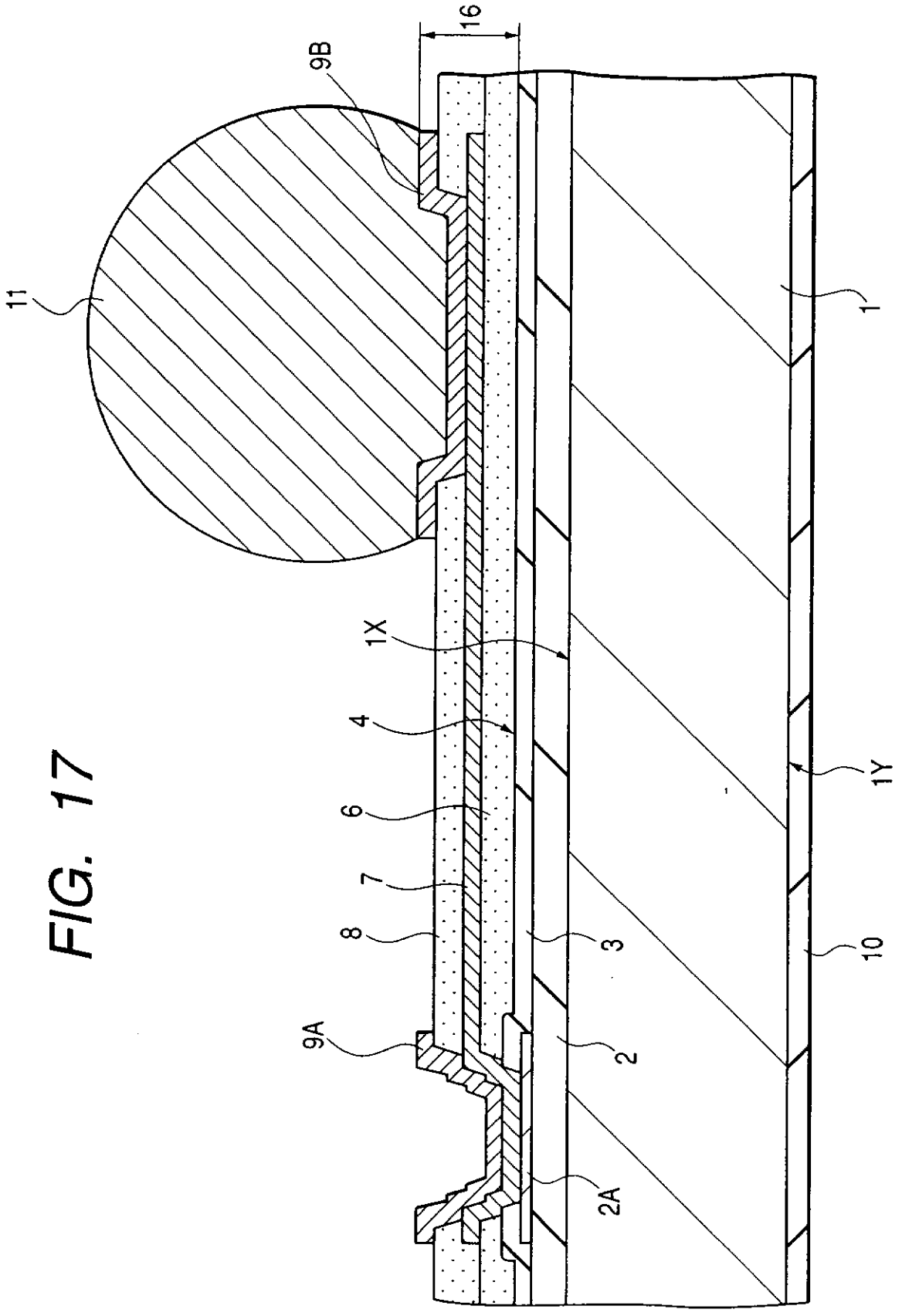


FIG. 18

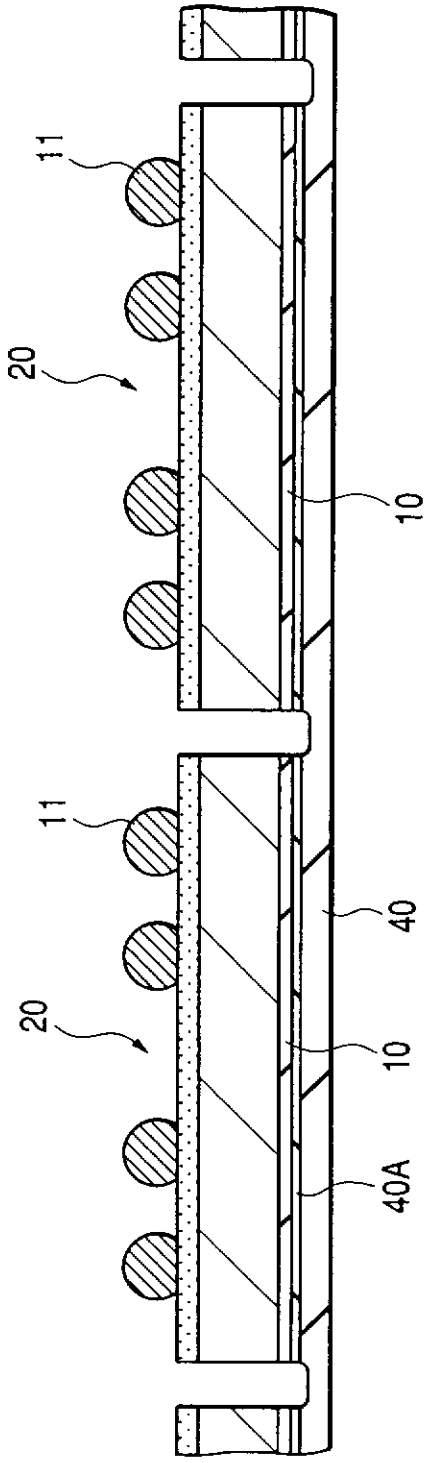


FIG. 20

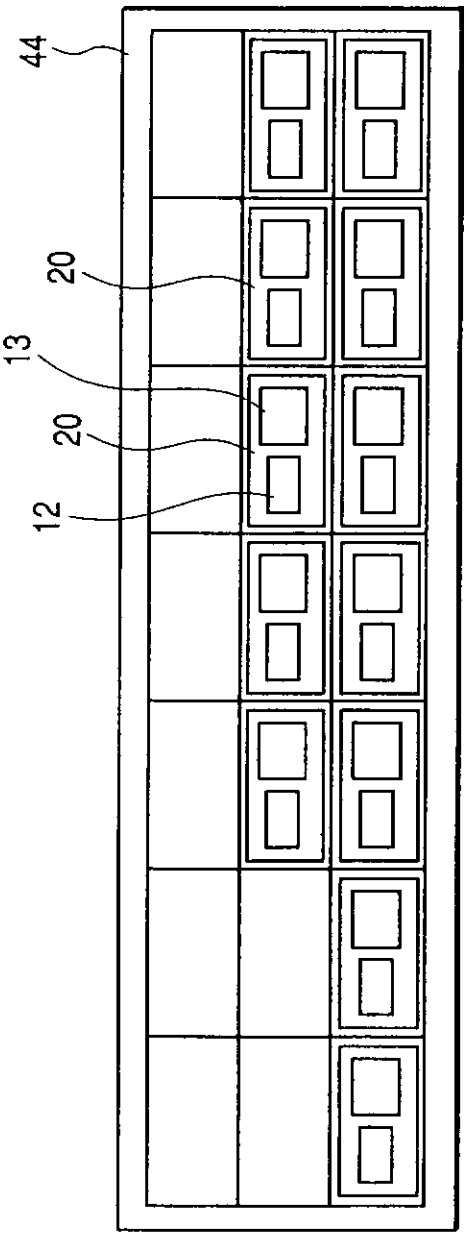


FIG. 19

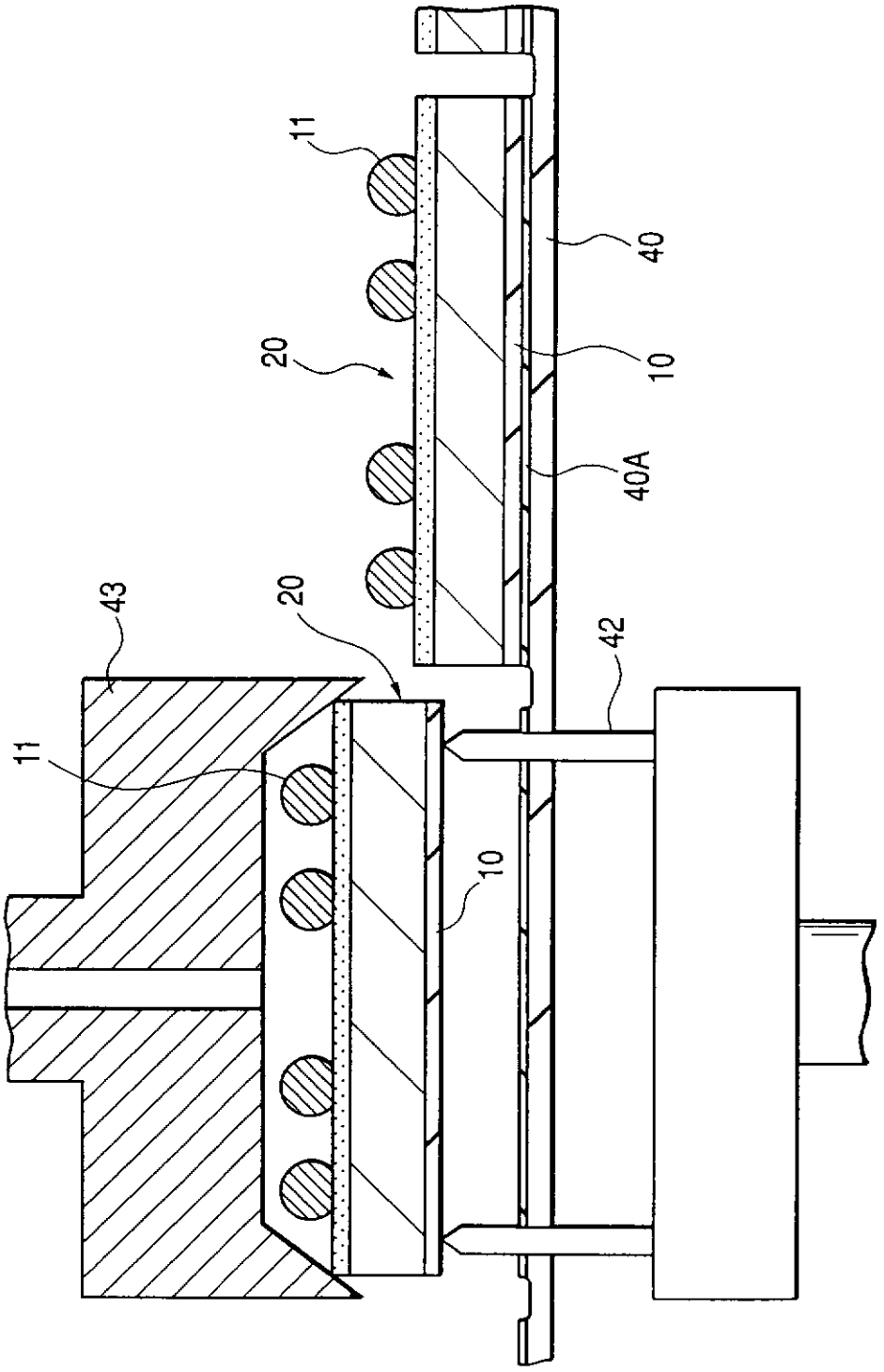


FIG. 21

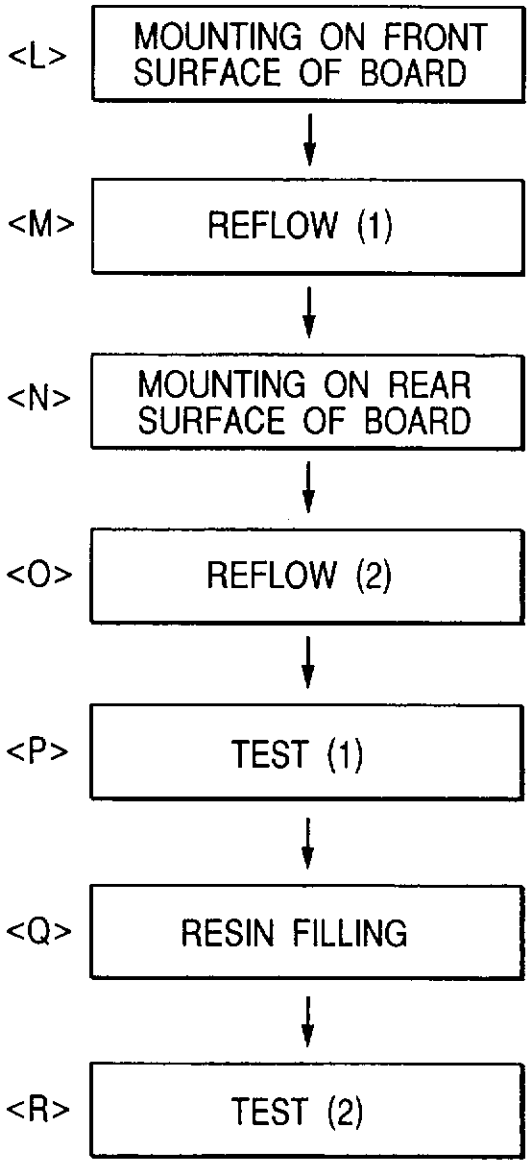

<L>
MOUNTING ON FRONT SURFACE OF BOARD
<M>
REFLOW (1)
<N>
MOUNTING ON REAR SURFACE OF BOARD
<O>
REFLOW (2)
<P>
TEST (1)
<Q>
RESIN FILLING
<R>
TEST (2)

FIG. 22

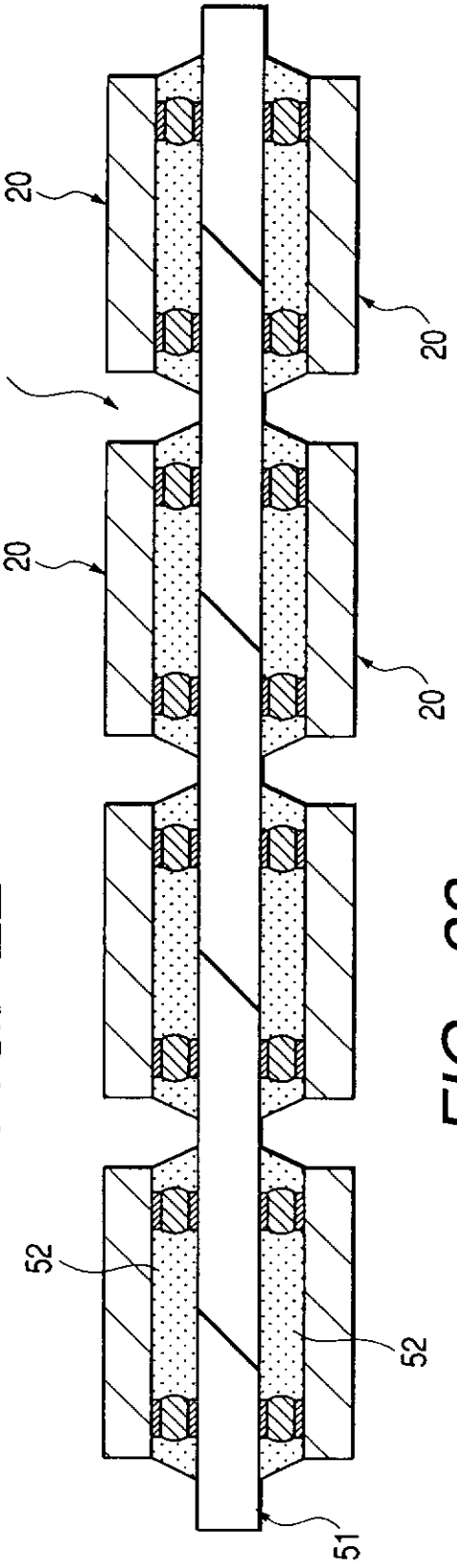
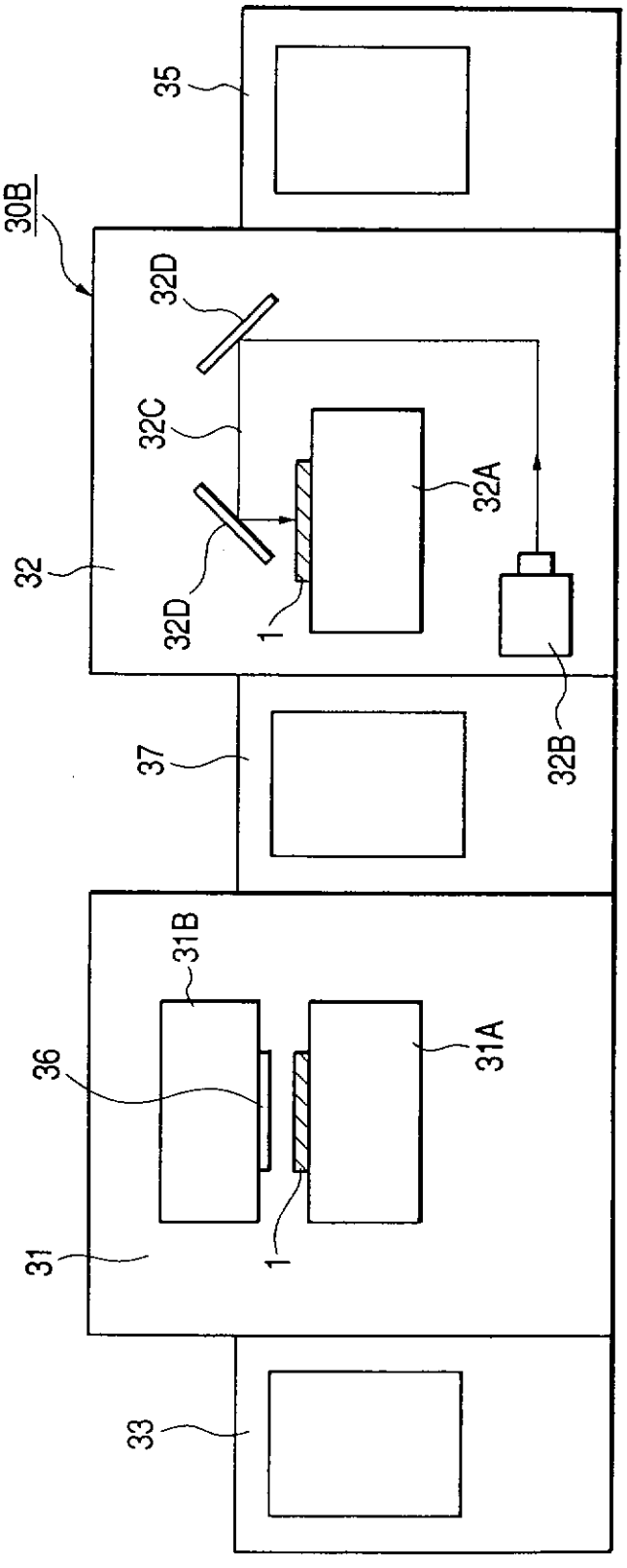

20
20
50
20
20
52
52
51

FIG. 23


35
30B
32D
32C
32A
32
32D
1
32B
37
31B
36
31A
31
1
33