SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES AND METHOD OF MANUFACTURING THE SAME

The present invention relates to a semiconductor integrated circuit device having a complementary insulated gate field effect transistor circuit and an integrated injection logic circuit on the same semiconductor substrate, and to a method of manufacturing the same.

Semiconductor integrated circuit devices (hereinafter referred to as CMISFET-I^2L ICs) having a complementary insulated gate field effect transistor circuit (hereinafter referred to as a CMISFET) and an integrated injection logic circuit (hereinafter referred to as an I^2L) on the same semiconductor substrate, have heretofore been known. For instance, a CMISFET-I^2L IC has been disclosed in United States Patent No. 4122481 or in Japanese Patent Laid-Open No. 52482/1979. As is seen in these publications, a CMISFET-I^2L IC is manufactured through a complicated process. Therefore, it has been attempted to form semiconductor regions which constitute a CMISFET circuit and semiconductor regions which constitute an I^2L circuit using the same steps as far as possible. For example, according to Japanese Patent Laid-Open No. 52482/1979, the well region for an I^2L and the well region for an N-channel MOSFET can be formed simultaneously.

In a CMISFET-I^2L IC obtained through the above-mentioned method, however, the electrical characteristics

of either the CMISFET or the I^2L must be sacrificed.

According to a study conducted by the inventors of the present invention, in order to improve the electrical characteristics without reducing the degree of integration, it was confirmed that the impurity concentration plays a very important role in the emitter region of the inverse transistors that operate as driver transistors in the I^2L, and in the semiconductor region (well region) where channels are formed in the CMISFET among the plurality of semiconductor regions that constitute the integrated circuit. These inverse transistors each have a collector region, a base region and an emitter region that are formed in the semiconductor substrate in that order from the main surface toward the inside of the substrate. Thus the inverse transistor is constructed in the opposite way to an ordinary transistor, which is why it is so called.

When forming the emitter and well regions simultaneously, if the impurity concentration is increased in order to increase the current amplification factor βi of the inverse transistors in an I^2L, the operating frequency of the CMISFET decreases. That is, if the impurity concentration in the well region is high, the depletion layer spreads less easily. Therefore, the junction capacity increases so that the switching operations of the CMISFET are no longer capable of following high-frequency signals. To increase the operating frequency, the gate width of the MISFETs must be increased to increase the

current capacity. Therefore, the MISFETs occupy an increased area, and the degree of integration decreases. On the other hand, if the impurity concentrations in these regions are made small in order to improve the operating frequency of the CMISFET, the current amplification factor βi becomes small, the operating speed of the I^2L decreases, and the power consumption increases.

In Japanese Patent Laid-Open No. 52482/1979, furthermore, the source and drain regions of the MISFETs are formed prior to the formation of the gate electrodes, and are not self-aligned relative to the gate electrodes. Similarly, the well region in the I^2L and the semiconductor region formed in the well region are not self-aligned, either. Therefore, a sufficient masking margin must be provided. Accordingly, it becomes difficult to obtain CMISFET-I^2L ICs in a highly integrated form.

Furthermore, United States Patent No. 4122481 or Japanese Patent Laid-Open No. 52482/1979 do not consider the relationship of the connection between the CMISFET circuit and the I^2L circuit.

In a first aspect the present invention therefore provides a semiconductor integrated circuit device comprising an epitaxial semiconductor layer having a first conductivity type formed on a semiconductor substrate, first and second semiconductor well regions having a second conductivity type opposite to said first conductivity type that are formed in the epitaxial semiconductor layer

separated from each other, a plurality of third semiconductor regions which constitute the elements of an I^2L circuit that is formed in the first semiconductor region, and a plurality of fourth semiconductor regions which constitute the elements of a MISFET circuit that is formed in the second semiconductor region, wherein the first semiconductor region has an impurity concentration that is greater than that of the second semiconductor region.

Embodiments of the invention will now be described by way of example, with reference to the accompanying drawings in which:

Fig. 1 is a sectional view of an integrated circuit according to the first embodiment of the present invention;

Figs. 2A to 2H are sectional views of steps in the process for producing the integrated circuit of Fig. 1;

Fig. 3 is a circuit diagram which schematically illustrates the first embodiment;

Fig. 4 is a plan view which schematically shows the layout of the connection between circuit I and circuit II of Fig. 3;

Fig. 5 is a plan view of the load transistor;

Fig. 6 is a circuit diagram showing the second embodiment of the present invention;

Fig. 7 is a circuit diagram showing the third embodiment;

Fig. 8 is a sectional view of an integrated circuit according to the fourth embodiment of the present invention; and

Fig. 9 is a circuit diagram which schematically illustrates the fourth embodiment.

Reference will first be made to Figs. 1 to 5, which illustrate a first embodiment of the present invention.

Fig. 1 is a diagram showing the construction of a CMISFET-I^2L IC according to the present invention, in which the region X_1 shows the construction of the complementary MISFETs, and the region X_2 shows the construction of the I^2L elements.

As shown in Fig. 1, unlike conventional devices, the integrated circuit of this embodiment is prepared by growing a p-type epitaxial layer 2 of a low impurity concentration on a p-type silicon substrate 1 of a low impurity concentration. Reference number 16 denotes an n^+-type buried layer formed under the well region that will form the I^2L circuit, 3 denotes a first n-type well region of a low concentration formed in the p-type epitaxial layer 2, and 4 denotes a second n-type well region having an impurity concentration smaller than that of the first n-type well region 3. An I^2L consists of a

p-type injector region 5, a p-type base region 6 of an npn inverse transistor, an n^+-type collector region 7 of the npn inverse transistor and an n^+-type emitter contact region 8 formed in the first n-type well region 3. The n-type well region 3 forms an emitter region for the npn inverse transistor. A p-channel MISFET consists of p^+-type source and drain regions 9 formed in the second n-type well region 4, a gate insulation film 11, and a polycrystalline silicon layer 14 that serves as a gate electrode. An n-channel MISFET consists of n^+-type source and drain regions 10 formed in the p^--type layer where no well region is formed, a gate insulation film 12, and a polycrystalline silicon layer 15 that serves as a gate electrode.

Figs. 2A to 2H are diagrams illustrating the process for producing the integrated circuit of Fig. 1. Complementary MISFETs are formed in the area X_1, and I^2L elements are formed in the area X_2.

Referring to Fig. 2A, first, n-type impurities such as arsenic impurities are selectively introduced into a predetermined portion of a p-type silicon substrate 1 by diffusion techniques or ion implantation techniques, and p-type doped silicon is deposited on the substrate by epitaxial growth to form a p^--type epitaxial layer 2 (impurity concentration N: 10^{15} atoms/cm^3). At the same time, an n^+-type buried layer 16 is also formed owing to the diffusion of the n-type impurities.

As shown in Fig. 2B, an n-type well region 4 is

p-type injector region 5, a p-type base region 6 of an npn inverse transistor, an n^+-type collector region 7 of the npn inverse transistor and an n^+-type emitter contact region 8 formed in the first n-type well region 3. The n-type well region 3 forms an emitter region for the npn inverse transistor. A p-channel MISFET consists of p^+-type source and drain regions 9 formed in the second n-type well region 4, a gate insulation film 11, and a polycrystalline silicon layer 14 that serves as a gate electrode. An n-channel MISFET consists of n^+-type source and drain regions 10 formed in the p^--type layer where no well region is formed, a gate insulation film 12, and a polycrystalline silicon layer 15 that serves as a gate electrode.

Figs. 2A to 2H are diagrams illustrating the process for producing the integrated circuit of Fig. 1. Complementary MISFETs are formed in the area X_1, and I^2L elements are formed in the area X_2.

Referring to Fig. 2A, first, n-type impurities such as arsenic impurities are selectively introduced into a predetermined portion of a p-type silicon substrate 1 by diffusion techniques or ion implantation techniques, and p-type doped silicon is deposited on the substrate by epitaxial growth to form a p^--type layer 2 (impurity concentration N: 10^{15} atoms/cm^3). At the same time, an n^+-type buried layer 16 is also formed owing to the diffusion of the n-type impurities.

As shown in Fig. 2B, an n-type well region 4 is

selectively formed in the p^--type layer 2 in order to form p-channel MISFETs. In order to selectively form the n-type well region 4, an oxide film 30 of a thickness of 500 angstroms is first formed by thermal oxidation on the whole surface of the p-type epitaxial layer 2, and an Si_3N_4 film 31 of a thickness of 1500 angstroms is formed thereon by the chemical vapor deposition method (hereinafter referred to as the CVD method). Then the oxide film 30 on that portion where the n-type well region is to be formed and the Si_3N_4 film 31, are selectively removed by plasma etching using a photoresist film (not shown) as a mask, such that the surface of the p-type epitaxial layer 2 is exposed. Masks for forming all the n-type well regions are completed in this step so that all the positions of all the well regions are determined by the masks. Thereafter, the windows for forming the n-type well regions that form the low-concentration I^2L are covered with a suitable mask such as a thick photoresist film 32 as shown in Fig. 2B, and n-type impurities such as phosphorus ions are implanted (N: 10^{16} atoms/cm^3) to form the n^--type well region 4 which has a low impurity concentration. Although the impurity concentration is low, the well region 4 should preferably be formed by the ion implantation method since it is possible to control the concentration precisely.

Then, the low-concentration n-type well region 3 is formed as shown in Fig. 2C. After the photoresist film 32 is removed, the n-type well region 4 is covered with a

thick photoresist film 33, and n-type impurities such as phosphorus ions are implanted (N: 10^7 atoms/cm^3) to form the low-concentration n-type well region 3. The well region 3 should preferably be formed by the ion implantation technique since it is possible to control the impurity concentration precisely as mentioned above.

A field oxide film is then formed as shown in Fig. 2D. After the photoresist film 33, the Si_3N_4 film 31 and the SiO_2 film 30 are removed in succession, an oxide film (SiO_2 film) 34 of a thickness of 500 angstroms is formed by thermal oxidation on the exposed surfaces of the epitaxial layer 2, and then an Si_3N_4 film 35 of a thickness of 1500 angstroms is formed by the CVD method. The Si_3N_4 film 35 is then selectively removed by plasma etching using a photoresist film (not shown) as a mask, so that the SiO_2 film 34 is partially exposed. To prevent the formation of an inversion layer under the field oxide film under this condition, p-type impurities such as boron ions are implanted while the photoresist film is still in place. The photoresist film is then removed, and a field oxide film (SiO_2 film) 17 is formed by thermal oxidation to a thickness of 9000 angstroms using the Si_3N_4 film 35, which is not permeable to oxygen, as a mask.

Then, as shown in Fig. 2E, the gate insulation films and the gate electrodes of the MISFETs are formed. After the SiO_2 film 34 and the Si_3N_4 film 35 are removed, a gate insulation film (SiO_2 film) is formed to a thickness of 500

angstroms by thermal oxidation on the whole surface of the exposed epitaxial layer 2. A polycrystalline silicon layer is then formed to a thickness of 3500 angstroms on the whole surface of the substrate by the CVD method. Phosphorus impurities are introduced into the polycrystalline silicon layer by diffusion to decrease its sheet resistance to such a level that it can be used as gate electrodes. To complete the gate electrodes, the polycrystalline silicon layer and the gate insulation film are selectively removed by plasma etching using a photoresist film as a mask. The gate insulation films 11,12 and the gate electrodes 14,15 of the MISFETs are thus completed. At the same time, the surface of the epitaxial layer 2 on the I^2L side is exposed.

Next, a p-type semiconductor region is formed as shown in Fig. 2F. First, to prevent the exposed epitaxial layer 2 from being contaminated, an SiO_2 film 25 is formed to a thickness of 100 to 200 angstroms by thermal oxidation on the surface of the epitaxial layer 2, and also on the surfaces of the polycrystalline silicon layers 14,15. Then an SiO_2 film 36 is formed to a thickness of 1500 angstroms by the CVD method. The SiO_2 film 36 is selectively removed by plasma etching using a photoresist film (not shown) as a mask, to complete the mask for forming the p-type regions. When forming the mask 36, the processing with photoresist does not require so high a precision. That is, the mask may be slightly shifted provided that its ends 36a,36b and

36c are on the field oxide film 17. Then p-type impurities such as boron ions are implanted (or diffused) into the surfaces of the n-type well regions 3,4 not covered by the polycrystalline silicon layer 14, the field oxide film 17 and the mask 36, in order to form the p-type regions 5 and 6 that serve as the injector and base of the I^2L, and to form the p^+-type source and drain regions 9 of the p-channel MISFETs. As will be obvious from Fig. 2F, the p-type region 5 is self-aligned by the field oxide film 17, and the p^+-type source and drain regions 9 are self-aligned by the field oxide film 17 and by the polycrystalline silicon 14.

Next, as shown in Fig. 2G, n-type semiconductor regions are selectively formed in the epitaxial layer 2 and in the n-type well region 3. First, the SiO_2 film 36 is removed, and a new SiO_2 film 37 is formed to a thickness of 1500 angstroms by the CVD method. The SiO_2 film 37 is then selectively removed by plasma etching using a photoresist film (not shown) as a mask, to complete the mask for forming the n-type regions. When forming the mask 37, the processing with photoresist does not require a high precision, as when forming the mask 36. Then n-type impurities such as phosphorus ions are implanted into the surface of the epitaxial layer 2 where the polycrystalline silicon layer 15 and the field oxide film 17 have not been formed, and into the surface of the well region 3 where the mask 37 and the field oxide film 17 have not been

formed, thereby forming the emitter contact region 8 of the I^2L, and the n^+-type source and drain regions 10 of the n-channel MISFETs.

Next, an n-type collector region is formed as shown in Fig. 2H. That is, after the SiO_2 film 37 is removed, a new SiO_2 film 38 is formed to a thickness of 1500 angstroms by the CVD method. The SiO_2 film 38 is then selectively removed by plasma etching using a photoresist film (not shown) as a mask, to complete the mask for forming the n-type collector region. Then n-type impurities such as phosphorus ions are introduced by implantation (or diffusion) to form an n-type collector 7.

After the SiO_2 film 38 is removed, an SiO_2 film 18 (see Fig. 1) is formed on the whole surface of the semiconductor body thus formed to a thickness of 1500 angstroms as an interlayer insulation film by the CVD method. After contact holes have been formed in the SiO_2 film 18, aluminum is deposited thereon to a thickness of 8000 angstroms by the vacuum evaporation method. The aluminum layer is patterned to the desired shape to form the aluminum electrodes 19 to 24 that are in ohmic contact with each region. Thus, the CMISFET-I^2L IC of the construction shown in Fig. 1 is completed.

According to this construction, use is made of a p^--type epitaxial silicon layer of a low impurity concentration, and the I^2L circuit and the p-channel MISFETs are formed in the n-type well regions that are separately formed in the epitaxial layer. Therefore, the impurity

concentration can be controlled for each of the well regions. By making the impurity concentration in the n-type well region 3 on the I^2L side greater than the impurity concentration of the well region 4, therefore, the inverse current amplification factor βi of the inverse transistors in the I^2L circuit can be enhanced to realize a I^2L which operates at high speeds and which consumes a reduced amount of electric power. With the impurity concentration being made low in the n-type well region 4 on the p-channel MISFET side, furthermore, high-speed operation can be realized even when the gate width of the MISFET is reduced. Accordingly, the chip size can be reduced but the high-speed operation is maintained.

Further, as will be obvious from the method of manufacturing the integrated circuits explained in conjunction with Figs. 2A to 2H, the well regions 3,4 are formed in the epitaxial layer 2 before forming the field oxide film 17 by the selective oxidation technique. In the well region 4 constituting the I^2L, therefore, a field oxide film can be formed in the I^2L elements to prevent the formation of parasitic transistors. The surface of the well region 3 under such a thick field oxide film is difficult to invert. Therefore, a wide range of power-supply voltages can be applied, and increased freedom is provided for laying out the wiring. Further, the surface of the well region 4 is also difficult to invert. Accordingly, the above-mentioned advantages are brought

about.

When forming the CMISFETs, furthermore, employment of the silicon gate processing technique makes it possible to obtain a CMISFET-I^2L IC of a high density.

In order to obtain the CMISFET-I^2L IC having a complementary MISFET circuit which operates at high speeds and which is highly integrated, and an I^2L circuit which operates at high speed and which consumes a reduced amount of power, formed in the same epitaxial layer, (1) the complementary MISFET circuit which operates at speeds faster than the I^2L circuit should be disposed on the input stage of the integrated circuit, and the I^2L circuit should be disposed on the output stage, and (2) the output of the complementary MISFET circuit should be directly connected to the input of the I^2L circuit without an interface circuit being disposed therebetween.

Fig. 3 is a diagram showing the circuits of a CMISFET-I^2L IC which is constructed by taking the above-mentioned points into consideration.

In Fig. 3, circuit I is a high-speed circuit consisting of a complementary MISFET circuit, circuit II consists of an I^2L circuit operating at speeds slower than circuit I, and circuit III acts to bias the I^2L circuit. In Fig. 3, the symbol Q_M denotes MISFETs, and in particular Q_{M11} and Q_{M21} denote p-channel MISFETs, and Q_{M12} and Q_{M22} denote n-channel MISFETs. Symbol Q_I denotes transistors that constitute the I^2L circuit. In particular, Q_{I11} and

Q_{I31} denote lateral transistors, and Q_{I12} and Q_{I32} denote inverse transistors.

Input signals V_{IN} from an external source are first received by circuit I. Circuit I is made up of, for example, an input protection circuit consisting of an input protection resistance R and an input protection diode D, a first-stage inverter consisting of MISFETs Q_{M11} and Q_{M12}, a signal processing circuit (not shown) which is connected thereto, and a final-stage inverter consisting of MISFETs Q_{M21} and Q_{M22} sending the output of the signal processing circuit to the I^2L circuit. Therefore, the input signal V_{IN} passes through the input protection circuit and the first-stage inverter, and is suitably processed at high speeds in the signal processing circuit, and the processed result is produced from the final-stage inverter in circuit I.

The output terminal of the final-stage inverter is directly connected to the input terminal of circuit II without passing through an interface. Therefore, the output signal from the complementary MISFET circuit (circuit I) is directly supplied to the I^2L circuit (circuit II).

Circuit II is made up of, for example, a first-stage inverter consisting of transistors Q_{I11} and Q_{I12}, a signal processing circuit (not shown) connected thereto, a final-stage inverter consisting of transistors Q_{I31} and Q_{I32} sending the output of the signal processing circuit to an

external unit, and a load transistor Q_L. Therefore, the output from circuit I passes through the first-stage inverter of circuit II, is suitably processed through the signal processing circuit, and the processed result is sent to an external unit via the final-stage inverter and via the load transistor Q_L.

Fig. 4 is a plan view which schematically shows the layout of the connection between circuit I and circuit II of Fig. 3, and in which cross-sections formed along the dot-dash chain lines X_1,X_2 denote the same areas as the areas X_1 and X_2 of Fig. 1. Further, the same parts as those of Fig. 1 are denoted by the same reference numbers.

Thus, the circuit consisting of complementary MISFETs is placed on the input side of the integrated circuit, and circuit II comprising the I^2L is placed on the output side of the integrated circuit, because of reasons mentioned below. The complementary MISFET circuit operates at speeds faster than the I^2L circuit, and the speed of the integrated circuit can be increased as a whole if it is placed on the input side. Further, unlike the complementary MISFET circuit, the I^2L circuit can be current-driven. Placing the I^2L circuit on the output side, therefore, increases the number of fan-outs that can be obtained, other integrated circuits can be directly driven, and the performance of the integrated circuit can be enhanced.

Further, circuit I is directly connected to circuit II without an interface circuit, because of reasons

mentioned below.

When the power-source voltage V_{CC} is 5 volts, the complementary MISFET circuit produces an output current over a range of 10 to 50 μA and an output voltage over a range of from about 0 volt to about 5 volts. The I^2L circuit, on the other hand, allows the introduction of a current over a range of 10 to 500 μA, and voltage of 1 to 15 volts. When the two circuits are directly connected without an interface circuit, the operation will be as described below. When the MISFET Q_{M21} is on, and the MISFET Q_{M22} is not, i.e., when a high signal level (about 5 volts) is applied to the gate-connection point G, electric current flows from the power source V_{CC} to the I^2L circuit through MISFET Q_{M21}, and the potential rises at the base of the inverse transistor Q_{I12} so that it is turned on. Therefore, the output OUT of the first-stage inverter in the I^2L circuit goes low (about 0 volt). The current flows through the paths indicated by the arrows (1). A potential nearly equal to V_{CC} is applied to the emitter of the transistor Q_{I11} via the I^2L bias circuit III. Therefore, when the MISFET Q_{M21} is turned on, the base potential of the transistor Q_{I12} instantaneously rises, and part of the current flowing from the transistor Q_{M21} to the I^2L circuit also flows from the collector to the base of the transistor Q_{I11}, but does not flow to the emitter thereof. The current flowing in the other direction is so small that it can be neglected. This can be attributed to the high

impurity concentration in the well region 3. When the MISFET Q_{M22} is on (MISFET Q_{M21} is off), i.e. when a low signal level (about 0 volt) is applied to the point G, the base of the transistor Q_{I12} nearly reaches ground potential so that it is turned off, and the output of the first-stage inverter in the I^2L circuit becomes a high signal level. Namely, the current flows through the path indicated by the arrow (2). In this case, the current taken by the complementary MISFET circuit from the I^2L circuit can be absorbed by suitably setting the ratio W/L of the gate width to gate length of the MISFET Q_{M22}. Because of these reasons, the complementary MISFET circuit can be directly connected to the I^2L circuit without using an interface circuit.

According to the above-mentioned embodiment, the following effects can be obtained.

(1) The I^2L elements and the p-channel MISFETs are respectively formed in different semiconductor regions, i.e. in different well regions formed at different steps. Therefore, the impurity concentration of each well region can be controlled independently. This makes it possible to slightly increase the impurity concentration in the well region where the I^2L circuit is formed, and to slightly decrease the impurity concentration in the well region where the p-channel MISFETs are formed. Accordingly, it is possible to form an I^2L circuit which operates at high speeds consuming a reduced amount of electric power, and a

complementary MISFET circuit which operates at faster speeds and which is highly integrated on the same semiconductor substrate. Therefore, a CMISFET-I^2L IC is obtained which features high-speed operation, low power consumption, and a high degree of integration.

(2) The well region and the semiconductor substrate have a reversed bias relationship or are at the same potential, so that no isolation region is needed to insulate and separate these regions. This means that the degree of integration can be increased accordingly.

(3) The n-type well region for forming the I^2L circuit, the p-type epitaxial layer for forming the n-channel MISFETs and the p-type substrate can be maintained at the same potential (ground potential), to prevent the development of parasitic bipolar transistors. Therefore, the reliability of the integrated circuit can be increased. Further, since the distance between the semiconductor regions does not need to be increased to prevent the formation of parasitic bipolar transistors, the integrated circuit can be easily designed, maintaining an increased degree of integration.

(4) Since the complementary MISFET circuit is directly coupled to the I^2L circuit without any interface circuit, the chip area can be reduced to simplify the design.

(5) A complementary MISFET circuit operates faster than a I^2L circuit. By placing the complementary MISFET

circuit on the input side, therefore, the operating speed of the integrated circuit can be increased as a whole. By placing the I^2L circuit on the output side, furthermore, an increased number of fan-outs can be obtained, making it possible to directly drive other elements.

(6) The output characteristics of the integrated circuit are greatly improved by providing the final output stage of the I^2L circuit with a load transistor Q_L equivalent to a pull-up resistance, as shown in Figs. 3 to 5. That is, provision of the load transistor Q_L (a) eliminates the need for attaching an external pull-up resistor for the integrated circuit, and hence enables the integrated circuit to be directly connected to other transistors and integrated circuits, (b) helps increase the ability for driving other integrated circuits (helps increase fan-outs), and (c) helps eliminate the defect that when the external pull-up resistance is employed, the resistance must be increased with any increase in the power-supply voltage V_{CC}, resulting in an increase in the consumption of electric power through the resistance.

Further, as Fig. 5 schematically illustrates the layout, the load transistor Q_L can be easily formed by providing a p^+-type region 40 simultaneously with the formation of other p^+-type region 6 in the n-type well region 3 in which the I^2L circuit is formed, i.e. the load transistor Q_L can be formed as a pnp lateral transistor which consists of the region 40 and the injector region 5,

without modifying the manufacturing conditions or process, and without needing any particular design requirements.

(7) As shown in Fig. 3, an increased current can be passed into the transistor Q_{I12} of the first stage of the I^2L circuit (the current flows from the MISFETs Q_{M21}, Q_{I11} as indicated by the arrows (1)) to increase the operating speed of the transistor Q_{I12}, and to reduce the frequency loss when signals are transmitted from the complementary MISFET circuit to the I^2L circuit.

The present invention, however, should in no way be limited to the above-mentioned embodiment only.

Fig. 6 is a diagram which illustrates another embodiment of the present invention, in which the same parts as those of the first embodiment are denoted by the same reference numbers.

This embodiment does not employ the lateral transistor Q_{I11} (the injector with respect to the transistor Q_{I12}) in the first stage of the I^2L circuit that was employed in the first embodiment. The construction of the other parts is the same as that of the first embodiment.

The operation in the past where the complementary MISFET circuit I is connected to the I^2L circuit II in the integrated circuit is described below. When the p-channel MISFET Q_{M21} is on (the n-channel MISFET Q_{M22} is off), current flows from the power source V_{CC} to the I^2L circuit II via MISFET Q_{M21}, so that the base potential of the

inverse transistor Q_{I12} rises. Therefore, the transistor Q_{I12} is turned on, and the first-stage inverter consisting of the transistor Q_{I12} produces a low-level output. The current runs from the power source V_{CC} to ground via the MISFET Q_{M21} and transistor Q_{I12}. Conversely, when the MISFET Q_{M22} is on (MISFET Q_{M21} is off), a discharge current flows from the base of the transistor Q_{I12} to ground via the MISFET Q_{M22}, and the potential at the base of the transistor Q_{I12} nearly reaches ground potential. Consequently, the transistor Q_{I12} is turned off, and the inverter of the first stage produces a high-level output. In this case, therefore, only a discharge current flows from the transistor Q_{I12} to ground via MISFET Q_{M22}, and no steady-state current flows.

This embodiment makes it possible to obtain the same effects as (1) to (6) obtained with the first embodiment. When the MISFET Q_{M22} is turned on, no steady-state current flows through the first stage of the I^2L circuit, enabling the consumption of power to be further reduced.

Fig. 7 is a diagram illustrating a further embodiment according to the present invention, in which the same parts as those of the first embodiment are denoted by the same reference numbers.

This embodiment does not employ the p-channel MISFET Q_{M21} in the inverter in the final stage of the complementary MISFET circuit that was used in the aforementioned first embodiment. In all other respects, however, the

construction is the same as that of the first embodiment. The operation in the part where the complementary MISFET circuit I is connected to the I^2L circuit II in the integrated circuit is now explained. When the p-channel MISFET Q_{M22} is off, no current path is formed from the lateral transistor Q_{I11} to the complementary MISFET circuit I, the transistor Q_{I11} is saturated. Therefore, the base potential of the transistor Q_{I12} rises so that it is turned on, and the first-stage inverter produces a low-level output. The current runs from the power source V_{CC} to ground via the I^2L bias circuit III, and transistors Q_{I11} and Q_{I12}. When the n-channel MISFET Q_{M22} is on, the circuit operates in the same manner as in the first embodiment. This embodiment also makes it possible to obtain the same effects as (1) to (6) of the first embodiment.

The invention can further be modified in a variety of other ways in addition to the above-mentioned embodiments. In the above-mentioned embodiments, for instance, the n^+-type buried layer 16 may be eliminated. In this case, the n-type well regions 3 and 4 may be formed in the p^--type silicon substrate 1 without forming the p-type epitaxial layer 2. Further, the high impurity concentration n-type well region where the I^2L circuit will be formed, may be formed in the following manner. Ions are implanted simultaneously with the formation of the n-type well region 4 where the p-channel MISFETs will be formed, and ions are

again implanted into the well region 3 while the well region 4 is covered by a mask. The above-mentioned order may of course be reversed. Further, the conductivity types of the semiconductor regions may be reversed.

Fig. 8 shows a complementary MISFET-I^2L IC according to a still further embodiment of the present invention. According to this embodiment, the I^2L circuit is formed in an epitaxial layer that is grown on the substrate, the n-channel MISFETs are formed in the epitaxial layer, in order to increase the local impurity concentration in the epitaxial layer where the I^2L circuit will be formed. That is, use is made of epitaxial layers that are insulated and separated as semiconductor regions that correspond to the well regions in the aforementioned embodiments, and the impurity concentrations are changed.

According to this embodiment as shown in Fig. 8, a low-concentration p^--type epitaxial layer 52 is allowed to grow on an n^--type silicon substrate 51 having a low impurity concentration. The p^--type epitaxial layer 52 is separated by an n-type isolation region 62 into the area X_1 where the complementary MISFETs will be formed and the area X_2 where the I^2L circuit will be formed. P-type impurities such as boron ions are implanted in a part 53 of the p^--type epitaxial layer 52 having a low impurity concentration in the area X_2, to increase the impurity concentration. An n^+-type injector region 58, and an inverse transistor

consisting of n^+-type base region 59, an emitter electrode contact region 60 and an emitter region 52, are formed in the region 53 thereby forming an I^2L circuit. N-channel MISFETs consisting of n^+-type source and drain regions 56, a gate insulation film 66 and a polycrystalline silicon layer 67 that serves as a gate electrode, and p-channel MISFETs consisting of p^+-type source and drain regions 57, a gate insulation film 63 and a polycrystalline silicon layer 64 that serves as a gate electrode in the n-type well region 54, are formed in the low impurity concentration epitaxial layer 52 in the area X_1 thereby forming a complementary MISFET circuit.

According to this embodiment, it is also possible to form a complementary MISFET circuit which operates at high speeds and which can be highly integrated, and an I^2L circuit which operates at high speeds consuming a reduced amount of electric power on the same substrate, just like the first embodiment. To obtain these advantages sufficiently, the connections should be realized as in Fig. 9.

In Fig. 9, symbols $Q_{I\bar{1}1}$..... denote transistors which correspond to Q_{I11}..... of Fig. 3, and which have opposite types of conductivity. Therefore, the relationship of the potential is reversed relative to Fig. 3. That is, the collector (the epitaxial layer 52) of the inverse transistor $Q_{I\bar{1}2}$ has a potential of 0.7 volt that is supplied through the I^2L bias circuit III, and the base of

the lateral transistor $Q_{I\overline{11}}$ in the same region (in the epitaxial layer 52) has a potential of 0.7 volt that is supplied by the I^2L bias circuit III. The injector region which is the emitter of the lateral transistor $Q_{I\overline{11}}$ has been grounded. The potential in the p^--type epitaxial layer in the region X_1 where the complementary MISFET circuit is formed is at ground potential. Therefore, the p-type epitaxial layer 52 is isolated by the n^--type semiconductor substrate 51 and by the n-type isolation layer 62, as shown in Fig. 8.

The operation of the part where the complementary MISFET circuit I is connected to the I^2L circuit II in the integrated circuit is now described. When the p-channel MISFET Q_{M21} is on (MISFET Q_{M22} is off), the base potential of the transistor $Q_{I\overline{12}}$ rises above 0.7 volt, the transistor $Q_{I\overline{12}}$ is turned off and the first-stage inverter of the I^2L circuit II produces a high-level output. When the n-channel MISFET Q_{M22} is on (MISFET Q_{M21} is off), the base of the transistor $Q_{I\overline{12}}$ nearly reaches ground potential, i.e. the transistor $Q_{I\overline{12}}$ is turned on, and the first-stage inverter produces a low-level output. The current runs from the I^2L circuit II to ground via the transistors $Q_{I\overline{12}}$, Q_{M22}. This embodiment makes it possible to obtain the same effects (1), (4), (5) and (6) as mentioned above.

(42)

This specification describes matter also disclosed in U.K. Patent Application No. 8502453 (published under No. 2154060A) and U.K. Patent Application No. 8502454 (published under No. 2054061A) which were divided from the present application. Attention is therefore drawn to those applications.

* C L M S *

CLAIMS

1. A semiconductor integrated circuit device comprising an epitaxial semiconductor layer having a first conductivity type formed on a semiconductor substrate, first and second semiconductor well regions having a second conductivity type opposite to said first conductivity type that are formed in the epitaxial semiconductor layer separated from each other, a plurality of third semiconductor regions which constitute the elements of an I^2L circuit that is formed in the first semiconductor region, and a plurality of fourth semiconductor regions which constitute the elements of a MISFET circuit that is formed in the second semiconductor region, wherein the first semiconductor region has an impurity concentration that is greater than that of the second semiconductor region.

2. A device according to claim 1 wherein the third semiconductor regions include an injector region of opposite conductivity type to the first semiconductor region and a base region of an inverse transistor.

3. A device according to claim 1 or claim 2, wherein the fourth semiconductor regions include source and drain regions of the MISFET circuit of opposite conductivity type to the second semiconductor region.

4. A device according to any one of claims 1 to 3, having a plurality of fifth semiconductor regions in part of the epitaxial semiconductor layer separated from the first and second semiconductor regions, the fifth semiconductor regions forming sources and drains of MISFETs having channels of the second conductivity type, and the fourth semiconductor regions form sources and drains of MISFETs having channels of the first conductivity type.

5. A semiconductor integrated circuit device according to claim 4, wherein gate electrodes of MISFETs having channels of said first type of conductivity type and of MISFETs having channels of said second conductivity type, consist of polycrystalline silicon.

6. A semiconductor integrated circuit device according to claim 5, wherein the first conductivity type is p-type.

7. A semiconductor integrated circuit device, substantially as any described herein with reference to the accompanying drawings.