

**PLASMA ENHANCED ATOMIC LAYER DEPOSITION
OF SILICON-CONTAINING FILMS**

INCORPORATION BY REFERENCE

5 **[0001]** A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein its entirety for all purpose.

BACKGROUND

10 **[0002]** Many semiconductor device fabrication processes involve formation of films including silicon-containing films such as silicon nitride and silicon oxide. Plasma enhanced atomic layer deposition (ALD) may be used to deposit silicon-containing films.

15 **[0003]** The background description provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

SUMMARY

20 **[0004]** One aspect of the disclosure relates to a method including:

providing a substrate in a processing station including a substrate support and a showerhead, the substrate including a gap to be filled; and

depositing silicon-containing film in the gap by a plasma-enhanced atomic layer deposition (PEALD) process including multiple cycles of operations (a)-(d):

- 25 (a) a dose operation including flowing a silicon-containing precursor into the processing station via the showerhead to allow the silicon-containing precursor to adsorb onto the substrate;
- (b) after (a), flowing a purge gas into the processing station;
- (c) after (b), exposing the substrate to plasma species to react with the adsorbed
- 30 silicon-containing precursor; and
- (d) after (c), flowing a purge gas into the processing station,

wherein the silicon-containing precursor continues to flow into the processing station during at least (b).

5 [0005] In some embodiments, the silicon-containing precursor continues to flow into the processing station during at least part of (c). In some embodiments, the silicon-containing precursor continues to flow into the processing station during (c) and at least part of (d). In some embodiments, after (a), the silicon-containing precursor flow continues into flow into the processing station at a decreasing flow rate.

10 [0006] In some embodiments, (a) includes flowing an inert gas and a vaporized silicon-containing precursor from a silicon-containing precursor source fluidically connected to a gas delivery line via an outlet valve, the gas delivery line fluidically connected to the showerhead, and at the end of (a), closing the outlet valve. In some such embodiments, silicon-containing precursor in the gas delivery line continues to flow into the processing station after the outlet valve is closed.

[0007] In some embodiments, the method further includes diverting silicon-containing precursor from the processing station during one or more of (c) and (d).

15 [0008] In some embodiments, the plasma in (c) is a dual frequency RF plasma generated using high frequency (HF) and low frequency (LF) RF power. In some such embodiments, the HF power is at least 4 kW and the LF power is between 500 W and 5 kW.

20 [0009] In some embodiments, the method further includes increasing an inert gas flow into the processing station during (c). In some embodiments, the method further includes sputtering and re-depositing silicon-containing film in the gap during deposition of the silicon-containing film in the gap.

25 [0010] In some embodiments, the plasma species are generated from oxygen (O_2). In some embodiments, the plasma species are generated from nitrous oxide (N_2O). In some embodiments, the plasma species are generated from nitrogen (N_2). In some embodiments, (b) is between 50–500 milliseconds in duration. In some embodiments, the gap to be filled is a gap between memory stacks of a 3D NAND structure. In some embodiments, the gap has aspect ratio of at least 20:1.

[0011] In some embodiments, the method further includes exposing the deposited film to an inhibition plasma before at least one of the multiple cycles. Another aspect of the disclosure relates to a comprising:

30 providing a substrate in a processing station comprising a substrate support and a showerhead, the substrate comprising a gap to be filled; and

depositing silicon-containing film in the gap by a plasma-enhanced atomic layer deposition (PEALD) process comprising multiple cycles of operations (a)-(d):

- (a) a dose operation comprising flowing a silicon-containing precursor into the processing station via the showerhead to allow the silicon-containing precursor to adsorb onto the substrate;
- (b) after (a), flowing a purge gas into the processing station;
- 5 (c) after (b), exposing the substrate to plasma species generated from a reactant gas to react with the adsorbed silicon-containing precursor; and
- (d) after (c), flowing a purge gas into the processing station, wherein the reactant gas and/or the plasma species continue to flow into the processing station during at least (a).

10 **[0012]** Another aspect of the disclosure relates to a method including: providing a substrate having a structure including a gap to be filled; depositing a silicon-containing protective film selectively at an upper portion of the structure such that it extends only partially into the gap by a plasma-enhanced atomic layer deposition (PEALD) process including:

- (a) a dose operation including flowing a silicon-containing precursor into the processing station via the showerhead to allow the silicon-containing precursor to adsorb onto the substrate;
- 15 (b) after (a), flowing a purge gas into the processing station;
- (c) after (b), exposing the substrate to plasma species to react with the adsorbed silicon-containing precursor, wherein the plasma in (c) is a dual frequency RF plasma generated using high frequency (HF) and low frequency (LF) RF power; and
- 20 (d) after (c), flowing a purge gas into the processing station.

[0013] In some embodiments, the method further includes performing one or more cycles of:

exposing the substrate including the protective film to an inhibition plasma including halogen species to inhibit deposition on a portion of the gap; and

25 after exposing the substrate to the inhibition, depositing dielectric material in the gap.

[0014] In some embodiments, the silicon-containing precursor continues to flow into the processing station during at least (b). In some embodiments, the protective film is etched during

exposure to the inhibition plasma. In some embodiments, the plasma during (a) is generated from nitrogen trifluoride (NF₃) and the protective liner is a silicon nitride film.

[0015] In some embodiments, the protective liner is between 10 and 999 Angstroms thick. In some embodiments, depositing a protective liner and the performing one or more cycles are performed in the same chamber.

[0016] In some embodiments, the structure is a 3D NAND structure, the gap is formed by two stacks each including multiple pairs of an oxide layer and a nitride layer and capped by a polysilicon layer and wherein the protective film protects the polysilicon layer.

[0017] Another aspect of the disclosure relates to method including:

10 providing a substrate in a processing station including a substrate support and a showerhead;

depositing a silicon-containing film on the substrate by a plasma-enhanced atomic layer deposition (PEALD) process including multiple cycles of operations (a)-(d):

15 (a) a dose operation including flowing a silicon-containing precursor into the processing station via the showerhead to allow the silicon-containing precursor to adsorb onto the substrate;

(b) after (a), flowing a purge gas into the processing station;

(c) after (b), exposing the substrate to plasma species to react with the adsorbed silicon-containing precursor; and

20 (d) after (c), flowing a purge gas into the processing station, wherein the silicon-containing precursor continues to flow into the processing station during at least (b).

[0018] In some embodiments, the silicon-containing film fills a gap on the substrate. In some embodiments, the silicon-containing film is non-conformally deposited on a structure having two stacks separated by a gap such that the film is deposited at the top of the stacks extending only partially into gap. In some embodiments, the plasma in (c) is a dual frequency RF plasma generated using high frequency (HF) and low frequency (LF) RF power.

[0019] Another aspect of the disclosure relates to a method including:

30 providing a substrate in a processing station including a substrate support and a showerhead;

depositing a silicon-containing film on the substrate by a plasma-enhanced atomic layer deposition (PEALD) process including multiple cycles of operations (a)-(d):

- 5 (a) a dose operation including flowing a silicon-containing precursor into the processing station via the showerhead to allow the silicon-containing precursor to adsorb onto the substrate;
- (b) after (a), flowing a purge gas into the processing station;
- (c) after (b), exposing the substrate to plasma species to react with the adsorbed silicon-containing precursor; and
- (d) after (c), flowing a purge gas into the processing station,
- 10 wherein the plasma in (c) is a dual frequency RF plasma generated using high frequency (HF) and low frequency (LF) RF power

[0020] In some embodiments, the silicon-containing film fills a gap on the substrate. In some embodiments, the silicon-containing film is non-conformally deposited on a structure having two stacks separated by a gap such that the film is deposited at the top of the stacks extending only partially into gap.

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[0021] Yet, another aspect of the disclosure relates to providing a substrate in a processing station; depositing a silicon oxynitride (SiON) film on the substrate by:

- 20 (a) stabilizing process conditions in the processing station for silicon oxide deposition;
- (b) performing x plasma-enhanced atomic layer deposition (PEALD) cycles using an oxygen-based plasma, where x is an integer greater than zero;
- (c) stabilizing process conditions in the processing station for silicon nitride deposition;
- 25 (d) performing y plasma-enhanced atomic layer deposition (PEALD) cycles using a nitrogen-based plasma, where y is an integer greater than zero; and
- (e) repeating (a)-(d) one or more times.

[0022] In some embodiments, $x + y$ is no more than 20, 15, or 10.

[0023] In some embodiments, the oxygen-based plasma of each cycle of (b) has a first duration and the nitrogen-based plasma of each cycle of (d) has a second duration wherein the second duration is at least twice as long as the first duration. In some embodiments, the SiON film is conformally deposited on a patterned layer.

5 [0024] These and other aspects are described further below with reference to the drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0025] Fig. 1 is a schematic of a gas delivery system for delivering reactants to a single station of a multi-station reaction chamber (not shown) which may be used to perform one or more ALD cycles.

10 [0026] Figs. 2 and 3 shows example timing diagrams for plasma enhanced atomic layer deposition (PEALD) of silicon oxide in a four-station chamber including divert of the silicon-containing precursor.

[0027] Fig. 4 shows a simplified schematic of a portion of a gas delivery system for delivering a silicon-containing precursor.

15 [0028] Figs. 5–9 provide examples of timing sequences for PEALD deposition of silicon oxide that include a CVD-type component.

[0029] Fig. 10 shows an example of deposition rate as a function of RF purge time, holding all other process parameters constant.

20 [0030] Fig. 11a shows an example of a structure including an unfilled gap that may be filled using methods described herein.

[0031] Fig. 11b shows an example of a structure including an unfilled gap between two memory stacks that may be filled using methods described herein.

25 [0032] Fig. 11c shows an example of a structure including an air gap that may be formed using the methods described herein.

[0033] Fig. 12a shows an example of a process sequence that may be used in accordance with the disclosed embodiments including deposition of a protective film.

[0034] Fig. 12b shows an example of a structure before and after deposition of a protective film.

30 [0035] Fig. 13 shows thickness non-uniformity (NU) and refractive index (RI) for films deposited using PEALD with high frequency RF power only and high frequency RF power and low frequency RF power.

[0036] Fig. 14 presents a process flow diagram for a single PEALD cycle that may be implemented as part of deposition of a protective liner or for any of the other ALD operations shown in Fig. 12b.

[0037] Fig. 15 is a process flow diagram for a method of forming a silicon oxynitride layer.

[0038] Fig. 16A shows refractive index (RI) and density for films deposited using various numbers of SiN cycles in a method according to Fig. 15.

5 [0039] Fig. 16B shows FTIR spectra for four 3 kÅ thick films deposited using methods described herein.

[0040] Fig. 16C shows a schematic example of a SiON film having a tuned composition and dry etch rate conformally deposited on a patterned layer.

10 [0041] Fig. 17 depicts a schematic illustration of an embodiment of a plasma enhanced atomic layer deposition (PEALD) process station that may be used to implement methods described herein.

[0042] Fig. 18 schematically shows an example substrate processing apparatus that may be used to implement the methods described herein.

DETAILED DESCRIPTION

15 [0043] In the following description, numerous specific details are set forth to provide a thorough understanding of the presented embodiments. The disclosed embodiments may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed embodiments. While the disclosed embodiments will be described in conjunction with the specific embodiments, it will
20 be understood that it is not intended to limit the disclosed embodiments.

[0044] Semiconductor manufacturing processes often involve deposition of dielectric materials including silicon-containing films. Such film may be used for gap fill in structures including 3D NAND structures, DRAM structures, and shallow trench isolation (STI) structures or onto
25 patterned substrates to form conformal films for various applications, such as barrier layers for contacts. Silicon nitride and silicon carbide layers may be used as encapsulation films, spacers, and barrier films in advanced devices for logic and memory structures, such as FinFETs, MRAM, 3DXPoint, ReRAM, and PCRAM.

[0045] Embodiments described herein involve deposition by ALD. ALD is a technique that deposits thin layers of material using sequential self-limiting reactions. Typically, an ALD cycle
30 includes operations to deliver and adsorb at least one reactant to the substrate surface, and then react the adsorbed reactant with one or more reactants to form at least a partial layer of film. As an example, a silicon oxide deposition cycle may include the following operations: (i) delivery/adsorption of a silicon-containing precursor, (ii) purging of the silicon-containing precursor from the chamber, (iii) delivery of an oxygen-containing reactant with an optional

plasma, and (iv) purging of the oxygen-containing reactant and/or plasma from the chamber. When a plasma is used during delivery of the second reactant, in some embodiments, this is referred to as plasma-enhanced atomic layer deposition (PEALD). Delivery or adsorption of the silicon-containing precursor may be referred to as a “dose” operation and delivery of the second reactant to react with the adsorbed precursor may be referred to as a “conversion” operation.

[0046] Unlike a chemical vapor deposition (CVD) technique, ALD processes use surface-mediated deposition reactions to deposit films on a layer-by-layer basis. In one example of an ALD process, a substrate surface that includes a population of surface-active sites is exposed to a gas phase distribution of a first precursor, such as a silicon-containing precursor, in a dose provided to a chamber housing a substrate. Molecules of this first precursor are adsorbed onto the substrate surface, including chemisorbed species and/or physisorbed molecules of the first precursor. It should be understood that when the compound is adsorbed onto the substrate surface as described herein, the adsorbed layer may include the compound as well as derivatives of the compound. For example, an adsorbed layer of a silicon-containing precursor may include the silicon-containing precursor as well as derivatives of the silicon-containing precursor. After a first precursor dose, the chamber is then evacuated to remove most or all of first precursor remaining in gas phase so that mostly or only the adsorbed species remain. In some implementations, the chamber may not be fully evacuated. For example, the chamber may be evacuated such that the partial pressure of the first precursor in gas phase is sufficiently low to mitigate a reaction. A second reactant, such as an oxygen-containing reactant, is introduced to the chamber so that some of these molecules react with the first precursor adsorbed on the surface. In some processes, the second precursor reacts immediately with the adsorbed first precursor. In other embodiments, the second reactant reacts only after a source of activation is applied temporally. In some embodiments, a plasma is ignited during the second reactant dose. The chamber may then be evacuated again to remove unbound second reactant molecules. In some embodiments the chamber may not be completely evacuated. Additional ALD cycles may be used to build film thickness. Examples of silicon-containing first reactants (also referred to as silicon-containing precursors) and second reactants (also referred to as co-reactants) are provided below.

[0047] Schematically illustrated in Fig. 1 is a gas delivery system 100 for delivering reactants to a single station of a multi-station reaction chamber (not shown) which may be used to perform one or more ALD cycles. The figure illustrates a configuration of gas flow lines, manifolds, valves, regulators, filters, showerhead, etc. for providing for ALD reactant delivery. Gas lines are schematically indicated as thin solid lines with arrows indicating the direction of gas flow; valves are indicated in the figure with crossed lines within a circle; regulators by an arrow within a circle;

manifolds by solid boxes labeled “Manifold”; filters with curved lines either side of a gas line, etc. Most of the gas flow lines route gas to the “showerhead” 110, which as shown in this schematic, is the device which delivers the ALD reactants to a reaction chamber which is not shown.

[0048] Thus, in reference to the particular embodiment of a gas delivery system 100 shown in Fig. 1, the delivery of film precursor (e.g., silicon-containing film precursor) to the reaction chamber—relevant to the ALD dosing and adsorption step (see operation (i) above)—may involve introducing precursor from a liquid delivery system (labeled “LPDS”) 120 to a heated injection manifold 125 (labeled “HIM”) where it is mixed with a preheated (see “preheater” 124) inert carrier gas originating from gas source 130 (“Manifold A”). The carrier gas then carries the precursor to an array of four valves 169, 164, 165, 166 which as an assembly 160 can be referred to as a point-of-use valve manifold (PVM) due to its close proximity (in terms of gas flow distance) to the reaction chamber. In particular, from the PVM 160, with valve 165 open and valve 166 closed, the precursor and carrier gas are flowed directly to the showerhead 110 and then into the reaction chamber.

[0049] Likewise, delivery system 100 of Fig. 1 also illustrates delivery of oxidant to a reaction chamber for use in ALD—relevant to the generation of an oxidative plasma and its reaction with adsorbed silicon-containing precursor (see step (iii) above). Specifically, gas source 140 (“Manifold C”) is shown as a source of O₂ and/or N₂O gas which is flowed to the showerhead 110 through valve 169 of the PVM 160 shown in the figure. The presence of Manifold C 140 and also “Manifold D” 170 should also be noted in the context of this configuration as they may be used to deliver inert gases for post-dose purge (step (ii) above) and post-RF purge (step (iv) above). With regards to Manifold D 170, the gas delivery system 100 is configured such that purge gas sourced from Manifold D passes through “Preheater” 171 and then is flowed on two paths towards the showerhead. Purge gas flowing on both paths pass through a regulator (172 or 173) and then on through a filter (173B or 175B) flanked upstream and downstream by valves (173A and 173C or 175A and 175C). One path then proceeds directly to showerhead 110, while the other connects to POS 160 first, in order to purge any remaining reactant gases lingering in the POS device after the dosing step. Also, note that, in some embodiments, precursor may be removed from the volume surrounding a processing station within a reaction chamber by applying vacuum to the reaction chamber (e.g., through the operation of a valve-operated vacuum source) without employing the use of an inert purge gas.

[0050] In addition, also note that Fig. 1 exhibits a remote plasma source 195, employing a NF₃-based plasma (as indicated in the figure), whose fluidic coupling to the reaction chamber and process station is regulated by valve 116. Finally, note that in some embodiments, Manifold B

150 (as regulated by valve 144) may serve as a source of a co-reactant gas—for example, a nitrogen-containing co-reactant such as nitrogen (N_2) that is flowed to showerhead 110 through valve 165 of POS 160.

[0051] A conformal film can be deposited via PEALD by performing multiple PEALD cycles in sequence. Each layer deposited by PEALD is very thin, typical being formed from a single monolayer of silicon-containing precursor, depositing a film of any substantial thickness can involve many cycles, and therefore may be relatively time consuming. In many cases, PEALD cycle times are comparable to valve and flow control device operating times, meaning that the time taken for such flow control devices to provide a steady state flow of silicon-containing precursor and/or other reactants becomes the limiting factor preventing desired further reductions in cycle time. A steady-state flow of reactants can be established by leaving flow control devices in their open positions, and to divert the flow of reactants to and from the reaction chamber as required by the timing requirements of an PEALD cycle.

[0052] Figs. 2 and 3 shows example timing diagrams for PEALD deposition of silicon oxide in a four-station chamber including divert of the silicon-containing precursor. Fig. 2 corresponds to concurrent dosing at four stations and Fig. 3 correspond to concurrent dosing at stations 1 and 2 followed by concurrent dosing at stations 3 and 4. It should be noted that the Figs. 2 and 3 are provided by way of example. The methods described herein may be implemented with any number of stations, including single station chambers. For multi-station chambers, silicon-containing precursor doses may be performed in parallel and/or sequentially across all or a subset of stations.

[0053] Further, deposition of other materials including silicon nitride, silicon oxynitride, silicon carbide, silicon oxycarbide, silicon oxycarbonitride, etc. may be performed by appropriate reactant choice. For example, the RF oxidizer operation in the timing diagrams may be replaced by RF nitridation.

[0054] In Fig. 2, displayed from top to bottom in the timing diagram is a schematic illustration of silicon-containing precursor delivery to each of 4 processing stations (labeled “Station 1” through “Station 4”) which is indicated by 4 traces 211, 212, 213, 214 showing precursor flow directed/redirected to each of the 4 processing stations. Schematically illustrated by a 5th trace 215 is precursor flow diverted to a divert flow path (i.e., not to the processing stations). These 5 traces (211, 212, 213, 214, and 215) represent a breakdown of the total precursor flow schematically illustrated by the top-most trace 210 in Fig. 2. The figure also schematically illustrates the timing of post-dose and post-RF purge gas flow—shown with trace 220/221 labeled “purge gases”—as well as the timing of oxidative plasma generation and reaction with adsorbed precursor—shown with trace 230 labeled “Oxidizer/RF.” In the example of Fig. 2, a single gas

delivery system like that shown in Fig. 1 may be used to flow precursor to each processing station in, for example, a 4-processing station configuration (possibly all contained within the same reaction chamber). In other embodiments, a dedicated gas delivery system for each processing station may be employed.

- 5 **[0055]** In the timing diagram of Fig. 2, the precursor dosing steps of the 4 ALD cycles are timed to coincide with one another. Thus, in step (i) (far left), substrates positioned at the 4 stations are simultaneously dosed with silicon-containing precursor which is allowed to adsorb onto the surface of each of the 4 wafers. For context, note that this could correspond to the opening of valve 164 in Fig. 1, while the other valves of the POS remain shut. After dosing step (i) concludes,
- 10 the totality of precursor flow is diverted as illustrated by the “Divert” trace 215 in the figure. During the post-dose purge step (ii) (shown by the “Purge gases” trace 220 in Fig. 2), during the reaction of adsorbed precursor via activation with RF-generated oxidative plasma in step (iii) (shown by the “Oxidizer/RF” trace 230 in Fig. 2), and during the post-RF purge (also shown by the “Purge gases” trace 220 in Fig. 2), there is total diversion of the silicon-containing precursor.
- 15 **[0056]** For context, it should be noted that the transition between the “dose” traces and the “divert” trace could correspond to the closing of valve 164 and the opening of valve 166 of the POS as shown by the “Divert to Vacuum” label of Fig. 1. Likewise, with valves 164 and 166 in these positions (164 closed and 166 opened), the purging steps (ii) and (iv) indicated by the “Purge gases” trace 220 in Fig. 1 may be accomplished by the opening of valve 165, 169 remaining closed
- 20 of course (and, in some embodiments, also accompanied by the opening of valves 162A and 162B for additional purge in the vicinity of the showerhead). The reaction via oxidative plasma step (iii) shown by the “Oxidizer/RF” trace 230 in Fig. 2 could correspond to the opening of valve 169 of the POS while the valve 165 (held open for the purge steps) is closed and 164 and 166 remain in their divert positions. It should be noted that the description of valve operation in reference to
- 25 Fig. 1 is an example.

[0057] Fig. 3 shows a timing diagram similar to that of Fig. 2, but with a parallel execution of a sequence of 4 ALD cycles where the flow of silicon-containing precursor from a common source initially doses wafers at processing stations 1 and 2, and afterwards is redirected to dose wafers at stations 3 and 4.

- 30 **[0058]** One aspect of the disclosure relates to methods of depositing material with increased growth rates by PEALD. The methods may be used for gap fill including in deep features and may result in fast closure of voids within the feature. Example applications include gap fill of slits in 3D NAND structures to isolate memory stacks, other 3D NAND structures, DRAM structures,

and shallow trench isolation (STI) structures. In some embodiments, the gaps may be high aspect ratio (HAR) gaps. Examples include gaps having aspect ratios of up to 35:1.

[0059] In some embodiments, the methods include controlling flow rates during the silicon-containing precursor dose. In some embodiments, the methods include allowing a silicon-containing precursor to flow into the station during at least part of the cycle that is after the dose. In some embodiments, the methods include controlling the timing sequence of the dose, purge, and RF operations. In some embodiments, the methods involve including low frequency RF (LFRF) component during the RF operation. According to various embodiments, any one or more of the above methods to increase growth rates is employed. The methods may increase growth rates by adding a CVD-type component to the ALD deposition.

[0060] Controlling flow rates during the silicon-containing precursor dose can involve reducing the total flow rate of the silicon-containing precursor and carrier gas by decreasing the carrier gas. This increases the concentration of silicon-containing precursor during the dose. As an example, a total flow rate per station may be 2000–4000 standard cubic centimeters per minute (sccm) of silicon-containing precursor and argon or another carrier gas. The silicon-containing precursor:carrier gas volumetric flow rate ratio during the dose may be, for example, 1:4–3:1 or 3:5–5:2. This can be compared to a ratio of 1:6–1:5 for a process without increased growth rate.

[0061] Allowing the silicon-containing precursor to flow into the chamber during a purge can be performed in various manners. For example, a valve to the showerhead may be left open with no divert of the silicon-containing precursor gas during at least part of time between the dose and RF operations. This allows silicon-containing precursor to continue to flow into the station.

[0062] In some embodiments, flow into the chamber may be controlled entirely at the silicon-containing precursor gas source. Fig. 4 shows a simplified schematic of a portion of a gas delivery system for delivering a silicon-containing precursor. Silicon-containing precursor gas source 402 may include, for example, a vapor-draw ampoule, a silicon-containing precursor source, and an inert gas source. The ampoule may be configured to receive silicon-containing precursor and an inert gas and to vaporize the silicon-containing precursor. A push gas may be supplied from push gas source 404 to push the silicon-containing precursor/inert gas mixture to a showerhead as shown. Three valves are depicted in the simplified schematic of Fig. 4. An outlet valve 412 controls the flow at the silicon-containing gas source. An inlet valve 416 to the showerhead controls flow into the station through its showerhead. Also shown is a divert line include a divert valve 414. The gas distribution system shown in Fig. 4 may be, for example, part of a gas distribution system as described above with respect to Fig. 1.

[0063] In certain embodiments, during at least a portion of the post-dose purge of an ALD cycle, the inlet valve 416 is open and with the divert valve 414 closed. This allows flow of the silicon-containing precursor gas to be controlled by outlet valve 412. Even after the outlet valve 412 is closed, some amount of silicon-containing precursor gas is in the line and can enter the station.

5 [0064] Figs. 5–8 provide examples of timing sequences for PEALD deposition of silicon oxide that include a CVD-type component. As described above with respect to Figs. 2 and 3, these sequences are not limited to deposition of silicon oxide or RF oxidation process. Deposition of other materials including silicon nitride, silicon oxynitride, silicon carbide, silicon oxycarbide, silicon oxycarbonitride, etc. may be performed by appropriate reactant choice. For example, the
10 RF oxidizer operation in the timing diagrams may be replaced by RF nitridation.

[0065] First, referring to Fig. 5, an example timing sequence for deposition of silicon oxide is shown. Five stages are shown in Fig. 5: two doses (D1 and D2), a post-dose purge (PDP), RF/oxidation, and post RF purge. The topmost trace shows the flow of Si-containing precursor and inert gas from a Si-containing precursor source outlet valve. An example is outlet valve 412
15 in Fig. 4. The second to topmost trace is the flow of Si-containing precursor and inert gas into a station. In the example of Fig. 4, the inert gas may come from the silicon-containing precursor gas source 402 in Fig. 4 and push gas source 404. Divert, purge gases, and RF/oxidizer are also shown.

[0066] During dose D1, the outlet valve from the Si-containing precursor gas source is open.
20 This is similar to the dose steps in Figs. 2 and 3. Once the outlet valve is closed, the flow of Si-containing precursor and inert gas stops from the Si-containing precursor gas source. Some amount of Si-containing precursor remains in the lines and the showerhead. During dose D2, this Si-containing precursor and inert gas continue to flow into the station. This is shown by the second to the topmost trace. Note that the while there is no continuing supply of Si-containing precursor
25 from the silicon-containing precursor gas source during D2, there may be inert gas supplied from an inert gas source in some embodiments. For example, in Fig. 4, inert gas may continue to flow from push gas source 404.

[0067] The sequence in Fig. 5 differs from that in Fig. 2, with the latter diverting flow of any Si-containing precursor after the dose. In the example of Fig. 5, any precursor remaining in the lines
30 is allowed to continue to flow into the station throughout the cycle with no divert. This includes during the post-dose purge, when purge gas is flowed, during the RF/oxidation stage, and during the post RF-purge. While the Si-containing precursor and inert gas continue to flow into the station during D2, the total flow and amount of Si-containing precursor in the flow decrease as there is no

new Si-containing precursor supplied from its source. In some embodiments, they may continuously decrease throughout the process.

[0068] In some embodiments, a divert may be used during a portion of the cycle. Fig. 6 shows another example of timing sequence that includes a D2 dose stage, as in Fig. 5. In the example of Fig. 6, the precursor flow is diverted for the RF/oxidation and post RF purge stages. In alternate embodiments, the divert may be started at the beginning of the PDP stage, or at any point during the PDP or RF/oxidation stages. In the examples of Figs. 5 and 6, the flow to the station includes silicon-containing precursor and inert gas that may be in the showerhead or in the line downstream of the divert valve 414.

[0069] Allowing the precursor to flow into the station after the D1 stage can facilitate providing a CVD-type component to the deposition process. Non-adsorbed precursor that is present in the station during the RF/oxidation stage will react in a CVD-type reaction. The amount of film deposited by the CVD-type component of the deposition process can be controlled by several parameters, including the presence, absence, and timing of D2 stage and a divert. More precursor will be present during the RF/oxidation stage using the timing diagram of Fig. 5 than using the timing diagram of Fig. 6. The presence, purge amount, and timing of the PDP stage may also be used to control the CVD-type component. To increase the CVD-type component, the amount of purge gas flowed during the PDP stage and/or the duration of the PDP stage can be reduced. In some embodiments, a post-dose purge may be omitted as shown in Fig. 7. In some embodiments, the D2 stage may be omitted, with the PDP stage beginning at the end of the D1 stage. Silicon-containing precursor may still flow to the station without divert as shown in the timing diagram of Fig. 8.

[0070] Another parameter to control the CVD-type component of the deposition is the time between the end of the D1 phase (or dose as referred to in Figs. 2 and 3) and the onset of the RF/oxidation. This time includes the D2 and/or PDP stages. Example times range from 5 milliseconds to 500 milliseconds. At the lower end of this range, the deposition has more of CVD-type component. At the higher end of the range, the deposition may be mostly ALD.

[0071] In some embodiments, during the oxidation or nitridation, the RF is supplied with a low frequency (LF) component as well as a high frequency (HF) component. In such embodiments, some of the deposited dielectric is sputtered from the feature top and re-deposited further within the feature. In some embodiments, the HF component is relatively high to obtain good conversion to an oxide, nitride, or other desired film. For example, the HF component may be between 4 kW–10 kW, divided among 4 stations, or 1 kW–2.5 kW per station. The amount of sputter and re-deposition may be tuned by controlling the LF power. In some embodiments, the LF power may

the same as or lower than the RF power. For example, the LF component may be 500 W–10 kW, divided among four stations, or 125 W – 2.5 kW per station. In some embodiments, the LF power is 500 W–5 kW, divided among four stations, or 125 W–1250 W per station. The per station power may be used for chambers having any number of stations. The HF frequency is about 13.56 or 27 MHz, while the LF frequency is between about 300–400 kHz.

[0072] The sputter and re-deposition may also be controlled by the flow rate of an inert gas such as argon (Ar). In some embodiments, a high argon Ar gas flow is used during the RF stage to increase the sputter and re-deposition. For example, an Ar flow rate of up to about 50 standard liters per minute (slm) for four stations, or up to 12.5 slm per station. At the lower end, an Ar flow rate of about 3.5–10 slm, or 875 sccm–2.5 slm may per station may be used during the RF stage. In some embodiments, an Ar flow into a station may be increased for the RF stage only.

[0073] In some embodiments, a CVD-type component is controlled using the RF purge (RFP). The oxidant or other co-reactant is not completely purged and allowed to remain in the chamber to react with the precursor in the next dose stage. This may be done in addition to or instead of the controlling the dose and/or PDP as described above. An example timing diagram is shown in Fig. 9.

[0074] Fig. 9 shows four stages in a cycle: dose, PDP, RF/oxidation, and RFP. In the example shown, the Si precursor and inert gas are at the station during the dose. In some embodiments, a divert (not shown) may be used to direct the precursor away from the station during the dose. In alternate embodiments, the precursor may be allowed to continue to flow into the chamber after the dose. In Figure 9, the oxidant is turned off and/or diverted at the same time as the plasma is extinguished. In alternate embodiments, it may be allowed to continue to flow into the chamber after the RF is off.

[0075] By appropriately controlling the timing of the RFP, a CVD-type component can be introduced during the subsequent dose. Purge flow and the amount and concentration of oxidizer (or other co-reactant) can also be controlled to affect the CVD-type component. By reducing the RFP time and/or increasing the amount and/or concentration of the oxidizer, oxidizer species are allowed to be present during the next dose phase where they react with precursor. The oxidizer species may be molecules and/or radicals or other afterglow plasma species. RF power (HF and/or LF) may also be increased to increase reactivity of the remaining species. Examples of RFP times range from 0.5 to 5 seconds. Examples of purge flows range from 5 lpm to 45 lpm (though will depend on the geometry and size of the particular reactor.)

[0076] In some embodiments, RFP time is less than 1 second. RFP times of 1 second or greater are likely to result in pure ALD. By contrast, at 0.1 second RFP with low purge flows, the CVD-

type component is high. In some embodiments, RFP time is less than 0.9 s, 0.8 s, 0.7 s, 0.6 s, 0.5 s, 0.4 s, 0.3, or 0.2 s.

[0077] Fig. 10 shows an example of deposition rate as a function of RFP time, holding all other process parameters constant. RF power of 5000 W was used. For the example process, deposition rate is higher for RFP time of about 0.3 s or below, then decreases with increasing RFP time. At 0.5 seconds, the process is at or close to pure ALD. RFP times that result in strong or weak CVD-type components or pure ALD depend on purge flows, amount of oxidizer, concentration of oxidizer, RF power, etc.

[0078] As described above, the methods may be implemented for a variety of applications, including memory and logic applications. In some embodiments, the methods may be used for gap fill. Fig. 11a shows an example of a feature 1101 including an unfilled gap 1103 between sidewalls 1115. In the figure, the width “a” and height “b” are indicated. Width may be a diameter. The aspect ratio (A/R) is given by b/a as indicated. The sidewalls 1115 are generally vertical. However, there may be some re-entrancy. Re-entrancy is narrowing from the bottom of the feature up. The inset 1110 shows that re-entrancy of a thickness “y” at a depth “x” in the feature. The sidewall surfaces may include one or more dielectric, conductive, or semi-conductive materials. In some embodiments, gap may be lined with a liner film.

[0079] In some embodiments, the methods are implemented to fill gaps during fabrication of a 3D NAND structure. For example, after etching slits in alternating silicon oxide/silicon nitride (ONON) layers, dielectric may be deposited in the slits. Fig. 11b shows an example of a structure including a gap 1103 between two memory stacks 1105. Each stack may include between 2 and 256 or more pairs of alternating oxide/nitride layers. According to various embodiments, the stacks may be lined with a layer, e.g., a polysilicon layer. During fill of the gap 1103, an LF component may be added to the RF oxidation operation. Adding a LF component mitigates crack formation in the ONON stack. In some embodiments, this is due to crosslinking and/or stress in the sputtered and re-deposited film.

[0080] The methods may be used for dielectric gap fill of any appropriate structure including DRAM structures and shallow trench isolation (STI) and deep trench isolation (DTI) structures for logic device fabrication. In some embodiments, during gap fill methods may include inhibition and/or etch operations. For example, a PEALD timing sequence as described above may be used for deposition operations in a deposition-etch-deposition (DED) process to fill a gap.

[0081] In some embodiments, the methods described herein are used to form closed voids in hole and trench structures. Fig. 11c shows an example of a void 1120 formed between two features. Dielectric material 1122 is deposited in the gap between the features with the CVD-type

component sufficient enough such that the void 1122 is formed as more dielectric material is deposited at the top of the feature. The techniques described above may be used to control the CVD-type component to form the void.

[0082] By forming a void (also referred to as an air gap) intra-level capacitance in semiconductor devices can be reduced. The methods may also be used to form air gaps in any appropriate context, including forming air gaps in MEMS devices. Examples of semiconductor structures include interconnects, conductive lines, or other conductive features. The method also may be implemented in any context in which air gaps capped by dielectric film between features are useful. Examples of structures include 3D NAND structures such as holes and slits, DRAM structures such as bitline structures, metal lines in back end of line (BEOL), logic gates, etc. The structures are characterized by having two or more adjacent features with an unfilled gap between the features. In many implementations, the features are conductive features, with the air gap to be formed providing very low k dielectric and reducing parasitic capacitance. However, the sidewall surfaces of the features may be any material including conductive, dielectric, or semiconducting surfaces or a combination of these. For example, the structure may be copper (Cu) lines coated with a silicon carbide (SiC) film. The dimensions of the structure will also depend on the particular application. For example, an incoming DRAM structure may have a gap 25–50 nm wide and 300–800 nm deep and an incoming 3D NAND structure may be 50–350 nm wide and 5–8 microns deep. However, the method is not limited to any particular structure dimension, feature composition, or sidewall surfaces. In some embodiments it may be implemented in applications in which other techniques for forming air gaps (such as deposition and removal of a sacrificial material) are difficult to implement.

[0083] A formed void can be characterized by placement and shape of the top of the void, shown at 1126. The void location can be tuned by the amount of RF time and/or sputter amount. The top of the void is generally some amount below the tops of the features to ensure the void remains closed during further processing. In some embodiments, the top of the void is rounded as shown in Fig. 11c. A rounded top helps prevent cracking.

[0084] The feature including a void can further be characterized by an indentation 1128 that forms a result of the deposition. Sputtering as described above widens the indentation angle 1130. In some embodiments, the indentation angle is greater than 50°, greater than greater than 55°, greater than 60°, greater than 65°, greater than 70°, greater than 75°, greater than 80°, or greater than 85°.

[0085] In some embodiments, the processes may include periodic exposure to an inhibition plasma. The inhibition plasma creates a passivated surface and increases a nucleation barrier of

the film. When the inhibition plasma interacts with material in the feature, the material at the bottom of the feature receives less plasma treatment than material located closer to a top portion of the feature or in field because of geometrical shadowing effects. Deposition at the top of the feature is selectively inhibited and deposition in lower portions of the feature proceeds with less inhibition or without being inhibited. As a result, bottom-up fill is enhanced, which creates a more favorable sloped profile that mitigates the seam effect and prevents void formation. Halogen-containing plasmas can be effective inhibition plasmas. For example, for some applications, a plasma generated from nitrogen trifluoride (NF_3) may provide an inhibition effect in a substantially reduced time compared to a plasma generated from molecular nitrogen (N_2). However, halogen-containing plasmas may also act as an etchant. For example, while performing an inhibition, an atom hitting a surface with low energy can act as an inhibitor while a high energy atom can remove material. Because the plasma has an energy distribution, some component of the plasma may hit near the top of the feature and etch. Any dielectric etched is replaced during deposition. If underlying material (e.g., polysilicon (poly Si), a metal oxide, etc.) is removed, it is not replaced and can affect device performance.

[0086] In some embodiments, the methods are implemented to form a protective film at the top of a gap. This film may be referred to as a “helmet” at the top of the gap and can protect against damage from inhibition plasma. Fig. 12a shows an example of a process sequence that may be used in accordance with the disclosed embodiments. In the example of Fig. 12a, multiple ALD operations are shown. Any one or more of these may use one or more of the techniques described above to include a CVD-type component.

[0087] The process sequence in Fig. 12a includes deposition of a protective film prior to exposure to an inhibition plasma. Other operations (e.g., soak, passivation) may be omitted in certain embodiments and operations may be added in certain embodiments. In the example process sequence of Fig. 12a, one or more wafers undergo gap fill. The process may begin with a soak after being provided to a deposition chamber. This can be useful, for example, to remove particles or another pretreatment. Then, $n1$ cycles of ALD deposition of protective film are performed. Further details of the protective liner ALD are discussed below. After the protective film is deposited, n inhibition blocks are performed, with the operations of one inhibition block shown. The first operation of the inhibition block is the inhibition plasma, which is a surface treatment. As discussed above, the plasma may include halogen species including anion and radical species such as F^- , Cl^- , I^- , Br^- , fluorine radicals, etc. Other inhibition plasmas may be used, with a protective film providing protection from any plasma that can damage a structure. For example, plasmas generated from molecular nitrogen (N_2), molecular hydrogen (H_2), ammonia (NH_3),

amines, diols, diamines, amino alcohols, thiols or combinations thereof may be used as inhibition plasmas. If conditions such as temperature, RF power, and sensitivity of the underlying material are such that plasma damage may occur with these, the protective film may be used. In some embodiments, a halogen-containing gas (e.g., NF_3) is used. It may be heavily diluted with another gas, such as oxygen (O_2) to control the inhibition and prevent etching. For example, in some

5 embodiments, an oxidant:halogen volumetric flow ratio may be at least 5:1 or at least 10:1.

[0088] When the inhibition plasma interacts with material in the feature, the material at the bottom of the feature receives less plasma treatment than material located closer to a top portion of the feature or in field because of geometrical shadowing effects. As a result, deposition at the top of the feature is selectively inhibited and deposition in lower portions of the feature proceeds with less inhibition or without being inhibited. In Fig. 12a, the next operation in the inhibition block is $n2$ cycles of ALD fill. The dielectric material is deposited selectively at the bottom of the feature. The inhibition plasma and the $n2$ cycles of ALD fill together make a growth cycle. A growth cycle can be repeated $n3$ times to continue filling the feature with intermittent inhibition operations when the inhibition effect diminishes. The number of growth cycles in an inhibition block may depend on the re-entrancy of the feature. Features that exhibit more re-entrancy may use a longer inhibition time or multiple inhibition blocks. In the example of Fig. 12a, the inhibition block ends with a passivation operation. This is a surface treatment that removes residual inhibitor and can also densify the deposited film. In some embodiments, an oxygen plasma is used. In

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20 some embodiments, a passivation cycle may be omitted.

[0089] One or more additional inhibition blocks, including growth cycle and passivation, may be performed for a total of n inhibition blocks. The number of inhibition blocks depends on how much material is used to fill the feature. Inhibition plasma, ALD, and passivation conditions may be changed from inhibition block to inhibition block to fill the feature. For example, an inhibition plasma duration may be 20 seconds until the bottom quarter of the feature is filled (inhibition block 1), then changed to 5 seconds for the middle 50% of the structure (inhibition block 2), etc.

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[0090] When the feature is nearly filled, inhibition may no longer be necessary, and the fill can be completed with $n4$ cycles of ALD fill. In some embodiments, a cap or overburden layer of dielectric may then be deposited. Plasma enhanced chemical vapor deposition (PECVD) may be used at this stage for a fast deposition.

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[0091] In some embodiments, a protective film is deposited using a CVD-type component as described above. Fig. 12b shows an example of a 3D NAND structure 1250 with poly Si 1218 at the top of an ONON stack. At 1251, the poly Si 218 is vulnerable if exposed to an inhibition plasma used to fill the gap 206. At 1253, a protective film 1260 is shown. In particular

embodiments, an inlet valve controlling silicon-containing precursor to the showerhead is open and with no divert valve closed. This allows flow of the silicon-containing precursor gas to be controlled by an outlet valve of the silicon-containing precursor source. As discussed above, with respect to Fig. 4, after the outlet valve is closed, some amount of silicon-containing precursor gas is in the line and can enter the station. In the same or other embodiments, LF power is used during formation of the protective film.

[0092] Allowing silicon-containing precursor to flow into the station during deposition of the protective liner allows the protective film to be deposited much more quickly than an ALD process without a CVD-type component. Providing an LF component can also improve deposition and provide a film with higher uniformity and higher refractive index (RI) than an HF-only deposited film. See Fig. 13, which shows thickness non-uniformity (NU) and refractive index (RI) for films deposited using a silicon-containing precursor/purge/N₂ plasma/purge sequence at 10 Torr by PEALD with 1000 W HF + 1500 W LF (triangle) and with 1000 W HF only. NU is significantly lower and RI higher for the HF + LF deposited film. RI is inversely correlated with etch rate. Thus, the HF + LF deposited film is more etch resistant. Deposition rate is also shown at multiple pressures and is higher for the HF + LF deposited film.

[0093] The protective film may be formed from a material that is relatively etch resistant to the inhibition plasma. Examples of protective liners include silicon nitrides, silicon carbides, and silicon oxides (including silicon oxynitrides, silicon oxycarbides, silicon carbon nitrides, etc.). Any material may be used that is compatible with the inhibitor gas and has a high selectivity (low etch rate) in the inhibitor compared to the underlying film.

[0094] Silicon oxide has lower resistance than silicon nitride or silicon carbide to fluorine-based or similar plasmas and may be used only in certain circumstances. These can include one or more of the following: the inhibition plasma being relatively weak, the inhibition plasma applied only for a short duration, and the feature dimensions allowing a fairly large amount of protective film deposited without pinching off the feature during the fill.

[0095] Silicon nitride (SiN) may be deposited using a N₂ plasma or other nitrogen-containing plasma. In some embodiments, no oxidant is used during SiN deposition. However, at certain process conditions, ambient conditions may lead to the formation of silicon oxide rather than silicon nitride. The use of LF during SiN protective film deposition results in formation of a nitride rather than an oxide. Referring to Fig. 13, for example, the HF-only deposition has a RI that indicates a significant portion of the film is an oxide rather than a nitride. The HF/LF-deposited film has an RI consistent with that of a nitride. LF RF power may be limited to avoid excessive sputtering. In some embodiments, the amount of LF power is between 1 and 2 kW for four stations

(or 250 W to 500 W per station). SiN films may also be deposited by using extremely low pressures at which little oxygen is present and/or using longer RF times. Silicon carbides may be deposited using a carbon-containing co-reactant (e.g., reacting silane with methane).

[0096] In many embodiments, the material is sacrificial and removed during inhibition and so not particularly limited. The depth of protective film may be determined by determining the depth that the inhibition plasma damages the underlying layer in the absence of the protective liner. This may be done experimentally, by modelling, or a combination of these. The protective film may be deposited to a thickness such that it will protect the underlying layer through the inhibition plasmas but be removed by the end of the last inhibition plasma. This can be determined experimentally and/or from known etch rates. Example thicknesses may range from tens to hundreds of Angstroms. In some embodiments, some amount of protective film may remain after gap fill. In such cases, a separate removal process may be implemented prior to filling the portion of the gap where the protective liner remains. In some embodiments, remaining protective film may be left in the device. In some embodiments, deposition of the protective film may be performed more than once – for example, every m inhibition blocks.

[0097] A CVD-type component in the PEALD process can facilitate depositing the protective liner preferentially at the top of the structure rather than conformally. As described above, in some embodiments, the silicon-containing precursor is allowed to flow throughout the process, or otherwise as described with respect to Figs. 5–8. In some embodiments, LF RF plasma is used. Further, pressure may be kept relatively low (e.g., less than 20 Torr, or less than 15 Torr) to further facilitate non-conformal deposition of the protective liner.

[0098] Deposition of the protective liner by the methods described herein can result in the thickness tapering down from the top of the gap to its deepest point. Etch rates decrease with increasing depth such that a tapered protective liner may be removed without etching the underlying layer.

[0099] Fig. 14 presents a process flow diagram for a single PEALD cycle that may be implemented as part of deposition of a protective liner or for any of the other ALD operations shown in Fig. 12a. In an operation 1402, the substrate is exposed to a silicon-containing precursor, to adsorb the precursor onto the surface of the feature. This operation may be self-limiting. In some embodiments, the precursor adsorbs to less than all the active sites on the surface of the feature. In an operation 1404, the process chamber is optionally purged to remove any unadsorbed silicon-containing precursors. As described above, in some embodiments, the substrate continues to be exposed to a flow including the silicon-containing precursor during the purge.

[0100] In an operation 1406, the substrate is exposed to a plasma generated from a co-reactant. Examples include O₂ and/or N₂O to form a silicon oxide layer or silicon oxynitride layer, nitrogen (N₂) or ammonia (NH₃) to form a silicon nitride layer, methane (CH₄) to generate a silicon carbide layer, etc. As described above, in some embodiments, the substrate continues to be exposed to a flow including the silicon-containing precursor during this operation. Also as described above, in the same or other embodiments, the plasma is an RF-generated plasma generated using LF and HF voltages.

[0101] In operation 1408, the process chamber is optionally purged to remove byproducts from the reaction between the silicon-containing precursor and the co-reactant. As described above, in some embodiments, the substrate continues to be exposed to a flow including the silicon-containing precursor during this operation. Operations 1402 through 1408 are repeated for a number of cycles to deposit the silicon-containing layer to a desired thickness in the feature.

[0102] It should be noted that the processes described herein are not limited to a particular reaction mechanism. Thus, the process described with respect to Fig. 14 includes all deposition processes that use sequential exposures to silicon-containing precursors and conversion plasmas, including those that are not strictly self-limiting. The process includes sequences in which one or more gases used to generate a plasma is continuously flowed throughout the process with intermittent plasma ignitions.

[0103] Another aspect of the disclosure relates to a method of forming a silicon oxynitride layer by PEALD. As used herein, silicon oxynitride (SiON) refers to SiO_xN_y wherein x and y are numbers greater than zero. Fig. 15 is a process flow diagram for a method of forming a silicon oxynitride layer. First, in an operation 1502, process conditions are stabilized for SiO deposition. This involves changes gas flows and stabilizing flow rates into a chamber or station of a chamber as described above. In some embodiments, it can involve stabilizing a chamber pressure. As discussed further below, the substrate temperature and/or chamber pressure may be the same as in a previous operation and may not need to be stabilized.

[0104] Next, x PEALD cycles using a silicon-containing precursor and oxygen-containing (O-containing) co-reactant are performed in an operation 1504. As described further below, the number of cycles x may be determined by the amount of oxygen to be incorporated into the deposited film and if the deposited film is a homogenous SiON film or a layered SiO/SiN film. In some embodiments, x is an integer from 1 to 15, or 1 or 10, or 1 to 7, including endpoints.

[0105] Once the x cycles have been performed, process conditions with the chamber are stabilized for SiN deposition in an operation 1506. Operation 1506 includes changing and stabilizing gas flows and may further include changing chamber pressure. As discussed further

below, the substrate temperature and/or chamber pressure may be the same as in a previous operation and may not need to be stabilized.

[0106] Next, y PEALD cycles using a silicon-containing precursor and nitrogen-containing (N-containing) co-reactant are performed in an operation 1508. The N-containing reactant typically does not contain any oxygen, with no O-containing reactants used during operation 1508. As described further below, the number of cycles y may be determined by the amount of nitrogen to be incorporated into the deposited film and if the deposited film is a homogenous SiON film or a layered SiO/SiN film. In some embodiments, y is an integer from 1 to 15, or 1 or 10, or 1 to 7, including endpoints.

[0107] In an operation 1501, operations 1502–1508 are then repeated one or more times to build up the film thickness. According to various embodiments, the entire process shown in Fig. 15 is performed in the same chamber, and in some embodiments, the same station of a multi-station chamber. In some embodiments, different stations may be used for different process operations.

[0108] Fine control of the incorporation of nitrogen into a SiON film can be used to control the dry etch rate of the film, with more nitrogen generally resulting a more etch resistant film. The ratio of $x:y$ can be used to tune the relative amounts of O and N in the film. In some embodiments, each of the number of cycles x and y and the total number of cycles $x + y$ before repeating the SiO and SiN depositions is kept low enough that the deposited film is a homogenous SiON film. In embodiments in which SiO and SiN are discrete alternating layers, the numbers of cycles can be increased. According to various embodiments, the ratio $x:y$ may range from 1:10 to 10:1. Other ratios may be used.

[0109] In some embodiments, chamber pressure is changed in operations 1502 and 1506. In the other embodiments, the same chamber pressure is used. Plasma duration during the PEALD cycles of operation 1508 (using a nitrogen-based plasma) are much longer than those of operation 1504 (using an oxygen-based plasma). For example, it be at least twice as long, at least 3 times as long, at least 5 times as long, or at least 7 times as long. According to various embodiments, the silicon-containing precursor used in operation 1504 may be the same or different as used in operation 1508.

[0110] According to various embodiments, operation 1502 may involve stopping a flow of nitrogen (N_2) or other non-oxygen-containing nitrogen-containing reactant(s) from entering a processing station. This can involve stopping or diverting flow from a manifold, for example. It may further involve starting a flow of oxidant (e.g., O_2 and/or N_2O) from a manifold with divert. It may further involve starting a flow of silicon-containing precursor to the processing station. This can involve opening a valve from a silicon-containing precursor gas source, for example valve

412 in Fig. 4, without divert. In some embodiments, the valve may be opened or left open during an RF purge operation of operation 1508.

[0111] According to various embodiments, operation 1506 may involve stopping a flow of oxygen (O_2) or other oxygen reactant(s) from entering a processing station. This can involve stopping or diverting flow from a manifold, for example. It may further involve starting a flow of non-oxygen-containing nitrogen-containing reactant (e.g., N_2) from a manifold with divert. It may further involve starting a flow of silicon-containing precursor to the processing station. This can involve opening a valve from a silicon-containing precursor gas source, for example valve 412 in Fig. 4, without divert. In some embodiments, the valve may be opened or left open during an RF purge operation of operation 1504.

[0112] Fig. 16A shows refractive index (RI) and density, which inversely correlate to etch rate, for films deposited using various numbers of SiN cycles in a method according to Fig. 15. As can be seen from Fig. 16A, the RI and the density (and thus the dry etch rate) can be tuned with a fairly broad window by increasing or decreasing the number of SiN cycles relative to total SiN and SiO cycles.

[0113] Fig. 16B shows FTIR spectra for four 3 kÅ thick films – one SiO₂ film, one SiN film, one SiON film deposited using a method as shown Fig. 15 with 3 oxidant cycles to 7 nitridant cycles for each iteration, and a SiON film deposited using a method as shown in Fig. 15 with 7 oxidant cycles to 3 nitridant cycles for each iteration. For the films deposited using both O₂/Ar plasma and N₂/Ar plasma operations, the peaks are between the SiO₂ and SiN peaks, indicating that the films are mixed SiON films and not layered SiO₂ / SiN films.

[0114] The SiON films described herein may be used in a variety of applications including as spacers in patterning schemes. For example, a SiON film may be deposited over a patterned core material that overlies a target layer to be etched. In some embodiments, the patterned core material may be a carbon-based structure such as an amorphous carbon structure. The SiON film may be deposited to conformally coat the patterned core material. Fig. 16C shows an example of a SiON film 1620 having a tuned composition and dry etch rate conformally deposited on a patterned layer 1613. Examples of materials for the patterned layer 1613 include amorphous carbon, amorphous silicon, and photoresist. The conformal film 1620 is directionally etched to form spacers 1621 flanking the patterned first layer 1613. The patterned first layer 1613 is selectively removed to leave free-standing spacers 1621. The spacers 221 may provide a mask with an even smaller CD for forming features with an even smaller pitch in the underlying layer 1605. As the SiON film 1620 may undergo several precise etch operations in a pattern transferring scheme, being able to tune the dry etch rate as described above is advantageous.

[0115] For depositing a silicon-containing film as described above with reference to Figs. 1–16C, one or more silicon-containing precursors may be used. The silicon-containing reactant may react with a co-reactant to form the silicon-containing film (e.g., SiO₂, SiN, SiON, SiC, SiOC, etc.) Silicon-containing precursors suitable for use in accordance with disclosed embodiments include polysilanes (H₃Si-(SiH₂)_n-SiH₃), where $n \geq 0$. Examples of silanes are silane (SiH₄), disilane (Si₂H₆), and organosilanes such as methylsilane, ethylsilane, isopropylsilane, t-butylsilane, dimethylsilane, diethylsilane, di-t-butylsilane, allylsilane, *sec*-butylsilane, hexylsilane, isoamylsilane, t-butylsilane, di-t-butylsilane, and the like.

[0116] A halosilane includes at least one halogen group and may or may not include hydrogens and/or carbon groups. Examples of halosilanes are iodosilanes, bromosilanes, chlorosilanes, and fluorosilanes. Specific chlorosilanes are tetrachlorosilane, trichlorosilane, dichlorosilane, monochlorosilane, chloroallylsilane, chloromethylsilane, dichloromethylsilane, chlorodimethylsilane, chloroethylsilane, t-butylchlorosilane, di-t-butylchlorosilane, chloroisopropylsilane, chloro-*sec*-butylsilane, t-butyl dimethylchlorosilane, hexyldimethylchlorosilane, and the like.

[0117] An aminosilane includes at least one nitrogen atom bonded to a silicon atom, but may also contain hydrogens, oxygens, halogens, and carbons. Examples of aminosilanes are mono-, di-, tri- and tetra-aminosilane (H₃Si(NH₂), H₂Si(NH₂)₂, HSi(NH₂)₃ and Si(NH₂)₄, respectively), as well as substituted mono-, di-, tri- and tetra-aminosilanes, for example, t-butylaminosilane, methylaminosilane, tert-butylsilanamine, bis(tert-butylamino)silane (SiH₂(NHC(CH₃)₃)₂) (BTBAS), tert-butyl silylcarbamate, SiH(CH₃)-(N(CH₃)₂)₂, SiHCl-(N(CH₃)₂)₂, (Si(CH₃)₂NH)₃ and the like. A further example of an aminosilane is trisilylamine (N(SiH₃)). In some embodiments, an aminosilane that has two or more amine groups attached to the central Si atom may be used. These may result in less damage than aminosilanes having only a single amine group attached.

[0118] Further examples of silicon-containing precursors include trimethylsilane (3MS); ethylsilane; butasilanes; pentasilanes; octasilanes; heptasilane; hexasilane; cyclobutasilane; cycloheptasilane; cyclohexasilane; cyclooctasilane; cyclopentasilane; 1,4-dioxo-2,3,5,6-tetrasilacyclohexane; diethoxymethylsilane (DEMS); diethoxysilane (DES); dimethoxymethylsilane; dimethoxysilane (DMOS); methyl-diethoxysilane (MDES); methyl-dimethoxysilane (MDMS); octamethoxydodecasiloxane (OMODDS); tert-butoxydisilane; tetramethylcyclotetrasiloxane (TMCTS); tetraoxymethylcyclotetrasiloxane (TOMCTS); triethoxysilane (TES); triethoxysiloxane (TRIES); and trimethoxysilane (TMS or TriMOS).

[0119] In some implementations silicon-containing precursors may include siloxanes or amino-

- group-containing siloxanes. In some embodiments, siloxanes used herein may have a formula of $X(R^1)_aSi-O-Si(R^2)_bY$, where a and b are integers from 0 to 2, and X and Y independently can be H or NR^3R^4 , where each of R^1 , R^2 , R^3 and R^4 is hydrogen, unbranched alkyl, branched alkyl, saturated heterocyclic, unsaturated heterocyclic groups, or combinations thereof. In some
- 5 embodiments, when at least one X or Y is NR^3R^4 , R^3 and R^4 , taken together with the atom to which each are attached, form a saturated heterocyclic compound. In some embodiments, the silicon-containing precursors are pentamethylated amino group containing siloxanes or dimethylated amino group containing siloxanes. Examples of amino group containing siloxanes include: 1-diethylamino 1,1,3,3,3,-pentamethyl disiloxane, 1-diisopropylamino-1,1,3,3,3,-
- 10 pentamethyl disiloxane, 1 dipropylamino-1,1,3,3,3,-pentamethyl disiloxane, 1-di-n-butylamino-1,1,3,3,3,-pentamethyl disiloxane, 1-di-sec-butylamino-1,1,3,3,3,-pentamethyl disiloxane, 1-N-methylethylamino 1,1,3,3,3,-pentamethyl disiloxane, 1-N-methylpropylamino-1,1,3,3,3,-pentamethyl disiloxane, 1 N-methylbutylamino -1,1,3,3,3,-pentamethyl disiloxane, 1-t-butylamino -1,1,3,3,3,-pentamethyl disiloxane, 1-piperidino-1,1,3,3,3,-pentamethyl disiloxane, 1-
- 15 dimethylamino-1,1-dimethyl disiloxane, 1-diethylamino-1,1-dimethyl disiloxane, 1-diisopropylamino-1,1-dimethyl disiloxane, 1-dipropylamino-1,1-dimethyl disiloxane, 1-di-n-butylamino-1,1-dimethyl disiloxane, 1-di-sec butylamino-1,1-dimethyl disiloxane, 1-N-methylethylamino-1,1-dimethyl disiloxane, 1-N methylpropylamino-1,1-dimethyl disiloxane, 1-N-methylbutylamino -1,1-dimethyl disiloxane, 1 piperidino-1,1-dimethyl disiloxane, 1-t-
- 20 butylamino -1,1-dimethyl disiloxane, 1-dimethylamino- disiloxane, 1-diethylamino- disiloxane, 1-diisopropylamino- disiloxane, 1-dipropylamino- disiloxane, 1-di-n-butylamino- disiloxane, 1-di-sec-butylamino- disiloxane, 1-N methylethylamino- disiloxane, 1-N-methylpropylamino-disiloxane, 1-N-methylbutylamino – disiloxane, 1-piperidino- disiloxane, 1-t-butylamino disiloxane, and 1-dimethylamino-1,1,5,5,5,-pentamethyl disiloxane.
- 25 **[0120]** In addition to a silicon-containing precursor, one or more other gases, including inert gases such as argon, nitrogen, helium, hydrogen, or combinations thereof, may also be flowed. In various embodiments, argon gas may be introduced using a flow rate between about 1 slm and about 20 slm. In some embodiments, nitrogen gas is introduced using a flow rate between about 0 slm and about 30 slm (with the understanding that 0 slm refers to no nitrogen gas being flowed).
- 30 In some embodiments, hydrogen gas is introduced using a flow rate between about 0 slm and about 5 slm (with the understanding that 0 slm refers to no hydrogen gas being flowed).
- [0121]** Plasma energy may be provided to activate the second reactant into ions and radicals and other activated species, which react with the adsorbed layer of adsorbed precursor and any precursor present in the vapor phase. In various embodiments, the plasma is an in-situ plasma,

such that the plasma is formed directly above the substrate surface in the chamber. The in-situ plasma may be ignited at a power per substrate area between about 0.2122 W/cm² and about 2.122 W/cm², or between about 0.4421 W/cm² and about 1.7684 W/cm². For example, the power for a single wafer may range from about 150W to about 6000W, or from about 500W to about 6000W, or from about 600W to about 6000W, or from about 800 W to about 4000W, or from about 310W to about 1250W. The power for four 300mm wafers may range from about 150W to about 6000W, or from about 1250W to about 5000W. Ranges described herein are inclusive of their end points.

[0122] Plasmas for ALD processes may be generated by applying a radio frequency (RF) field to a gas using two capacitively coupled plates. Ionization of the gas between plates by the RF field ignites the plasma, creating free electrons in the plasma discharge region. These electrons are accelerated by the RF field and may collide with gas phase reactant molecules. Collision of these electrons with reactant molecules may form radical species that participate in the deposition process. It will be appreciated that the RF field may be coupled via any suitable electrodes.

[0123] In this application, the terms “semiconductor wafer,” “wafer,” “substrate,” “wafer substrate,” and “partially fabricated integrated circuit” are used interchangeably. One of ordinary skill in the art would understand that the term “partially fabricated integrated circuit” can refer to a silicon wafer during any of many stages of integrated circuit fabrication thereon. A wafer or substrate used in the semiconductor device industry typically has a diameter of 200 mm, or 300 mm, or 450 mm. Unless otherwise stated, the processing details recited herein (e.g., flow rates, power levels, etc.) are relevant for processing 300 mm diameter substrates, or for treating chambers that are configured to process 300 mm diameter substrates and can be scaled as appropriate for substrates or chambers of other sizes.

[0124] Fig. 17 depicts a schematic illustration of an embodiment of a plasma enhanced atomic layer deposition (PEALD) process station 1700 having a process chamber body 1702. The PEALD process station 1700 may be suitable for processing substrates in a low-pressure environment in some embodiments. In some embodiments, one or more hardware parameter values of PEALD process station 1700, including those discussed in detail below may be adjusted programmatically by one or more computer controllers 1750.

[0125] The PEALD process station 1700 fluidly communicates with reactant delivery system 1701a for delivering process gases to a distribution showerhead 1706. The reactant delivery system 1701a may include one or more manifolds as described above with reference to Fig. 1 or below with reference to Fig. 18, mixing vessels, mass flow controllers, liquid flow controllers and valves. In various embodiments, delivery of one or more process gases to the showerhead 1706 or to the process chamber 1702 may be varied across cycles. For example, the duration of dosing

one or more process gases may be varied. In disclosed embodiments, a controller 1750 may control the delivery of one or more process gases by controlling one or more inlet valves, divert valves, and outlet valves.

[0126] Showerhead 1706 distributes process gases toward substrate 1712. In the embodiment shown in Fig. 17, the substrate 1712 is located beneath showerhead 1706 and is shown resting on a pedestal 1708. Showerhead 1706 may have any suitable shape and may have any suitable number and arrangement of ports for distributing process gases to substrate 1712. Optionally, pedestal 408 may be lowered and/or raised during portions the process to modulate process pressure, reactant concentration, plasma density, etc.

[0127] The showerhead 1706 and/or pedestal 1708 electrically communicate with a high frequency radio frequency (HFRF) power supply 1714a and a low frequency radio frequency (LFRF) through a matching network 1716 for powering a plasma. In some embodiments, the plasma energy may be controlled by controlling one or more of a process station pressure, a gas concentration, an RF source power, an RF source frequency, and a plasma power pulse timing. Such parameter values may be varied from ALD cycle to ALD cycle in a multi-cyclic ALD process as described herein. For example, LFRF power supply 1714b and matching network 1716 may be operated at any suitable power to for desired sputtering effect during one or more ALD cycles. Examples of suitable powers are included above. Example low-frequency RF frequencies may include, but are not limited to, frequencies between 50 kHz and 500 kHz. Example high-frequency RF frequencies may include, but are not limited to, frequencies between 1.8 MHz and 2.45 GHz.

[0128] In some embodiments, the plasma may be monitored in-situ by one or more plasma monitors. In one scenario, plasma power may be monitored by one or more voltage, current sensors (e.g., VI probes). In another scenario, plasma density and/or process gas concentration may be measured by one or more optical emission spectroscopy sensors (OES). In some embodiments, one or more plasma parameter values may be programmatically adjusted based on measurements from such in-situ plasma monitors. For example, an OES sensor may be used in a feedback loop for providing programmatic control of plasma power. It will be appreciated that, in some embodiments, other monitors may be used to monitor the plasma and other process characteristics. Such monitors may include, but are not limited to, infrared (IR) monitors, acoustic monitors, and pressure transducers.

[0129] In some embodiments, instructions for a controller 1750 may be provided via input/output control (IOC) sequencing instructions. In one example, the instructions for setting conditions for a process phase may be included in a corresponding recipe phase of a process recipe. In some cases, process recipe phases may be sequentially arranged, so that all instructions for a

process phase are executed concurrently with that process phase. In some embodiments, instructions for setting one or more reactor parameter values may be included in a recipe phase. For example, a first recipe phase may include instructions for setting a flow rate of an inert and/or a reactant gas (e.g., the first precursor such as silane), instructions for setting a flow rate of a carrier gas (such as nitrogen or argon), and time delay instructions for the first recipe phase. A second, subsequent recipe phase may include instructions for modulating or stopping a flow rate of an inert and/or a reactant gas, and instructions for modulating a flow rate of a carrier or purge gas and time delay instructions for the second recipe phase. A third recipe phase may include instructions for setting a flow rate of an inert and/or reactant gas which may be the same as or different from the gas used in the first recipe phase (e.g., the second precursor such as oxygen), instructions for setting a plasma HFRF power, instructions for setting a plasma LFRF power, instructions for modulating a flow rate of a carrier gas which may be the same as or different from the flow rate in the first recipe phase, plasma conditions, and time delay instructions for the third recipe phase. A fourth recipe phase may include instructions for modulating or stopping a flow rate of an inert and/or a reactant gas, instructions for modulating the flow rate of a carrier or purge gas, and time delay instructions for the fourth recipe phase. A fifth recipe phase may include instructions for setting a flow rate of an inert and/or reactant gas (e.g., oxygen and/or argon), instructions for setting a different or same plasma LFRF and/or HFRF power, instructions for modulating a flow rate of a carrier gas, plasma conditions, and time delay instructions for the fifth recipe phase for performing an intermittent plasma treatment. In some cases, the recipe phase may also include instructions for pulsing the plasma between ON and OFF states. More recipe phases may also be used. It will be appreciated that these recipe phases may be further subdivided and/or iterated in any suitable way within the scope of the present disclosure.

[0130] In some embodiments, pedestal 1708 may be temperature controlled via heater 1710. Further, in some embodiments, pressure control for process station 1700 may be provided by butterfly valve 1718. As shown in the embodiment of Fig. 17, butterfly valve 1718 throttles a vacuum provided by a downstream vacuum pump (not shown). However, in some embodiments, pressure control of process station 1700 may also be adjusted by varying a flow rate of one or more gases introduced to the process station 1700. The process station 1700 may include a control 1750 for controlling example recipes as described above.

[0131] In some implementations, a controller 1750 is part of a system, which may be part of the above-described examples. Such systems can comprise semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems

may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the “controller,” which may control various components or subparts of the system or systems. The controller 1750, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases and/or variation of different dose times for delivery of process gases including diversion of one or more gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, RF generator settings and/or variation of RF power settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

[0132] Broadly speaking, the controller 1750 may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller 450 in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0133] The controller 1750, in some implementations, may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller 1750 may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer.

In some examples, the controller 1750 receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller 1750 is configured to interface with or control. Thus as
5 described above, the controller 1750 may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer)
10 that combine to control a process on the chamber.

[0134] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an
15 atomic layer deposition (ALD) chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0135] As noted above, depending on the process step or steps to be performed by the tool, the
20 controller 1750 might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0136] The methods described herein may be implemented using a multi-station or single station substrate processes apparatus. In some embodiments of a multi-station substrate processing apparatus, control and/or supply of various process inputs (e.g., process gases, plasma power, gases for plasma generation, reactants, film precursors, heater power, etc.) may be distributed from shared sources to the plurality of processing stations within the multi-station apparatus. For
25 example, in some embodiments, a shared source of RF power may supply RF power for plasma generation within two or more processing stations. In another example, a shared gas distribution manifold may supply process gases to two or more processing stations. Some non-limiting example embodiments of multi-station processing tools are described below.

[0137] Fig. 18 schematically shows an example substrate processing apparatus 3840, which

includes a plurality of processing stations 3842 in a common low-pressure reaction chamber. By maintaining each station in a low-pressure environment, defects caused by vacuum breaks between film deposition processes may be avoided. In the example shown in Fig. 18, each processing station 3842 is configured to deposit a silicon-containing film as described above. In the

5 embodiment depicted in Fig. 18, process gases for each processing station 3842 are supplied by a common mixing vessel 3844 for blending and/or conditioning process gases prior to delivery. In some embodiments, mixing vessel 3844 may be temperature controlled. Process gases, including film precursors (such as silicon-containing film precursor) and possibly other reactants in a carrier gas, as well as gases for plasma support, may be supplied from a plurality of process gas delivery

10 lines, valves, and manifolds. For example, Fig. 18 depicts a manifold A including a silicon-precursor/argon mixture and argon (as the carrier gas) fluidly communicating with a delivery line 3845; a manifold B including nitrogen and argon (again, serving as a carrier gas) fluidly communicating with an delivery line 3847; and a manifold C including oxygen gas (O_2) and/or nitrous oxide (N_2O), helium, and/or argon (the latter two as carrier gases) fluidly communicating

15 with delivery line 3848. It should be appreciated that other suitable arrangements and chemistries (as described above) are included within the scope of the present disclosure, and that various ALD-based film deposition chemistries and multi-substrate apparatuses and arrangements may benefit from the process timing sequences disclosed herein. In some embodiments, separate mixing vessels may be employed, separating incompatible reactants and precursors.

20 **[0138]** While Fig. 18 depicts a multi-station substrate processing apparatus having four processing stations within a single reaction chamber, other configurations may have a greater or lesser number of processing stations within a single reaction chamber. Thus, for example, in some embodiments, a multi-station substrate processing apparatus may have 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, or 16, or more processing stations per reaction chamber; or a number of processing

25 stations per reaction chamber within a range defined by any pair of the foregoing numbers of processing stations per reaction chamber: e.g., 2 to 6 processing stations per reaction chamber, 4 to 8 processing stations per reaction chamber, 8 to 16 processing stations per reaction chamber, etc.

[0139] In other embodiments, a substrate processing apparatus may have just a single processing

30 station per reaction chamber.

[0140] The apparatus/process described herein may be used in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of semiconductor devices, displays, LEDs, photovoltaic panels and the like. Typically, though not necessarily, such tools/processes will be used or conducted together in a common fabrication facility. Lithographic

patterning of a film typically includes some or all of the following operations, each operation enabled with a number of possible tools: (1) application of photoresist on a workpiece, i.e., substrate, using a spin-on or spray-on tool; (2) curing of photoresist using a hot plate or furnace or UV curing tool; (3) exposing the photoresist to visible or UV or x-ray light with a tool such as a wafer stepper; (4) developing the resist so as to selectively remove resist and thereby pattern it using a tool such as a wet bench; (5) transferring the resist pattern into an underlying film or workpiece by using a dry or plasma-assisted etching tool; and (6) removing the resist using a tool such as an RF or microwave plasma resist stripper.

CONCLUSION

10 [0141] Although the foregoing embodiments have been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. It should be noted that there are many alternative ways of implementing the processes, systems, and apparatus of the present embodiments. Accordingly, the present embodiments are to be considered as illustrative and not
15 restrictive, and the embodiments are not to be limited to the details given herein.

CLAIMS

What is claimed is:

1. A method comprising:

providing a substrate in a processing station comprising a substrate support and a
5 showerhead, the substrate comprising a gap to be filled; and

depositing silicon-containing film in the gap by a plasma-enhanced atomic layer
deposition (PEALD) process comprising multiple cycles of operations (a)-(d):
 - (a) a dose operation comprising flowing a silicon-containing precursor into the
processing station via the showerhead to allow the silicon-containing
10 precursor to adsorb onto the substrate;
 - (b) after (a), flowing a purge gas into the processing station;
 - (c) after (b), exposing the substrate to plasma species to react with the adsorbed
silicon-containing precursor; and
 - (d) after (c), flowing a purge gas into the processing station,
15 wherein the silicon-containing precursor continues to flow into the processing
station during at least (b).
2. The method of claim 1, wherein the silicon-containing precursor continues to flow into
the processing station during at least part of (c).
3. The method of claim 1, wherein the silicon-containing precursor continues to flow into
20 the processing station during (c) and at least part of (d).
4. The method of claim 1, wherein after (a), the silicon-containing precursor flow continues
into flow into the processing station at a decreasing flow rate.
5. The method of claim 1, wherein (a) comprises flowing an inert gas and a vaporized
silicon-containing precursor from a silicon-containing precursor source fluidically
25 connected to a gas delivery line via an outlet valve, the gas delivery line fluidically
connected to the showerhead, and at the end of (a), closing the outlet valve.
6. The method of claim 5, wherein silicon-containing precursor in the gas delivery line

continues to flow into the processing station after the outlet valve is closed.

7. The method of claim 1, further comprising diverting silicon-containing precursor from the processing station during one or more of (c) and (d).
8. The method of claim 1, wherein the plasma in (c) is a dual frequency RF plasma generated using high frequency (HF) and low frequency (LF) RF power.
9. The method of claim 8, further comprising increasing an inert gas flow into the processing station during (c).
10. The method of claim 8, wherein the HF power is at least 4 kW and the LF power is between 500 W and 5 kW.
11. The method of claim 8, further comprising sputtering and re-depositing silicon-containing film in the gap during deposition of the silicon-containing film in the gap.
12. The method of claim 1, wherein the plasma species are generated from oxygen (O₂).
13. The method of claim 1, wherein the plasma species are generated from nitrous oxide (N₂O).
14. The method of claim 1, wherein the plasma species are generated from nitrogen (N₂).
15. The method of claim 1, wherein (b) is between 50–500 milliseconds in duration.
16. The method of claim 1, wherein the gap to be filled is a gap between memory stacks of a 3D NAND structure.
17. The method of claim 1, wherein the gap has aspect ratio of at least 20:1.
18. The method of claim 1, further comprising exposing the deposited film to an inhibition plasma before at least one of the multiple cycles.
19. A method comprising:

providing a substrate having a structure including a gap to be filled;

depositing a silicon-containing protective film selectively at an upper portion of the structure such that it extends only partially into the gap by a plasma-enhanced atomic layer deposition (PEALD) process comprising:

- 5 (a) a dose operation comprising flowing a silicon-containing precursor into the processing station via the showerhead to allow the silicon-containing precursor to adsorb onto the substrate;
- (b) after (a), flowing a purge gas into the processing station;
- 10 (c) after (b), exposing the substrate to plasma species to react with the adsorbed silicon-containing precursor, wherein the plasma in (c) is a dual frequency RF plasma generated using high frequency (HF) and low frequency (LF) RF power; and
- (d) after (c), flowing a purge gas into the processing station.

20. The method of claim 19, further comprising: performing one or more cycles of:

- 15 exposing the substrate including the protective film to an inhibition plasma comprising halogen species to inhibit deposition on a portion of the gap; and
- after exposing the substrate to the inhibition, depositing dielectric material in the gap.

21. The method of claim 19, wherein the silicon-containing precursor continues to flow into the processing station during at least (b).

20 22. The method of claim 20, wherein the protective film is etched during exposure to the inhibition plasma.

23. The method of claim 20, wherein the plasma during (a) is generated from nitrogen trifluoride (NF₃) and the protective liner is a silicon nitride film.

24. The method of claim 1, wherein the protective liner is between 10 and 999 Angstroms thick.

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25. The method of claim 1, wherein depositing a protective liner and the performing one or more cycles are performed in the same chamber.

26. The method of claim 1, wherein the structure is a 3D NAND structure, the gap is formed by two stacks each comprising multiple pairs of an oxide layer and a nitride layer and capped by a polysilicon layer and wherein the protective film protects the polysilicon layer.
- 5 27. A method comprising:
- providing a substrate in a processing station comprising a substrate support and a showerhead;
- depositing a silicon-containing film on the substrate by a plasma-enhanced atomic layer deposition (PEALD) process comprising multiple cycles of operations (a)-(d):
- 10 (e) a dose operation comprising flowing a silicon-containing precursor into the processing station via the showerhead to allow the silicon-containing precursor to adsorb onto the substrate;
- (f) after (b), flowing a purge gas into the processing station;
- (g) after (b), exposing the substrate to plasma species to react with the adsorbed
- 15 silicon-containing precursor; and
- (h) after (c), flowing a purge gas into the processing station, wherein the silicon-containing precursor continues to flow into the processing station during at least (b).
28. The method of claim 27, wherein the silicon-containing film fills a gap on the substrate.
- 20 29. The method of claim 27, wherein the silicon-containing film is non-conformally deposited on a structure having two stacks separated by a gap such that the film is deposited at the top of the stacks extending only partially into gap.
30. The method of claim 27, wherein the plasma in (c) is a dual frequency RF plasma generated using high frequency (HF) and low frequency (LF) RF power.
- 25 31. A method comprising:
- providing a substrate in a processing station comprising a substrate support and a showerhead;

depositing a silicon-containing film on the substrate by a plasma-enhanced atomic layer deposition (PEALD) process comprising multiple cycles of operations (a)-(d):

(e) a dose operation comprising flowing a silicon-containing precursor into the processing station via the showerhead to allow the silicon-containing precursor to adsorb onto the substrate;

(f) after (b), flowing a purge gas into the processing station;

(g) after (b), exposing the substrate to plasma species to react with the adsorbed silicon-containing precursor; and

(h) after (c), flowing a purge gas into the processing station,

wherein the plasma in (c) is a dual frequency RF plasma generated using high frequency (HF) and low frequency (LF) RF power

32. The method of claim 31, wherein the silicon-containing film fills a gap on the substrate.

33. The method of claim 31, wherein the silicon-containing film is non-conformally deposited on a structure having two stacks separated by a gap such that the film is deposited at the top of the stacks extending only partially into gap.

34. A method comprising:

providing a substrate in a processing station;

depositing a silicon oxynitride (SiON) film on the substrate by:

(f) stabilizing process conditions in the processing station for silicon oxide deposition;

(g) performing x plasma-enhanced atomic layer deposition (PEALD) cycles using an oxygen-based plasma, where x is an integer greater than zero;

(h) stabilizing process conditions in the processing station for silicon nitride deposition;

(i) performing y plasma-enhanced atomic layer deposition (PEALD) cycles using a nitrogen-based plasma, where y is an integer greater than zero; and

(j) repeating (a)-(d) one or more times.

35. The method of claim 34, wherein $x + y$ is no more than 20.

36. The method of claim 34, wherein $x + y$ is no more than 15.

37. The method of claim 34, wherein $x + y$ is no more than 15.

5 38. The method of claim 34, wherein the oxygen-based plasma of each cycle of (b) has a first duration and the nitrogen-based plasma of each cycle of (d) has a second duration wherein the second duration is at least twice as long as the first duration.

39. The method of claim 34, wherein the SiON film is conformally deposited on a patterned layer.

10 40. A method comprising:

providing a substrate in a processing station comprising a substrate support and a showerhead, the substrate comprising a gap to be filled; and

depositing silicon-containing film in the gap by a plasma-enhanced atomic layer deposition (PEALD) process comprising multiple cycles of operations (a)-(d):

15 (a) a dose operation comprising flowing a silicon-containing precursor into the processing station via the showerhead to allow the silicon-containing precursor to adsorb onto the substrate;

(b) after (a), flowing a purge gas into the processing station;

20 (c) after (b), exposing the substrate to plasma species generated from a reactant gas to react with the adsorbed silicon-containing precursor; and

(d) after (c), flowing a purge gas into the processing station, wherein the reactant gas and/or the plasma species continue to flow into the processing station during at least (a).

25 41. A method comprising:

providing a substrate in a processing station comprising a substrate support and a

showerhead, the substrate comprising a gap to be filled; and

depositing silicon-containing film in the gap by a plasma-enhanced atomic layer deposition (PEALD) process comprising multiple cycles of operations (a)-(d):

- 5 (a) a dose operation comprising flowing a silicon-containing precursor into the processing station via the showerhead to allow the silicon-containing precursor to adsorb onto the substrate;
- (b) after (a), flowing a purge gas into the processing station;
- (c) after (b), exposing the substrate to plasma species generated from a reactant gas to react with the adsorbed silicon-containing precursor; and
- 10 (d) after (c), flowing a purge gas into the processing station, wherein the silicon-containing precursor continues to flow into the processing station during at least (b) and/or wherein the reactant gas and/or the plasma species continue to flow into the processing station during at least (a),
- 15 wherein a closed void is formed in the gap.

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