

PATENT SPECIFICATION

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DRAWINGS ATTACHED

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(54) ELECTRICAL CIRCUITS EMPLOYING TRANSISTORS

(71) We, RCA CORPORATION, formerly known as Radio Corporation of America, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electrical circuits and, more particularly, to an integrated circuit including a common emitter transistor amplifier connected in circuit with a common collector transistor amplifier and interconnected with a voltage divider network in a degenerative feedback loop such that the common emitter stage additionally provides a stabilized direct current (d—c) voltage reference for the common collector stage. Depending upon the manner of its connection to surrounding and cooperating electrical circuitry, the integrated arrangement can perform many different functions. Some of these, to be described below, are: as a source of regulated operating potential; as a translating stage for referencing an output signal to a direct voltage different from that to which the corresponding input signal is referenced; and as an amplifier stage in which the signal gain and d—c output voltage can be individually controlled.

As used herein, the term "integrated circuit" refers to a unitary or monolithic semiconductor device or chip which is the equivalent of a network of interconnected active and passive circuit elements.

The terms "resistors", "capacitors", "transistors", "rectifiers", etc. as used herein are intended to apply to the equivalent device as incorporated in or on an integrated circuit device, unless otherwise indicated. The manner of implementing these components on such a device is known in the art.

In the accompanying drawings:

FIGURE 1 is a schematic circuit diagram

of a source of regulated operating potential incorporating the principles of the invention;

FIGURE 2 is a schematic circuit diagram embodying the present invention of a translating stage for referencing an output signal to a direct voltage different from that to which the corresponding input signal is referenced;

FIGURE 3 is a schematic circuit diagram of an amplifier stage in which the signal gain and direct current output voltage can be individually controlled, and which is constructed in accordance with the principles of the invention; and

FIGURE 4 is a schematic circuit diagram of a modification of the operating potential source of FIGURE 1.

Referring now to the drawings, wherein like reference characters are used to designate like elements throughout the several figures, and particularly to FIGURE 1, the regulated operating supply there shown includes a pair of transistors 12 and 14. One transistor 12 is arranged in a common emitter type configuration, with its collector electrode connected to an energizing potential terminal 16 through a resistor 18 and with its emitter electrode connected to a reference terminal 20, which is shown at ground potential.

The other transistor 14 is arranged in a common collector type configuration, with its collector electrode connected to the energizing potential terminal 16 and with its emitter electrode connected to the reference terminal 20 through a pair of serially coupled resistors 22 and 24. The emitter electrode of transistor 14 is connected to a first output terminal 26 while the junction between the resistors 22 and 24 is connected to the base electrode of transistor 12 by a conductor 27.

The collector electrode of transistor 12 is additionally connected to the base electrode of transistor 14 by a conductor 29 and to a second output terminal 28. Appropriate load circuits 30 and 32 are connected respectively between the first and second output terminals

26 and 28 and reference terminal 20. Potential terminal 16 and reference terminal 20 are adapted to be connected to a source of proper polarity (not shown).

- 5 In the operation of the regulated supply of Figure 1, i.e., with a proper polarity potential source connected between the terminals 16 and 20, a point of equilibrium is reached at which one V_{be} voltage drops are developed across the base-emitter junctions of each of the transistors 12 and 14. V_{be} is defined as the voltage drop developed across the base-emitter junction of a transistor. The series combination of the base-emitter junction of transistor 14 and the resistor 22, however, is connected in parallel with the collector-base junction of transistor 12 by conductors 27 and 29. The quiescent voltage developed between the collector and emitter electrodes of transistor 12, therefore, equals the sum of the V_{be} voltage drops of transistors 12 and 14 and the voltage drop across resistor 22.

- 25 With the emitter electrode of transistor 12 grounded via terminal 20, a potential equal to the V_{be} voltage drop of transistor 12 is developed at the common junction of resistors 2 and 24 relative to the ground terminal 20, while a potential equal to that V_{be} voltage plus the voltage drop across the resistor 22 is developed at output terminal 26 relative to ground. With a resistance value for resistor 24 which is small relative to the input impedance of the transistor 12, it can be seen from the drawing that this latter voltage drop substantially equals NV_{be} , where N represents the resistance ratio between resistors 22 and 24, with the resistance value of the resistor 22 being in the numerator and that of the resistor 24 being in the denominator. The potential developed at the output terminal 26 with respect to ground thus is seen to be $(N+1)V_{be}$. Where transistors 12 and 14 are each composed of the same semiconductor material, such as in a monolithic silicon integrated structure, the potential developed at the output terminal 28 would be $(N+2)V_{be}$ relative to the terminal 20. With the illustrative values shown in the drawing, $3V_{be}$ and $4V_{be}$ voltages will be developed at the output terminals 26 and 28, respectively. If the terminal 20 were not grounded but were at some level of direct voltage instead, then these output potentials would each be increased by that amount.

- 55 The regulated supply of FIGURE 1, is a stabilized circuit in that the degenerative feedback loop bounded by the collector-base junction of transistor 12, the lead 29, the base-emitter junction of transistor 14, the resistor 22, and the lead 2, balances out any voltage variations in the supply due to changes in the operating potential applied between terminals 16 and 20.

- 65 A second feature of the supply of FIGURE

1 is that no capacitors are employed. This makes the features of the illustrated circuit particularly useful for integrated circuits since the problems that would be created by incorporating capacitors in integrated circuit design are eliminated.

A third feature of this supply is that low values of resistance (of the order of 5,000 ohms or less) can be used for resistors 18, 22 and 24 and, therefore, only a small amount of space on the integrated chip is required.

A fourth feature of the supply is that the circuit presents low output impedances at the terminals 26 and 28, in order of 100 ohms and less. A fifth feature is that the output potentials developed are referenced against ground and are thus substantially free of any random variations produced at the potential terminal 16 by common impedance coupling to that terminal from the various other circuits on the integrated chip.

Enhanced freedom from oscillation can be had in the circuit of FIGURE 1, if desired, by a number of methods. In one, a resistor can be substituted for the direct connection 27 to form a dominant time constant with the Miller capacitance of the transistor 12. In another method, one or more forward biased and/or avalanche diodes can be connected in series with the load resistor 18, to reduce the trans-conductance (g_m) of the transistor 12 and, consequently, the gain around the feedback loop. A circuit arrangement using a zener diode 70 to effect this reduction in g_m and increase in d-c stability is shown in FIGURE 4.

The direct current re-referencing stage shown in FIGURE 2 is of the same general form as the regulated supply of FIGURE 1. The re-referencing stage differs, however, in that the junction of the resistors 22 and 24 is connected to the base electrode of the transistor 12 by means of a serially coupled resistor 40 instead of the lead 27 of FIGURE 1. The stage also differs in that the end of resistor 18 remote from the transistor 12 is connected to the emitter electrode of a third transistor 42 rather than to the potential terminal 16.

The collector electrode of the transistor 42 is instead connected to the terminal 16 and its base electrode is connected to a source of input signals, represented in the drawing by the terminal 44.

The direct current re-referencing stage further differs from the arrangement of FIGURE 1 by including a bypass capacitor 46 in the feedback loop, for example, to couple the base electrode of transistor 12 to ground. In an integrated version of the circuit shown in FIGURE 2, it will be understood that, depending upon the available area on the chip, the capacitor 46 may be connected as an external component. In such case, the capacitor 46 would be connected

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to the circuit on the chip through a terminal 48, in the manner shown in FIGURE 2.

In the operation of the stage, input signals which are referenced to a first d-c voltage level are supplied via terminal 44 to the base electrode of the transistor 42. These signals may be referenced, for example, to a fraction of the operating potential applied to the terminal 16, and are subsequently translated by the base-emitter junction of the transistor 42 and the resistor 18 to the base electrode of the transistor 14.

The d-c component of the signals developed at the output emitter electrode of the transistor 14 would normally be at a voltage level one V_{be} volts below that existing at its input base electrode, but because of the negative feedback action provided by the loop bounded by the lead 29, the collector-base junction of transistor 12, the base-emitter junction of the transistor 14, and the resistors 22 and 40, that level is constrained to one which is substantially equal to $(N+1)V_{be}$, N and V_{be} being set forth above. Any tendency for the input d-c level to vary (due to a variation in the value of the operating potential supply, for example) is offset, furthermore, by the feedback within the loop so that the output d-c component becomes stabilized against such changes.

The alternating current (a-c) component of the signals developed at the emitter electrode of the transistor 14, on the other hand, is bypassed to ground by the capacitor 46 and, therefore, is not degenerated by the feedback loop. That component thus produces an output signal by emitter follower action at the terminal 26. The resulting re-referencing of the d-c component of the input signal in this manner, without substantially affecting the a-c component, is particularly desirable where terminal 26 is connected to additionally bias a succeeding stage designed to operate with multiple V_{be} bias voltages instead of with the input fractional operating potential voltage.

It will be noted that as a result of the above described action, the direct current voltage at the emitter electrode of the transistor 14 will be independent of variations in the potential applied to terminal 16. That is, being dependent primarily on V_{be} voltage drops, this voltage varies not as a function of operating potential, but as a function of temperature. This, however, may not be a problem in integrated circuit design but an advantage, for example, in those cases where the direct current voltage sets the base-emitter bias for a succeeding transistor amplifier stage connected to the terminal 26. In such cases, the variations in the d-c voltage is in a direction to offset similar variations with temperature in the base-to-emitter voltage drop of the following transistor

and helps to maintain more constant current flow therein.

It will also be noted that the inclusion of the resistors and transistors in a direct current re-referencing stage such as shown in FIGURE 2 is oftentimes justified in integrated circuit design, even if only to save one of the two terminals which would be used in employing a more conventional coupling capacitor for re-referencing purposes, in those instances where the number of available terminals on the chip are severely limited. (It will be understood in this regard that the ground terminal 20 is required in any case and is not counted toward the number of terminals used in the re-referencing scheme.)

It will be appreciated, however, that with present integrated circuit fabrication techniques, the amount of space required on the monolithic chip to include these added components is acceptably small. As with the arrangement of FIGURE 1, a direct connection can be used to couple to the base electrode of the transistor 12 in FIGURE 2 instead of the resistor 40, without impairing the operation of the re-referencing stage.

The amplifier stage shown in FIGURE 3 is substantially identical in construction to the regulated operating supply of FIGURE 1 and, as in that supply, choice of the resistance ratio between the resistors 22 and 24 primarily determines the direct voltage output level to which, in this case, the amplified signals will be referenced. The amplifier, in addition to the components recited with respect to FIGURE 1, includes a source of a-c input signals 50, which is coupled to the base electrode of the transistor 12 by means of a capacitor 52.

It will be understood that in an integrated circuit version of the amplifier of FIGURE 3, both the source 50 and the capacitor 52 will be external to the monolithic chip, but will be connected to the remainder of the amplifier circuitry thereon via a terminal 54. The source 50 and the capacitor 52 are selected to exhibit an impedance at the input signal frequency which is considerably smaller than the resistance value of the parallel combination of the resistors 22 and 24.

With such an arrangement, choice of the resistance values for the resistors 22 and 24, once again determines the d-c output voltage established at the output terminal 26. More particularly, by virtue of the degenerative action within the feedback loop between the collector and base electrode of the transistor 12, the d-c voltage is established at terminal 26 at the afore-defined $(N+1)V_{be}$ level. The feedback loop is effectively bypassed for a-c signals, however, in that substantially all of the a-c signal voltage is dropped across the resistor 22. This follows since the impedance of the resistor 22 is many times greater than the effective imped-

ance apparent at the base electrode of the common emitter transistor 12.

The signal gain provided by the amplifier stage is thus set by the product of the transconductance, or g_m , of the transistor 12 and the value of its load resistor 18, which, as can be seen, is independent of the d-c output voltage established by selection of the resistors 22 and 24. With the values shown in the drawing, a voltage gain of approximately 150 times is provided, and the signals developed at the output terminal 26 are each referenced to a $6V_{be}$ volts level. Alternatively, the amplified signals can be taken from the output terminal 28, where they are referenced to a $7V_{be}$ level. It will be apparent that, in such a case, the added $1V_{be}$ volts of reference follows from the V_{be} drop (typically 0.7 volts) across the base-emitter junction of the transistor 14.

As was previously mentioned, these amplified signals can be coupled to an input terminal of a differential amplifier type utilization circuit (not shown), for example, which also is referenced to a corresponding $6V_{be}$ or $7V_{be}$ level, as the case may be. With a one volt or so input signal, such a circuit can then be used to provide limiting, if desired.

As is clear from the above, the circuit arrangements incorporating the principles of the present invention are particularly attractive for integrated circuit design. The operation of each, for example, depends on the ratio of the pair of impedance elements which, in an integrated circuit structure, is relatively stable, although the absolute values of the impedances may vary because of the manufacturing process tolerances. In the regulated potential supply environment, the fact that the V_{be} voltages provided may vary somewhat with temperature does not prove undesirable where the supply is used to bias amplifier stages employing integrated circuit transistors whose base-to-emitter voltage drops vary with temperature in the same manner and direction.

In the direct voltage re-referencing situation, where the bypass capacitor would normally be connected external to the integrated chip, it will be appreciated that one less terminal will be used to connect to that capacitor than would usually be the case where conventional capacitive coupling is used between stages to perform the re-referencing function, a point of major importance where the number of available terminals on the chip are limited. In the amplifier arrangement, furthermore, both the signal gain provided and the quiescent direct voltage output level can be independently set so as to permit optimum performance of any subsequently connected amplifier circuitry, or the like. With respect to these features, it will be understood that capacitors, in integrated

circuit design, occupy considerable area on the monolithic device, even for a relatively small amount of capacitance.

WHAT WE CLAIM IS:—

1. An electrical circuit in which a first transistor connected in common emitter configuration is connected in cascade with a second transistor connected in common collector configuration with an output terminal d-c connected to the base or emitter of the second transistor, the base of the second transistor being d-c coupled to the collector of the first transistor, and the emitter of the second transistor being d-c coupled to the base and emitter of the first transistor over a voltage divider network coupling the two transistors in a degenerative feedback loop such that the d-c voltage component of a signal at said output terminal is substantially determined by the V_{be} (base-emitter) voltage in the first transistor (or in both transistors as the case may be) substantially unaffected by variation of voltage supply to the circuit.

2. An electrical circuit according to Claim 1 wherein the emitter of the first transistor is directly (non-degeneratively) coupled to a reference potential point and said voltage divider network is connected between said reference point and the emitter of the second transistor, with an intermediate point of the network d-c coupled to the base of the first transistor.

3. An electrical circuit comprising a first transistor connected in common emitter configuration, a second transistor connected in common collector configuration, d-c coupling between the collector of the first transistor and the base of the second transistor, an output terminal connected to the emitter or base of the second transistor, a d-c voltage divider comprising first and second resistive elements connected in series in that order from the emitter of the second transistor to the emitter of the first transistor, this latter emitter being non-degeneratively coupled for d-c to a reference potential point, and a degenerative d-c feedback coupling to the base of the first transistor from the junction of said resistive elements, the resistance of the first element being greater by a factor N than that of the second element and the latter having a relatively low resistance compared with the base input resistance of the first transistor, whereby the quiescent voltage drop across the first resistive element will in operation approximate to N times the voltage drop across the second resistive element with the latter voltage drop determined by the V_{be} (base-emitter) voltage in the first transistor.

4. An electrical circuit as claimed in Claim 1 characterized in that said transistors together with resistive elements and inter-

ance apparent at the base electrode of the common emitter transistor 12.

The signal gain provided by the amplifier stage is thus set by the product of the transconductance, or g_m , of the transistor 12 and the value of its load resistor 18, which, as can be seen, is independent of the d—c output voltage established by selection of the resistors 22 and 24. With the values shown in the drawing, a voltage gain of approximately 150 times is provided, and the signals developed at the output terminal 26 are each referenced to a $6V_{be}$ volts level. Alternatively, the amplified signals can be taken from the output terminal 28, where they are referenced to a $7V_{be}$ level. It will be apparent that, in such a case, the added $1V_{be}$ volts of reference follows from the V_{be} drop (typically 0.7 volts) across the base-emitter junction of the transistor 14.

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As is clear from the above, the circuit arrangements incorporating the principles of the present invention are particularly attractive for integrated circuit design. The operation of each, for example, depends on the ratio of the pair of impedance elements which, in an integrated circuit structure, is relatively stable, although the absolute values of the impedances may vary because of the manufacturing process tolerances. In the regulated potential supply environment, the fact that the V_{be} voltages provided may vary somewhat with temperature does not prove undesirable where the supply is used to bias amplifier stages employing integrated circuit transistors whose base-to-emitter voltage drops vary with temperature in the same manner and direction.

In the direct voltage re-referencing situation, where the bypass capacitor would normally be connected external to the integrated chip, it will be appreciated that one less terminal will be used to connect to that capacitor than would usually be the case where conventional capacitive coupling is used between stages to perform the re-referencing function, a point of major importance where the number of available terminals on the chip are limited. In the amplifier arrangement, furthermore, both the signal gain provided and the quiescent direct voltage output level can be independently set so as to permit optimum performance of any subsequently connected amplifier circuitry, or the like. With respect to these features, it will be understood that capacitors, in integrated

circuit design, occupy considerable area on the monolithic device, even for a relatively small amount of capacitance.

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2. An electrical circuit according to Claim 1 wherein the emitter of the first transistor is directly (non-degeneratively) coupled to a reference potential point and said voltage divider network is connected between said reference point and the emitter of the second transistor, with an intermediate point of the network d—c coupled to the base of the first transistor.

3. An electrical circuit comprising a first transistor connected in common emitter configuration, a second transistor connected in common collector configuration, d—c coupling between the collector of the first transistor and the base of the second transistor, an output terminal connected to the emitter or base of the second transistor, a d—c voltage divider comprising first and second resistive elements connected in series in that order from the emitter of the second transistor to the emitter of the first transistor, this latter emitter being non-degeneratively coupled for d—c to a reference potential point, and a degenerative d—c feedback coupling to the base of the first transistor from the junction of said resistive elements, the resistance of the first element being greater by a factor N than that of the second element and the latter having a relatively low resistance compared with the base input resistance of the first transistor, whereby the quiescent voltage drop across the first resistive element will in operation approximate to N times the voltage drop across the second resistive element with the latter voltage drop determined by the V_{be} (base-emitter) voltage in the first transistor.

4. An electrical circuit as claimed in Claim 1 characterized in that said transistors together with resistive elements and inter-



13 (15)

connections constituting said cascaded common emitter and common base configurations are disposed in a single integrated circuit.

5 4 wherein said integrated circuit also includes further circuitry coupled to said output terminal to receive direct current voltage biasing therefrom.

10 6. An electrical circuit as claimed in any preceding Claim wherein the collector of said first transistor is coupled through a (further) resistive element to a connection point for a source of energizing potential, the collector of said second transistor being
15 directly connected to said connection point.

20 7. An electrical circuit as described in Claim 6 having coupled between said (further) resistive element and said connection point a low impedance source of input signal, and having a capacitor decoupling terminal connected to the base of said first transistor.

8. An electrical circuit as claimed in Claim

6 having an input terminal connected to the base of said first transistor (12) for receiving an input signal thereto through a capacitive element. 25

9. An electrical circuit substantially as hereinbefore described with reference to Figure 1 of the accompanying drawings.

10. An electrical circuit substantially as
30 hereinbefore described with reference to Figure 2 of the accompanying drawing.

11. An electrical circuit substantially as
35 hereinbefore described with reference to Figure 3 of the accompanying drawing.

12. An electrical circuit substantially as hereinbefore described with reference to Figure 4 of the accompanying drawing.

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