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INTEGRATED HIGH-PERFORMANCE DECOUPLING CAPACITOR

FIELD OF THE INVENTION

This invention relates generally to semiconductor integrated circuits decoupling capacitors and more particularly to an integrated circuit formed on the active front major surface of a semiconductor chip and having a decoupling capacitor formed on the inactive back major surface of the chip such that the chip substrate functions as one plate of the decoupling capacitor.

BACKGROUND OF THE INVENTION

As integrated circuits on semiconductor chips become denser, faster and more complex, their electrical performance requirements become higher. Consequently these integrated circuits require greater and more effective capacitive decoupling.

Currently, only two effective ways have been used by or known to the industry, to address this need for larger and more effective capacitive decoupling in integrated circuits.

The first way depends on discrete decoupling capacitors being added onto the package containing the integrated semiconductor chip. Because the decoupling capacitors are far removed from the active circuitry on the chip they provide, at best, only marginal decoupling. Furthermore as the circuits and hence the chips become

larger the decoupling effects of such off chip capacitors become further degraded.

The second way depends on the adequacy of available regions in the circuity itself. However, as the chip circuitry becomes denser, the free area into which such decoupling capacitors can be placed becomes reduced at the same time that the demand for more decoupling capacitance is increasing. Simultaneously the deposited oxide on the active major circuit front major surface or face is becoming thinner while the need to decouple large on-chip voltages or voltage spikes, requiring thicker oxides or larger area or both becomes greater.

Thus just as the size and number of such decoupling capacitors that can be placed in unused areas on the active front major surface of the semiconductor chip becomes fewer and smaller and more ineffective there is an increasing need for more decoupling capacitance.

SUMMARY OF THE INVENTION

The present invention solves this problem and provides the means of applying significant amounts of effective on-chip decoupling capacitance in an integrated circuit, regardless of the density of the formed circuit.

This is achieved by providing a decoupling capacitance that uses the substrate of the chip itself as one of the capacitive plates while the other plate is

comprised of a metallic deposit formed on the back or inactive major surface of the chip and electrically connected to the active circuit on the front or active major surface of the chip.

The present invention thus results in significant and effective decoupling capacitance in close proximity to the active circuit on the chip requiring such decoupling capacitance.

More specifically the present invention achieves this desirable result by providing a metal coated, dielectric layer on the unused backside of the chip that serves as a first plate of the decoupling capacitor and employing the chip substrate as the second plate of the decoupling capacitor.

Very precise decoupling of selected areas in the chip circuit can be achieved by forming a plurality of precisely sized metal deposits on the insulated back surface of the chip and selectively and individually connecting, through appropriate vias, these deposits to the circuits, on the front surface of the chip, needing the precise decoupling capacitance.

Accordingly it is an object of the invention to provide a significant and very effective decoupling capacitor in close proximity to the active circuit on the chip requiring such decoupling capacitance.

These and other objects and features of the present invention will become further apparent from the following

description taken in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional schematic representation of a semiconductor chip having an integrated circuit formed on one face thereof and having a decoupling capacitor, in accordance with the present invention, formed thereon.

Fig. 2 is a cross-sectional schematic representation of a semiconductor chip having an integrated circuit formed on one face thereof and having a plurality of decoupling capacitors, in accordance with the present invention, formed thereon.

Fig. 3 is a graph depicting the range of the formed capacitance of the present invention as a function of the backside insulation thickness and comparing the scope of the present invention to the scope of the prior art decoupling capacitance.

Fig. 4 is a cross-sectional schematic representation of a semiconductor chip similar to that of Fig. 1 but having a different embodiment of the decoupling capacitor formed on the back of the chip.

Fig. 5 is a cross-sectional schematic representation of a semiconductor chip similar to that of Fig. 4 but having still a further and different embodiment of the decoupling capacitor formed on the back of the chip.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 1 is a cross-sectional schematic representation of an semiconductor chip 10 employing the present invention. The semiconductor chip or substrate 10 has a pair of substantially parallel major surfaces 12 and 14. A doped or epitaxial layer or region 16 is created on surface 12 and a plurality of devices 18 are created in the region 16 by, for example, diffusion or ion implantation or any other suitable method known to the semiconductor art. Thus surface 12 is hereby defined as the active surface or face of the chip and surface 14 as the back or inactive surface of the chip.

The devices 18, are used herein to represent both active and inactive circuit elements, e.g. transistors or resistors. To achieve the proper biasing of the devices 18, one or more wiring levels, interposed with insulating or passivating layers, are formed on the surface 17 of the region 16 to interconnect the formed devices 18 into a desired integrated circuit. In present day integrated circuits, the region 16 and the circuit formed of the devices 18 are coupled to a selected voltage source 19, usually positive, and the substrate 10 is connected to ground. This is possible because of the semiconductor junction existing, at surface 12, between the region 16 and the substrate 10. It should be noted that the substrate 10 could be connected to a second

voltage source, such as a negative voltage source, instead of to ground.

More specifically, the desired circuit configuration is created by forming a first insulating layer 20 on the surface 12 and forming interconnection openings 21 therein by etching or the like. A first wiring layer 22 is now formed on the surface of the insulating layer 20 and contacts are made to selected portions of selected ones of the devices 18 through the interconnection openings 21. A second insulating layer of silicon oxide 23 is now formed over the formed wiring layer 22. Following the formation of the insulating layer 23 different interconnection openings 24 are made therein and a second wiring layer 25 is formed on the surface of the insulating layer 23 with the material of the second layer 25 contacting selected portions of the devices 18 as well as selected points on the first wiring layer 22 through the openings 24. A final top passivating layer 26 is disposed over this second wiring level 25. the layers 20,22,23 and 25 together form a wiring net 27.

It should be understood that the above steps of forming the insulating layers, the interconnection openings therein and the wiring levels can be repeated any number of times until the final desired circuit is formed. The formation of such multiple wiring levels is widely practiced in the semiconductor art.

Now, in accordance with the present invention, a

precisely positioned via 30, having an inner diameter of approximately 0.003 inches, is ablated through the substrate 10, the epitaxial layer 16, the insulating layers, 20, 23, and 26 and the wiring levels 22 and 25, by applying a laser beam from an XeCl excimer laser to a selected position on the chip 10.

The laser beam, for accomplishing this task, preferably, has a wavelength of 308 nanometers (nm) with a pulse width (FWHM) of 25 nanoseconds (ns). The laser beam is first passed through a commercially available beam homogenizer to develop a uniform intensity profile and then through suitable 10X reducing optics. Beam fluance of 17 - 30 Joules/cm^2 for 20 - 30 seconds at a pulse rate of approximately 200 pulses per second is particularly suitable for forming the desired via 30.

The laser beam, striking the chip, ablates all the material thereon, as well as the silicon of the chip itself, and forms a precise, cylindrical hole or via 30 therethrough. Using the above described laser the formed via 30 typically has an inner diameter of approximately 0.003 inches and is almost ideally cylindrical in form.

It should be noted that the diameter of the via can be altered by changing the above characteristics of the laser beam as is known to those skilled in the art.

It should also be noted that although only a single laser formed via 30 is shown in Fig. 1 that a plurality of such vias or holes can be formed in the substrate

provided that the vias are separated from the edge or from one another by a distance equal to a least four times the inner diameter of the formed via. Other than these constraints there are no inherent limitations on where these vias can be formed in the chip substrate. However it should be clearly understood that the design of the integrated circuit formed on the active surface 12 can further constrain the location of these vias.

That is, the formed via must be positioned with consideration as to the location of the devices 18, the wiring levels produced on the active face of the chip and any interconnections therebetween.

Once the via 30 is formed through the entire body 10, the backside surface 14 is provided with a dielectric coating or layer 32 which extends down the entire length of the via 30 as layer 32a and wraps around the bottom of the via 30, as layer 32b to overlie a small portion of the passivation layer 26 and the wiring net 27. Preferably these dielectric layers 32, 32a and 32b are formed of Silicon Dioxide (SiO_2) ranging between 50 and 5000 Ångstoms in thickness. Other suitable dielectrics are Polyamide and Silicon Nitride.

These dielectric layers 32, 32a and 32b can be formed using either of the below described low temperature Silicon Dioxide growth techniques.

The first technique consists of the following procedure.

The wafer to be treated is immersed into an aqueous solution of 3650 ml ethanolamine, 1660 ml deionized water, 1150 grams of gallic acid, 0.3 ml of a 10% surfactant solution comprised of potassium fluorinated alkyl carboxalates and sold under the trade name FC-129 by the 3M Corp. and from 0.006 to 0.5 M of quinoxaline which produces at higher catalyst concentration a suitable dielectric coating, such as silicon dioxide (SiO_2), both on the surface 14 of the wafer as well as on the wall of the laser created via 30. By controlling the thickness of the oxide, forming layers 32, 32a and 32b, the core of the via 30 is left open so that a conductive material 34a can be coated onto dielectric layer 32a coating the wall of the via 30 as will be later described.

The second technique is a low temperature deposition of silicon dioxide by a plasma enhanced chemical vapor deposition process. This process uses any commercially available apparatus having a 13.56 MHz RF power source, an electrode spacing of 3.2 cm. and a top electrode maintained at 80° C. This apparatus is capable of depositing SiO_2 on a substrate at a rate of approximately 60 Å per minute when the substrate is held temperature of 350° C, the reactive gases, N_2O and SiH_2, introduced into the chamber containing the substrate, have a ratio greater than 100, preferably a ratio of approximately 125, with the chamber pressure at 1 Torr and the power

level at 25 watts.

Following the formation of the dielectric layers 32, 32a and 32b an interconnection opening 33 is made through the dielectric 32b, and the passivation layer 26 to contact to one of the wiring levels 22 or 25, forming the wiring net 27, and a conductive layer 34, formed of any suitable conductive material, for example, of a metal, such as aluminum, copper, tungsten, gold, lead, tin, silicon, titanium, chrome or combinations thereof, is deposited over the dielectric layer 32, as layer 34, down the length of the via 30 as layer 34a and wrapped around the end of the via 30 as layer 34b to pass through the interconnection opening 33 and connect to the wiring net 27. The formation of these metal layers can be made in any number of ways well known to the semiconductor art among which are plating, evaporation or sputtering techniques.

In this way the metallic layer 34 is connected to a respective voltage in the wiring net 27.

By connecting the layer 34 to the circuit such that the layer 34 is biased positive with respect to the grounded substrate 10, the layer 34 will serve as one plate of the decoupling capacitor and the substrate 10 serves as the other plate of the capacitor.

The layer 34 may be insulatively coated with a suitable dielectric 36 and the circuit completed by forming input/output pads (not shown) connected to the

wiring net and then appropriately securing the finished unit to a suitable semiconductor package.

Turning now to Fig. 2 a different embodiment of the invention will be discussed. Shown in this figure 2, the layer 34 is divided into a multiplicity of individual plates 40, 41, 42, 43 and 44, each of which is separately coupled to respective points in the wiring network 27 requiring an individual decoupling capacitor. Plates 43 and 44 are shown as being identical in size. Plates 40 and 41 are schematically shown connected to wiring network 27 through respective vias 45 and 46 by respective connectors 47 and 48.

Very precise decoupling of selected areas in the chip circuit can be achieved by forming such a plurality of precisely sized metal deposits on the insulated back surface of the chip and selectively and individually connecting, through appropriate vias, these deposits to the circuits, on the front surface of the chip, needing the precise decoupling capacitance.

Although only two of the capacitors, 43 and 44, are shown as identical in size, it should be understood that all the plates 40, 41, 42, 43 and 44 can be identical in size and capacitive value or all may be different in size and capacitive value.

In this way, the invention provides larger, more precisely designed and very effective decoupling capacitors to specified portions of the circuit.

Turning now to Fig. 3 there is shown a graph depicting the range of the formed capacitance of the present invention as a function of the backside insulation thickness and comparing the capacitor formed in accordance with the present invention to the typical prior art decoupling capacitors.

The graph of Fig. 3 is representative of the capacitance available on a particular sized integrated circuit chip and illustrates the variation in capacitance for that chip versus the available insulator thicknesses.

In the graph of Fig. 3 the parallelogram 50 sets forth a typical design range of decoupling capacitors formed, in accordance with the present invention, on the back side of the integrated circuit described below. The smaller window 51 depicts the typical design range of decoupling capacitors formed, in accordance with the prior art, on the active face of the same integrated circuit.

As is well known the desired capacitor size is established by the well known capacitor equation

$$C = \epsilon A/s$$

where ϵ is the permittivity of the chosen dielectric; A is the area of the electrodes and s the thickness of the formed dielectric layers 32, 32a and 32b.

The decoupling capacitance for a typical prior art chip which depends on available space on the active face

of the integrated circuit can be determined as follows. If we assume that a typical chip is 0.8 cm long and has a width of 1.75 cm then one face thereof has an area A of 1.4 cm^2. and if we further assume the dielectric is silicon dioxide having a thickness s of 100 x 10^{-8} cm and a permitivity ϵ of 34.5 X 10^{-14} Fd/cm and the typical pad size, used on the active face of present day integrated circuits, is 1 X 10^{-4} Cm^2 then, for a chip having 100 pads, the area available for the formation of the decoupling capacitors on the surface of the active surface of the device is accordingly reduced. The total capacitance of the decoupling capacitors that can be provided on the active face of the device when using all the area available, i.e., the space on the active face not required for the chip pads etc. on the typical, above described chip, can readily be calculated to range between 5 X 10^{-7} and 3.5 X 10^{-11} Farads.

The present invention relies on using the entire back surface of the integrated circuit chip on which to form the decoupling capacitor and its total capacitance is determined as follows. Again if we assume that the typical chip is 0.8 cm long and has a width of 1.75 cm then the major surfaces thereof each has an area A of 1.4 cm^2. We will further assume the dielectric provided on the back major surface of the chip, is, as above discussed, silicon dioxide having a thickness s of 100 x 10^{-8} cm^2 and a permitivity ϵ. Now, however,

because the present invention does not rely on having the capacitors on the active major surface of the circuit the number of pads and their sizes can be disregarded. Accordingly, because the entire back surface of the chip is available, the capacitor formed, using the entire back surface of the device as taught by the present invention, on the above described chip using the described dielectric materials can now be readily be calculated to range between 1 X 10^{-6} and 1 X 10^{-12} Farads. It should be understood that the capacitor or capacitors actually formed in the above example will depend on the selected plate area and that this can be less than the total area of the back side of the chip.

It should be further clearly understood that the range given in the above example was for a particularly sized chip and the graph shown will vary with chip size. Furthermore the graph can readily be altered by changing one or more elements in the above capacitor equation. That is, the capacitance can altered by selecting a different dielectric material, hence changing the permittivity, or by using a different size chip, or otherwise changing the area of the capacitor electrodes, or by changing the thickness of the formed dielectric layer or by altering any combination these elements. Thus, for example, the chip illustrated in Fig. 2 would provide four different capacitive values.

Fig. 4 is a cross-sectional schematic representation

of a semiconductor chip similar to that of Fig. 1 but having a different embodiment of the decoupling capacitor formed on the back of the chip.

Fig. 4 shows a cross-sectional schematic representation of an semiconductor chip 10 showing a different embodiment of the present invention. The semiconductor chip or substrate 10 has a pair of substantially parallel major surfaces 12 and 14 with a doped or epitaxial layer or region 16 on surface 12 and a plurality of active and inactive devices 18 in the region 16. Again surface 12 is defined as the active face of the chip and surface 14 as the back of the chip and one or more wiring levels, interposed with insulating or passivating layers, are formed on the surface 17 of the region 16 to interconnect the formed devices 18 into a desired integrated circuit. Again the region 16 and the circuit formed of the devices 18 are coupled to a selected voltage source 19.

Again the via 30 passes through the substrate 10, the epitaxial layer 16, the insulating layers, 20, 23, and 26 and the wiring levels 22 and 25 to a selected position on the chip 10 and the backside surface 14 provided with a dielectric 32 overcoated with a conductive layer 34 both of which extend down the via 30 and as layers 32a and 34a and as layers 32b and 34b, wrap around over the wiring net 27 with layer 34b contacting the wiring net 27.

Now a new or additional via 39 is ablated, using the above described laser method, through the conductive layer 34, the dielectric layer 32 and through the substrate 10 the epitaxial layer 16, the insulating layers, 20, 23, and 26 and the wiring levels 22 and 25 to a different selected position on the chip 10. Once the new via 39 has been created, the layer 34 is insulatively coated with a suitable dielectric 36 and a second conductive layer 37 is formed over the layer 36 as described above. Again these added layers extend through the via 30 as layers 36a and 37a, and as layers 36b and 37b wrap around atop the wiring net 27. Again the layer 37a can be made to contact any suitable voltage or even ground in the wiring net 27.

Again the upper plate 37 may be coated with a suitable insulator 38 and the circuit completed by forming input/output pads (not shown) connected to the wiring net and then appropriately securing the finished unit to a suitable semiconductor package (not shown).

Fig. 5 is a cross-sectional schematic representation of a semiconductor chip similar to that of Fig. 4 but having still a further and different embodiment of the decoupling capacitor formed on the back of the chip.

Fig. 5 shows a cross-sectional schematic representation of an semiconductor chip 10 and shows still a different embodiment of the present invention. The semiconductor chip or substrate 10 has a pair of

substantially parallel major surfaces 12 and 14 with a doped or epitaxial layer or region 16 on surface 12 and a plurality of active and inactive devices 18 in the region 16. Again surface 12 is defined as the active face of the chip and surface 14 as the back of the chip and one or more wiring levels, interposed with insulating or passivating layers, are formed on the surface 17 of the region 16 to interconnect the formed devices 18 into a desired integrated circuit. Again the region 16 and the circuit formed of the devices 18 are coupled to a selected voltage source 19.

Again the via 30 passes through the substrate 10, the epitaxial layer 16, the insulating layers, 20, 23, and 26 and the wiring levels 22 and 25 to a selected position on the chip 10 and the backside surface 14 provided with a dielectric 32 overcoated with a conductive layer 34 both of which extend down the via 30 and as layers 32a and 34a and as layers 32b and 34b, wrap around over the wiring net 27 with layer 34b contacting the wiring net 27.

The layer 34 is now insulatively coated with a suitable dielectric 36 extended through the via 30, as taught above, as layer 36a to wrap around the layer 34b as layer 36b. A second conductive layer 37 is now formed over the layer 36 to also extend through the via 30 as layer 37a to wrap around atop the wiring net 27 as layer 37b. Again the layer 37a can be made to contact

any suitable voltage or even ground in the wiring net 27.

Again the upper plate 37 may be coated with a suitable insulator 38 and the circuit completed by forming input/output pads (not shown) connected to the wiring net and then appropriately securing the finished unit to a suitable semiconductor package (not shown).

From the above it can be readily seen that the present invention provides significantly greater capacitance that was available to prior art devices which depended on placing the decoupling capacitors on the active surface of the circuit.

It should however be noted that in the present invention the available capacitance can be further extended by also combining the present invention with the prior art. That is, there is no reason as why a device built in accordance with the present invention cannot also incorporate the prior art decoupling capacitors on the face of the chip.

It should be noted that although the preferred embodiment has been described as using silicon substrates and associated materials that any semiconductor material and suitable materials can be substituted therefore as would be well known to those skilled in the semiconductor art.

It should be further noted that although the substrate has been described as being connected to ground that it could also be a connected to second voltage

source such as a negative voltage source.

Thus the invention teaches a significant and very effective decoupling capacitor in close proximity to the active circuit on the chip requiring such decoupling capacitance.

While the invention has been particularly described with respect to a preferred embodiment, it should be understood that one skilled in the art can, from the foregoing, readily make changes in form and detail without departing from the spirit and scope of the invention.

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What is claimed is:

1. A semiconductor integrated circuit comprising:

a semiconductor substrate having first and second major surfaces;

said first one of said major surfaces having an integrated circuit formed thereon;

an opening having extended walls passing between said first and second surfaces;

an insulator disposed on said second major surface and on the walls of said opening;

a metallic deposit formed on said insulator on said major surface and on the insulator on said walls.

2. The circuit of claim 1 wherein said metallic coating is further covered with an insulator.

3. The circuit of claim 1 wherein said metallic layer is electrically connected to said integrated circuit on said first major surface.

4. The circuit of claim 3 wherein said metallic layer is connected to a voltage and forms one plate of a capacitor and said substrate is connected to ground and forms the second plate of said capacitor.

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5. The circuit of claim 1 wherein said substrate is formed of silicon, said insulator is selected from the group consisting of polyamide, silicon nitride, and silicon dioxide.

6. The circuit of claim 1 wherein said insulator is at least 50 x 10^{-8} cm in thickness and said metallic deposit is selected from the group consisting of tungsten, copper, gold, lead, aluminum, tin, copper aluminum, titanium, chrome and alloys thereof.

7. A semiconductor integrated circuit comprising:

a semiconductor substrate having first and second major surfaces;

said first major surface having an integrated circuit with selected contact points formed thereon;

a plurality of openings having extended walls passing between said first and second surfaces;

an insulator disposed on said second major surface and on the walls of said openings;

a plurality of spaced metallic deposits formed on said insulator on said second major surface, each of said deposits extending down through a respective opening and being connected to a respective one of said contact points.

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8. The circuit of claim 7 wherein said substrate is formed of silicon.

9. The circuit of claim 7 wherein said substrate is formed of silicon, said insulator is selected from the group consisting of polyamide, silicon nitride, and silicon dioxide.

10. The circuit of claim 7 wherein said insulator is at least 50 x 10^{-8} cm in thickness and said metallic deposit is selected from the group consisting of tungsten, copper, gold, lead, aluminum, tin, titanium , chrome and alloys thereof.

11. The circuit of claim 7 further wherein the conductive layer on said dielectric layer is further coated with an insulating layer, said substrate is connected to ground and said conductive layer on said dielectric layer is connected to a power source.

12. The process of claim 7 wherein said substrate is connected to ground and said conductive layer on said dielectric layer is connected to a power source.

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13. A process of forming a capacitor on a semiconductor substrate having first and second major surfaces comprising the steps of:

forming an integrated circuit having a wiring level on said first major surface;

forming a hole through said substrate; said hole extending from said second major surface to and exposing a selected region of said wiring level;

forming a dielectric layer on said second major surface of said substrate and a dielectric coating on the wall of said through hole, said dielectric coating in said hole extending to said wiring level;

forming a conductive layer on said dielectric layer on said second major surface of said substrate and on said dielectric on said wall of said hole; said conductive layer coating said dielectric on said wall of said hole, extending though said hole and electrically contacting said selected region of said first surface of said wring level.

14. The process of claim 13 wherein said formed hole is substantially cylindrical.

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15. The process of claim 13 further comprising the steps of;

coating said conductive layer on said dielectric layer with an insulating layer;

connecting said substrate to ground; and

connecting said conductive layer on said dielectric layer to a power source.

16. The process of claim 13 further comprising the steps of;

connecting said substrate to ground; and

connecting said conductive layer on said dielectric layer to a power source.

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17. A process of forming a capacitor on a semiconductor substrate having first and second major surfaces comprising the steps of:

forming an integrated circuit on said first major surface;

forming a substantially cylindrical hole through said substrate; said hole extending to a selected region of said integrated circuit;

forming a dielectric layer on said second major surface of said substrate and a dielectric lining on the wall of said through hole, said dielectric lining in said hole extending to said wiring level; and

depositing a conductive layer on said dielectric layer on said second major surface of said substrate and on said dielectric lining in said hole; said conductive layer coating said dielectric on said lining in said hole being substantially coaxial with said wall of said hole and extending though said hole and electrically contacting said selected region of said integrated circuit.

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18. A semiconductor integrated circuit comprising:

a semiconductor substrate having first and second major surfaces;

said first one of said major surfaces having an integrated circuit formed thereon;

an opening having extended walls passing between said first and second surfaces;

a first insulator disposed on said second major surface and on the walls of said opening;

a first metallic deposit formed on said insulator on said major surface and on the insulator on said walls.

a second insulator disposed on said first metallic deposit and over the first metallic layer on the walls of said opening; and

a second metallic deposit formed on said second insulator on said major surface and on said second insulator on said walls.

19. The circuit of claim 18 wherein said second metallic coating is further covered with an insulator.

20. The circuit of claim 18 wherein said first and second metallic layers are electrically connected to respective point on said integrated circuit on said first major surface.

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21. The circuit of claim 20 wherein said first metallic layer is connected to a voltage and forms one plate of a capacitor and said second metallic layer is connected to ground and forms the second plate of said capacitor.

22. The circuit of claim 18 wherein said substrate is formed of silicon, said insulator is selected from the group consisting of polyamide, silicon nitride, and silicon dioxide.

23. The circuit of claim 18 wherein said insulator is at least 50 x 10^{-8} cm in thickness and said metallic deposit is selected from the group consisting of tungsten, copper, gold, lead, aluminum, tin, copper aluminum, titanium , chrome and alloys thereof.

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24. A process of forming a capacitor on a semiconductor substrate having first and second major surfaces comprising the steps of:

forming an integrated circuit on said first major surface;

forming a first substantially cylindrical hole through said substrate; said hole extending to a first selected region of said integrated circuit;

forming a first dielectric layer on said second major surface of said substrate and a dielectric lining on the wall of said through hole, said dielectric lining in said hole extending to said wiring level; and

depositing a first conductive layer on said dielectric layer on said second major surface of said substrate and on said dielectric lining in said hole; said conductive layer coating said dielectric on said lining in said hole being substantially coaxial with said wall of said hole and extending though said hole and electrically contacting said first selected region of said integrated circuit;

forming a second substantially cylindrical hole through said substrate; said hole extending to a second selected region of said integrated circuit;

forming a second dielectric layer on said first conductive layer on second major surface of said substrate and a dielectric lining on the wall of said second through hole, said dielectric lining in said hole

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extending to said wiring level; and

depositing a second conductive layer on said second dielectric layer on said second major surface of said substrate and on said dielectric lining in said second hole; said second conductive layer coating said dielectric on said lining in said hole being substantially coaxial with said wall of said hole and extending though said hole and electrically contacting said second selected region of said integrated circuit.

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