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(54) Title: SURFACE MOUNT IC STACKING METHOD AND DEVICE

(57) Abstract

Packaged surface mount (SMT) chips having matched top contacts and bottom contacts are stacked. Chip features are selected to provide the desired connectivity between chip layers with a greater ease of manufacture. In one embodiment, additional spacing and routing layers are optionally provided between layers. In another, chips are differentiated by optionally providing different conductor and/or nonvolatile cell configurations. In yet another, a minority of a substrate's contacts are configured for aligning with a dielectric region of a spacing layer or substrate to create very low capacitance signal paths between stacked chips.

