

Description

Field of invention

The present invention relates to examination of coins for authenticity and denomination, more particularly but not exclusively to an adjustment-free mechanism especially useful for the examination of coin material characteristics through the use of a low frequency electromagnetic field.

Background of the invention

It has long been recognized in the coin examining art that the interaction of an object with a low frequency electromagnetic field can be used to indicate, at least in part, the material composition of the object and thus whether or not the object is an acceptable coin and if acceptable its denomination. See, for example, U.S. Patent No. 3,059,749. It has also been recognized that such low frequency tests are advantageously combined with one or more tests at a higher frequency. See, for example, U.S. Patent No. 3,870,137 assigned to the assignee of the present invention. The optimum methods for low frequency testing have, in the past, used bridge circuits which incorporate testing of both phase and amplitude effects of coin interaction with an electromagnetic field.

Another technique which has been popular in the testing of coins has been the transmit-receive technique in which an electromagnetic field is created by an inductor adjacent one face of a coin and characteristics of the received signal adjacent the other face are examined as a step in determining the coin's authenticity and denomination. For example, each of U.S. Patent Nos. 3,599,771 and 3,741,363 discloses a transmitter coil creating an electromagnetic field at either end. Spaced adjacent each end of the transmitter coil is a secondary coil. The two secondary coils are electrically connected in series, and have opposing orientations with respect to the transmitting coil field. An unknown coin is placed between one secondary coil and the transmitting coil and a known coin is placed between the other secondary coil and the transmitting coil. The unknown coin is accepted only if the signal delivered by the secondary coils does not exceed a threshold value. Such an arrangement, of course, is suitable only for examination of one coin denomination per testing station.

U.S. Patent No. 3,966,034, assigned to the assignee of the present invention discloses a phase sensitive coin discrimination method and apparatus operating by the transmit-receive technique with particular utility in distinguishing between two similar coins such as the British 5P and the West German 1DM. Unlike the preferred embodiments of the present invention, the detailed embodiments of that patent operate at relatively high frequencies (for example 320 kHz) and rely upon differences in coin volume to help distinguish between otherwise similar coins.

U.S. Patent No. 4,086,527, upon which the preambles of the independent claims are based,

discloses a transmit-receive type coin examining apparatus in which the transmitter coil is driven by a controlled variable frequency oscillator operated at selected frequencies in the range of 5—300 kHz. The secondary or receiving coil is connected to an undisclosed "quantifying operator" circuit which obtains quantitative information regarding amplitude of the secondary signal and its phase with respect to the primary (transmitted) signal. A selector is arranged to select both the frequency at which the transmitter coil is driven and a reference value against which the information from the quantifying operator circuit is compared to determine acceptability. Thus, each coin is tested at a plurality of transmitter coil frequencies.

A United States application entitled "Low Frequency Phase Shift Coin Examination Method and Apparatus", Serial No. 295,138 filed August 21, 1981 and assigned to the assignee of the present invention (now issued as U.S. Patent No. 4,398,626 and corresponding to published U.K. Patent Application No. 2106683A) discloses a transmit-receive type coin examination method and apparatus in which a nonlinear amplifier is employed between the receiving inductor and the phase shift measuring means in order to introduce an additional phase shift which is inversely related to the amplitude of the output of the receiving inductor. The additional phase shift improves the capability of the apparatus of the application to discriminate between various coins and particularly to discriminate between coins which produce nearly the same phase shift as measured by phase shift measuring circuitry lacking the nonlinear amplifier disclosed in U.S. Serial No. 295,138.

European Patent Application 0 048 557, filed September 2, 1981, discusses an electronic coin validator having a transmit coil and a receive coil for performing tests of coin face area and coin resistance. An automatic gain control circuit is described for use in modifying signal amplitude to provide compensation. This gain control circuit apparently has as its basic input the received signal amplitude for a transmitted signal having a frequency below 1 kHz. At least one absolute adjustment is needed to set up the validator in production.

Generally, low frequency test apparatus require at least one tuning element and at least one tuning adjustment during the manufacturing of such apparatus to compensate for components having slightly different values within tolerance and for variations in component positioning which occur during the construction of the test apparatus. For example, in low frequency coin test apparatus employing a bridge circuit, the bridge circuit is normally tuned to both the amplitude and the phase of the signal received when an acceptable coin is in the test position. An additional problem long recognized in the coin testing art is the problem of how to compensate for component aging, for changes in the environment of the coin apparatus such as temperature

changes, and for similar disruptive variations which result in undesirable changes in the operating characteristics of the electronic circuits employed in coin test apparatus.

Various discrete compensation circuits have been developed to meet this problem. See, for example, U.S. Application No. 308,548, filed October 2, 1981 and assigned to the assignee of the present invention, and published European Patent Specification Nos. 0034887, 0059511 and 0059512.

Summary of the invention

Aspects of the present invention are set out in the accompanying claims. The preferred embodiment relates to a method and apparatus for examining the interaction of coins with a relatively low frequency electromagnetic field at which the coin material plays a significant role. The transmit-receive technique is used and the phase shift that results from the presence of a coin or other object between the transmitting inductor, which creates the field, and the receiving inductor is used as an indication of the identity of the coin. The preferred embodiment provides a novel method and apparatus which eliminates the need for any tuning adjustments related to the low frequency test and also eliminates the need for discrete compensation circuitry. This is achieved by monitoring the frequency of the transmitted signal and adjusting the coin identification criterion based upon the monitored frequency of the transmitted signal.

Other features and advantages of the invention will be clear from the drawings and the detailed description of an embodiment of the invention which follows.

Description of drawings

Fig. 1 is a schematic block diagram of an embodiment of the coin examining circuit in accordance with the invention;

Fig. 2 graphically illustrates the signals produced at the points (a)—(d) in the coin examining circuit of Fig. 1.

Fig. 3 is a graph of phase shift count versus reference period for 25-cent coins;

Fig. 4 is a schematic diagram illustrating the incorporation into a coin handling mechanism of transmit and receive inductors suitable for the embodiment of Fig. 1;

Fig. 5 is a cross-sectional view of a coin passageway along line 3—3 of Fig. 4 showing one arrangement of transmitting and receiving inductors suitable for the embodiment of Fig. 1;

Fig. 6 illustrates a transmitting inductor suitable for the embodiment of Fig. 1;

Fig. 7 is a detailed schematic diagram of a circuit suitable for the embodiment of Fig. 1.

Although coin selector apparatus constructed in accordance with the principles of this invention may be designed to identify and accept any number of coins from the coin sets of many countries, the invention will be adequately illustrated by explanation of its application to identify-

ing the U.S. 5-, 10-, and 25-cent coins. The figures are intended to be representational and are not necessarily drawn to scale. Throughout this specification the term "coin" is intended to include genuine coins, tokens, counterfeit coins, slugs, washers, and any other item which may be used by persons in an attempt to use coin-operated devices. Furthermore, from time to time in this specification, for simplicity, coin movement may be described as rotational motion; however, except where otherwise indicated, translational and other types of motion also are contemplated. Similarly, although specific types of logic circuits are disclosed in connection with the embodiments described below in detail, other logic circuits can be employed to obtain equivalent results without departing from the invention.

Detailed description

Fig. 1 shows a block schematic diagram of a coin examining circuit 1 in accordance with the present invention. The coin examining circuit 1 includes a transmitter 10 having a transmitting inductor 32, a receiver 20 having a receiving inductor 32a, a first squaring circuit 30 with one input connected to the transmitter 10 and its output connected as a feedback input to the transmitter 10, a second squaring circuit 40 with an input connected to the receiver 20, gating circuit 50 connected to outputs of the squaring circuits 30 and 40, a counter 60 connected to the output of gating circuit 50, and a logic control means 80 is connected to the transmitter 10, the output of the first squaring circuit 30, one input of gating circuit 50, a reset input of the counter 60 and the output of the counter 60 which is shown in Fig. 1 as an eight bit parallel connection.

The operation of coin examining circuit 1 is as follows. The transmitter 10 produces a sine wave oscillator signal which drives transmitting inductor 32. In this embodiment, this sine signal is a low frequency signal with a resonant frequency of 5 kHz. Inductor 32 produces an electromagnetic field in a test region of a coin passageway (see Fig. 4 and the discussion thereof below for details of the relationship of the transmitting inductor 32, coin passageway and receiving inductor 32a). The oscillator signal is transmitted by transmitting inductor 32 across the low frequency test region. As a coin passes through the test region between inductors 32 and 32a, it is subjected to the electromagnetic field and a phase shift dependent upon the coin's material is introduced. The receiving inductor 32a receives a phase shifted signal which has been transmitted across the coin passageway.

The phase difference between the signal transmitted by transmitter 10 (transmitted signal) and the signal received by receiver 20 (received signal) is indicative of coin material and is measured as discussed below. The sine wave signal produced by transmitter 10 is fed as an input to the first squaring circuit 30. Squaring circuit 30 transforms by conventional means the sine wave connected to its input into a square

wave which appears at its output. The signal received by receiver 20 is connected to the input of the second squaring circuit 40 which inverts the sine wave at its input and similarly transforms the inverted sine wave into a square wave appearing at its output. The square wave outputs of both of the squaring circuits 30 and 40 along with a rapid clock signal from logic control means 80 serve as the inputs of gating circuit 50. Gating circuit 50 ANDs together the signals applied to its inputs. The output of the gating circuit 50 consists of a series of bursts of pulses with the number of pulses in each burst being indicative of the phase shift between the transmitted and the received signals.

The relationship of the various waveforms and signals discussed above is illustrated in Fig. 2. Waveforms 2(a)—2(d) are representative of typical waveforms which might be observed at the points (a)—(d) shown in Fig. 1. Fig. 2(a) shows a sine wave output signal for transmitter 10 having a period (T) of 200 μ sec and a frequency (f) of 5 kHz. Fig. 2(b) shows the square wave output of first squaring circuit 30 when the waveform of Fig. 2(a) is applied as its input. It should be noted that this square wave output has the same frequency as the input sine wave. Fig. 2(c) shows the output of second squaring circuit 40. The output of second squaring circuit 40 consists of its input signal squared and inverted. Finally, Fig. 2(d) shows the output of the gating circuit 50 which consists of a series of bursts of pulses.

The output of gating circuit 50 is connected to an input of the counter 60 which counts the number of pulses in each burst and produces an output count signal indicative thereof. The output count signal of counter 60 is supplied as one input to the logic control means 80. Between bursts, a reset signal is supplied by the logic control means 80 to an input of counter 60 so that the counter 60 is reset before each burst.

A second input of logic control means 80 is connected to the output of the first squaring circuit 30. The logic control means 80 continually monitors the frequency of the transmitted signal by monitoring the frequency of the output of the first squaring circuit 30. Based upon the frequency of the transmitted signal just prior to or just after the time when an output count signal is fed to logic control means 80 by counter 60, the logic control means 80 determines an acceptable phase shift for an acceptable coin. For example, the logic control means 80 may produce a signal indicative of a number or a range of numbers corresponding to those for an acceptable coin at the monitored frequency. This signal is then compared with the output from counter 60 and the logic control means 80 produces an output signal indicative of whether the coin passing through the test region of the coin passageway is an acceptable coin or not.

Fig. 3 shows a plot of phase shift count ϕ for acceptable 25-cent coins versus the reference period T in microseconds of the transmitted

signal, where the reference period T is the reciprocal of the reference or monitored frequency f of the transmitted signal. This plot was experimentally determined using apparatus according to the present invention. From the plot of Fig. 3, it can be seen that for 25-cent coins the phase shift count

$$\phi = 86 + 0.30 (T - 175)$$

or

$$\phi \approx 86 + (1/4 + 1/32 + 1/64) (T - 175).$$

Such information can be stored in logic control means 80 using any suitable means, such as storing a look-up table, or can be generated by a program such as a microprocessor program or a similar computing means. Like information for 10-cent and 5-cent coins can similarly be determined and stored in the logic control means 80 when the coin examining circuit 1 is to be used for examining United States coins. It is readily apparent that the system described above can be easily adapted to any other coin set by storing the appropriate phase count information for that coin set in the logic control means 80.

The above-described coin examining circuit 1 avoids the need for factory tuning to adjust for different component values within component tolerance or for positioning errors within manufacturing tolerance in positioning the transmitting inductor 32 and the receiving inductor 32a. Further, the above described coin examining circuit 1 avoids the need for retuning due to component aging, power supply drift or the like and also avoids the need for discrete compensation circuitry to compensate for component aging, drift or the like and environmental changes such as temperature changes. The adjustment free operation of coin examining circuit 1 results from the fact that for apparatus according to the described embodiment of the invention, the phase shift count depends only on the frequency of the transmitted signal which is continually monitored and taken into consideration by logic control means 80 in making the coin acceptance decision. Other variables such as the value of the transmitter and receiver inductances, the separation of the transmitter and receiver inductors 32 and 32a, the coin position with respect to the coils 32 and 32a when the coin is in the test position and variations in the component values of other components in the coin examining circuit 1, either have an insignificant effect on the phase shift count or result in a change in the frequency of the transmitted signal and consequently are compensated for by logic control means 80.

The incorporation of this embodiment into a coin handling mechanism is illustrated in Figs. 4 and 5. Figs. 4 and 5 show the mechanical portion of a coin handling apparatus 11 including transmitter and receiver inductors 32 and 32a appropriately located along a coin passageway. (A relatively higher frequency inductive coin examining circuit, such as that disclosed in a United States Patent Application entitled "Coin

Examination Apparatus Employing an RL Relaxation Oscillator", Serial No. 294,997, filed August 21, 1981 and assigned to the assignee of this invention corresponding to published International Application No. WO 83/00762, can be advantageously incorporated in the same apparatus for more complete testing of coin characteristics. The locations of inductors as disclosed in an embodiment of that application are indicated by the broken lines 37 and 39 in Fig. 4 of the present application).

The coin handling apparatus 11 also includes a conventional coin receiving cup 31, and two spaced sidewalls 36 and 38, connected by a hinge and spring assembly 34 in a manner similar to that shown in U.S. Patent No. 3,970,086, except that the retarding apparatus for sidewall closing disclosed in that patent is not necessarily used. The sidewalls 36, 38 are tipped slightly from the vertical so that the coins bear facially on the sidewall in which the receiver inductor 32a is located, here the front sidewall 38. The portions of the apparatus 11 shown in Figs. 4 and 5 also include a first coin track 33 under the coin entry cup 31 comprising an edge of a first energy dissipating device, and a second coin track 35 comprising an edge of a second energy dissipating device 35a, which forms the initial track section, and a terminal track section which is molded from plastic along with the sidewall 36. The energy dissipating devices 33, 35a, track 35 and sidewalls 36 and 38 form a coin passageway from the coin entry cup 31 past the coin testing inductors 32 and 32a. Coins entering the apparatus 11 fall edgewise onto a first energy dissipating element 33, roll off and fall onto a second energy dissipating element 35a which forms the initial section of a coin track 35 on which the coins roll past the transmitter inductor 32 and the receiver inductor 32a.

The transmitter inductor 32, shown in Fig. 6, is a type designed to produce a projecting magnetic field from its ends. The core 26 of the transmitter inductor 32 is dumbbell shaped, in this case, having two relatively large diameter cylindrical end pieces connected by a smaller diameter central section. The coil 27 is wound about the central section of the core 26 and the ends of the coil 27 are connected to leads 28a and b.

As shown in Figs. 4 and 5, the transmitter inductor 32 is located in a recess in the plastic back sidewall 36 of the coin apparatus with one end 29 adjacent the coin passageway formed by sidewalls 36 and 38. In a recess in the opposite, front sidewall 38 is the receiver inductor 32a. It is of the conventional pot core type. The axes of the two inductors 32 and 32a coincide in this embodiment, although they need not do so in all embodiments of the invention.

In this embodiment, which is designed primarily for identification of United States coinage, the nearest faces of the inductors 32 and 32a are about 3.8 mm apart. The axes of the inductors 32 and 32a are located 9.77 mm above the track 35

on which coins roll as they pass through the coin testing section of the apparatus. It is an important benefit of the present embodiment that positioning errors within normal manufacturing tolerances have no significant effect on the effectiveness of the low frequency test and such positioning errors do not result in a requirement for a tuning adjustment. The transmitter inductor 32 is 10 mm long by 8 mm in diameter with a central section 3.6 mm long, and has an inductance of 10 mH. The receiver inductor 32a is approximately 7 mm deep by 13.63 mm in diameter and has an inductance of 23 mH.

Fig. 7 is a detailed schematic diagram of the circuit 1 shown in Fig. 1 in block form. As discussed above, the transmitter 10 includes a transmitter inductor 32 and produces a low frequency sine wave signal, the transmitted signal, which is coupled to the input of the squaring circuit 30. Fig. 7 shows this coupling as being through a capacitor C2. The squaring circuit 30 is based upon a comparator 135 which may suitably be one section of a National Semiconductor type LM339 open collector comparator. The output of comparator 135 is a first square wave having the same frequency as the sine wave signal produced by transmitter 10. This first square wave output provides pulses of drive current through resistor R1 to the base of transistor T1. The square wave output of comparator 135 also serves as one input of gating circuit 50.

A second input of gating circuit 50 is connected to the output of the second squaring circuit 40. A first comparator 145 in squaring circuit 40 inverts the received signal from receiver 20. A second comparator 146 transforms the inverted output from comparator 145 into a second square wave output. Both of the comparators 145 and 146 may consist of one section of a National Semiconductor type LM339 open collector comparator.

A third input of gating circuit 50 is connected to a clock output of a logic means 80 such as an Intel type 8048 microprocessor. The gating circuit 50 consists of two 3-input NAND gates 151 and 152, such as National Semiconductor type 74LS10, connected together as an AND gate. The three inputs to gating circuit 50 are connected as the three inputs of NAND gate 151 and the output of NAND gate 151 is connected to all three inputs of NAND gate 152 so that NAND gate 152 serves as an inverter.

The input of gating circuit 50 is a series of pulse bursts with the number of pulses in each burst being indicative of the phase shift between the transmitted signal and the received signal. The number of pulses in each burst relates to the phase shift as follows. Each burst occurs during the time that the outputs of the squaring circuits 30 and 40 are both high. The number of pulses in each burst is the number of clock pulses from the clock output of microprocessor 80 occurring during that time. Since the time of coincidence of high outputs from the squaring circuits 30 and 40 is directly related to the phase shift between the transmitted and the received signals, the number

of pulses in each burst is an indication of the phase shift.

The number of pulses at the output of gating circuit 50 and the phase shift produced by any coin under test will vary depending on the frequency of the transmitted signal. Circuit 1 compensates for any frequency change as follows. Microprocessor 80 monitors the frequency of the signal applied to its input 181. The output of first squaring circuit 30 is connected to the input 181. Since the output of squaring circuit 30 is a square wave having the same frequency as the transmitted signal, the microprocessor 80 monitors the frequency of the transmitted signal by monitoring the output of squaring circuit 30. Depending upon the frequency of the signal applied to input 181, microprocessor 80 determines a count or a range of counts corresponding to those for an acceptable coin and the monitored frequency. For example, microprocessor 80 may store phase shift counts or an equation for computing phase shift counts from the monitored frequency for 5-, 10-, and 25-cent coins as discussed above with regard to Fig. 3 and determine therefrom an appropriate count for the monitored frequency.

The output of gating circuit 50 is connected to a counter 60, such as a National Semiconductor type 4520 counter, which produces an output count signal corresponding to the number of pulses in each burst of the output of gating circuit 50. This count signal is fed as an eight-bit parallel input to inputs 182—189 of microprocessor 80. The microprocessor 80 compares the count fed to inputs 182—189 with the count determined for an acceptable coin and the monitored frequency, and determines if the coin under test has the material of an acceptable coin. An output 191 of microprocessor 80 is connected to a reset input of counter 60. After each count is fed from counter 60 to microprocessor 80, microprocessor 80 produces a reset signal at its output 191 so that counter 60 is reset between the bursts appearing at the output of gating circuit 50.

In a preferred embodiment of the circuit 1, the following components and component values are used:

Inductors	32	10 mH
	32a	23 mH
Resistors	R1	100 k
	R2	100 k
	R3	100 k
	R4	1 k
	R5	10 M
	R6	1 k
	R7	470 k
	R8	2.2 k
	R9	1.2 k
	R10	27 k
	R11	4.7 k
	R12	2.2 k
	R13	4.7 k
	R14	4.7 k
	R15	4.7 k
	R16	1 k
Capacitors	C1	.1 uF
	C2	.1 uF
	C3	82 pF
	C4	8 pF
	C5	1 uF
	C6	.001 uF
	C7	.01 uF
Transistors	T1	2N3563
	T2	2N3563
Diode	D1	1N4148

Claims

1. A method of testing a coin comprising generating a varying magnetic field and comparing the effect of the coin on the varying magnetic field with an acceptable effect to determine whether the coin is acceptable, wherein, in use, the frequency of variation of the magnetic field may change and the acceptable effect is arranged to differ in correspondence with said frequency changes, characterised in that the frequency of variation of the magnetic field is monitored, and that the acceptable effect is determined in response to the monitored frequency.

2. A method as claimed in claim 1, wherein the frequency of variation of the magnetic field is in the range of 1 to 75 kHz.

3. A method as claimed in claim 1, wherein the frequency of variation of the magnetic field is approximately 5 kHz.

4. A method as claimed in any preceding claim, comprising the steps of transmitting a first, low frequency electrical signal with a first inductor (32) to generate said varying magnetic field, monitoring the frequency of the first low frequency electrical signal, receiving a portion of the transmitted signal with a second inductor (32a) and producing a second, received signal, measuring the phase shift between the transmitted signal and the received signal when the coin is between the first and second inductors (32, 32a), determin-



of pulses in each burst is an indication of the phase shift.

The number of pulses at the output of gating circuit 50 and the phase shift produced by any coin under test will vary depending on the frequency of the transmitted signal. Circuit 1 compensates for any frequency change as follows. Microprocessor 80 monitors the frequency of the signal applied to its input 181. The output of first squaring circuit 30 is connected to the input 181. Since the output of squaring circuit 30 is a square wave having the same frequency as the transmitted signal, the microprocessor 80 monitors the frequency of the transmitted signal by monitoring the output of squaring circuit 30. Depending upon the frequency of the signal applied to input 181, microprocessor 80 determines a count or a range of counts corresponding to those for an acceptable coin and the monitored frequency. For example, microprocessor 80 may store phase shift counts or an equation for computing phase shift counts from the monitored frequency for 5-, 10-, and 25-cent coins as discussed above with regard to Fig. 3 and determine therefrom an appropriate count for the monitored frequency.

The output of gating circuit 50 is connected to a counter 60, such as a National Semiconductor type 4520 counter, which produces an output count signal corresponding to the number of pulses in each burst of the output of gating circuit 50. This count signal is fed as an eight-bit parallel input to inputs 182—189 of microprocessor 80. The microprocessor 80 compares the count fed to inputs 182—189 with the count determined for an acceptable coin and the monitored frequency, and determines if the coin under test has the material of an acceptable coin. An output 191 of microprocessor 80 is connected to a reset input of counter 60. After each count is fed from counter 60 to microprocessor 80, microprocessor 80 produces a reset signal at its output 191 so that counter 60 is reset between the bursts appearing at the output of gating circuit 50.

In a preferred embodiment of the circuit 1, the following components and component values are used:

Inductors	
32	10 mH
32a	23 mH
Resistors	
R1	100 k
R2	100 k
R3	100 k
R4	1 k
R5	10 M
R6	1 k
R7	470 k
R8	2.2 k
R9	1.2 k
R10	27 k
R11	4.7 k
R12	2.2 k
R13	4.7 k
R14	4.7 k
R15	4.7 k
R16	1 k
Capacitors	
C1	.1 uF
C2	.1 uF
C3	82 pF
C4	8 pF
C5	1 uF
C6	.001 uF
C7	.01 uF
Transistors	
T1	2N3563
T2	2N3563
Diode	
D1	1N4148

Claims

1. A method of testing a coin comprising generating a varying magnetic field and comparing the effect of the coin on the varying magnetic field with an acceptable effect to determine whether the coin is acceptable, wherein, in use, the frequency of variation of the magnetic field may change and the acceptable effect is arranged to differ in correspondence with said frequency changes, characterised in that the frequency of variation of the magnetic field is monitored, and that the acceptable effect is determined in response to the monitored frequency.

2. A method as claimed in claim 1, wherein the frequency of variation of the magnetic field is in the range of 1 to 75 kHz.

3. A method as claimed in claim 1, wherein the frequency of variation of the magnetic field is approximately 5 kHz.

4. A method as claimed in any preceding claim, comprising the steps of transmitting a first, low frequency electrical signal with a first inductor (32) to generate said varying magnetic field, monitoring the frequency of the first low frequency electrical signal, receiving a portion of the transmitted signal with a second inductor (32a) and producing a second, received signal, measuring the phase shift between the transmitted signal and the received signal when the coin is between the first and second inductors (32, 32a), determin-



ing an acceptable phase shift for an acceptable coin based upon the monitored frequency, and comparing the measured phase shift and the acceptable phase shift.

5. A method as claimed in claim 4, comprising the further step of generating said first low frequency electrical signal.

6. A method as claimed in claim 4 or 5, wherein the frequency of the first signal is monitored by squaring the first signal so that a first square wave signal having the same frequency as the first signal is produced, and monitoring the frequency of the first square wave signal.

7. A method as claimed in claim 6, wherein the phase shift between the first signal and the second signal is measured by inverting and squaring the second signal so that a second square wave signal 180° out of phase and having the same frequency as the second signal is produced, generating a rapid clock signal, and logically gating the first square wave signal, the second square wave signal and the rapid clock signal so that a plurality of output pulses are produced at the output of a logic gate means (50) whenever the first square wave signal, the second square wave signal and the rapid clock signal are all coincidentally high.

8. A method as claimed in claim 7, further comprising counting the output pulses at the output of the logic gate means (50) and generating a first phase shift count indicative of the measured phase shift between the first signal and the second signal.

9. A method as claimed in claim 8, wherein the acceptable phase shift is determined by using the frequency of the first square wave signal to calculate an acceptable phase shift count.

10. A method as claimed in claim 9, further comprising the step of storing an equation relating the acceptable phase shift count to the frequency of the first signal and wherein the acceptable phase shift count is calculated by solving the stored equation using the monitored frequency of the first square wave signal.

11. A method as claimed in any one of claims 4 to 10, wherein the acceptable phase shift consists of a range of acceptable phase shift counts.

12. A method as claimed in claim 11, further comprising the steps of producing a measured phase shift count based upon the measured phase shift between the first and second signals and producing a signal indicative of an acceptable coin when the measured phase shift count falls within the range of acceptable phase shift counts.

13. Apparatus for testing a coin, the apparatus being operable to generate a varying magnetic field, the frequency of variation of which may change in use, and to compare the effect of a coin on the field with an acceptable effect, which is arranged to differ in correspondence with said frequency changes, to determine whether the coin is acceptable, characterised in that the apparatus has means (30, 80) for monitoring to the frequency of variation of the magnetic field, and means (80) for determining said acceptable effect in response to the monitored frequency.

14. Apparatus for examining coins, comprising: means defining a coin passageway, means (C1, R1, T1, R9) for producing a first low frequency electrical signal,

a first inductor (32) connected to the output of the first signal producing means (C1, R1, T1, R9), the first inductor (32) being located on one side of the coin passageway and arranged to produce an electromagnetic field in the coin passageway,

a second inductor (32a) located on the other side of the coin passageway from the first inductor (32) so that coins to be examined will pass between the first and second inductors (32, 32a), the second inductor (32a) being arranged to receive a portion of the field and to produce a second low frequency signal as its output,

means (50, 60) to measure the phase shift between the first signal and the second signal, and means (80) to compare the measured phase shift and an acceptable phase shift for an acceptable coin,

the apparatus being characterised by:

means (30, 80) to monitor the frequency of the first signal, and

means (80) to determine said acceptable phase shift based upon the monitored frequency of the first signal.

15. Apparatus as claimed in claim 14, wherein the frequency of the first signal is in the range of 1 to 75 kHz.

16. Apparatus as claimed in claim 14, wherein the frequency of the first signal is approximately 5 kHz.

17. Apparatus as claimed in claim 14, 15 or 16, wherein the means (C1, R1, T1, R9) for producing the first signal comprises an oscillator having its output connected to the first inductor (32).

18. Apparatus as claimed in any one of claims 14 to 17, wherein the means (30, 80) to monitor the frequency of the first signal comprises a first squaring circuit (30), the first squaring circuit (30) producing a first square wave at its output and having an input connected to the output of the means (C1, R1, T1, R9) for producing the first signal.

19. Apparatus as claimed in claim 18, wherein the first squaring circuit (30) further comprises a second input connected to a biasing circuit and wherein its output is connected to a first input (181) of a logic means (80).

20. Apparatus as claimed in claim 19, wherein the logic means (80) comprises a microprocessor having a plurality of inputs, the microprocessor (80) being programmed to determine the frequency of the signal applied to its first input (181).

21. Apparatus as claimed in claim 20, wherein the microprocessor (80) is programmed to calculate the acceptable phase shift based upon the frequency of the signal applied to its first input (181).

Patentansprüche

1. Verfahren zur Prüfung einer Münze, bei dem ein wechselndes Magnetfeld erzeugt wird, und zur



Feststellung, ob die Münze akzeptabel ist, die Wirkung der Münze auf das wechselnde Magnetfeld mit einer akzeptablen Wirkung verglichen wird, wobei sich im Betrieb die Frequenz der Magnetfeldänderungen ändern kann, und die akzeptable Wirkung angelegt ist, um in Übereinstimmung mit den Frequenzänderungen zu variieren, dadurch gekennzeichnet, daß die Frequenz der Magnetfeldänderung überwacht wird, und die akzeptable Wirkung in Reaktion auf die überwachte Frequenz bestimmt wird.

2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß die Frequenz der Magnetfeldänderung im Bereich von 1 bis 75 kHz liegt.

3. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß die Frequenz der Magnetfeldänderung etwa 5 kHz beträgt.

4. Verfahren nach einem der vorhergehenden Ansprüche, gekennzeichnet durch folgende Verfahrensschritte:

Senden eines ersten, niederfrequenten elektrischen Signals mit einem ersten Induktor (32) zur Erzeugung eines sich ändernden Magnetfeldes,

Überwachen der Frequenz des ersten niederfrequenten elektrischen Signals,

Empfangen eines Teils des gesendeten Signals mit einem zweiten Induktor (32a) und Erzeugung eines zweiten Empfangssignals,

Messung der Phasenverschiebung zwischen dem gesendeten und dem empfangenen Signal, wenn die Münze sich zwischen dem ersten und dem zweiten Induktor (32, 32a) befindet,

Bestimmung einer akzeptablen Phasenverschiebung für eine akzeptable Münze, basierend auf der überwachten Frequenz, und

Vergleich der gemessenen Phasenverschiebung und der akzeptablen Phasenverschiebung.

5. Verfahren nach Anspruch 4, gekennzeichnet durch den weiteren Schritt der Erzeugung des ersten niederfrequenten elektrischen Signals.

6. Verfahren nach Anspruch 4 oder 5, dadurch gekennzeichnet, daß die Frequenz des ersten Signals durch Rechteckformung des ersten Signals überwacht wird, so daß ein erstes rechteckförmiges Signal mit der gleichen Frequenz wie des ersten Signals erzeugt wird, und die Frequenz des ersten rechteckförmigen Signals überwacht wird.

7. Verfahren nach Anspruch 6, dadurch gekennzeichnet, daß die Phasenverschiebung zwischen dem ersten Signal und dem zweiten Signal gemessen wird durch Invertierung und Rechteckbildung des zweiten Signals, so daß ein zweites rechteckförmiges Signal um 180° phasenverschoben und mit der gleichen Frequenz wie das zweite Signal erzeugt wird; ferner ein schnelles Taktsignal erzeugt wird, und das erste rechteckförmige Signal, das zweite rechteckförmige Signal und das schnelle Taktsignal logisch ausgetastet werden, so daß eine Vielzahl von Ausgangsimpulsen am Ausgang einer logischen Torschaltung (50) erzeugt wird, wann immer das erste rechteckförmige Signal, das zweite rechteckförmige Signal und das schnelle Taktsignal gleichzeitig auf hohem Potential liegen.

8. Verfahren nach Anspruch 7, dadurch gekennzeichnet, daß außerdem die Ausgangsimpulse am Ausgang der logischen Torschaltung (50) gezählt werden, und ein erster Phasenverschiebungszählerstand erzeugt wird, der kennzeichnend ist für die gemessene Phasenverschiebung zwischen dem ersten Signal und dem zweiten Signal.

9. Verfahren nach Anspruch 8, dadurch gekennzeichnet, daß die akzeptable Phasenverschiebung dadurch bestimmt wird, daß die Frequenz des ersten rechteckförmigen Signals benutzt wird zur Berechnung eines akzeptablen Phasenverschiebungszählerstandes.

10. Verfahren nach Anspruch 9, ferner gekennzeichnet durch den Verfahrensschritt, daß eine Gleichung gespeichert wird, die einen akzeptablen Phasenverschiebungszählerstand in Bezug setzt zur Frequenz des ersten Signals und wobei der akzeptable Phasenverschiebungszählerstand durch Lösung der gespeicherten Gleichung unter Verwendung der überwachten Frequenz des ersten rechteckförmigen Signals errechnet wird.

11. Verfahren nach einem der Ansprüche 4 bis 10, dadurch gekennzeichnet, daß die akzeptable Phasenverschiebung aus einem Bereich akzeptabler Phasenverschiebungszählerstände besteht.

12. Verfahren nach Anspruch 11, gekennzeichnet durch die weiteren Verfahrensschritte der Erzeugung eines gemessenen Phasenverschiebungszählerstandes, basierend auf der gemessenen Phasenverschiebung zwischen dem ersten und dem zweiten Signal, und der Erzeugung eines Signals, das kennzeichnend ist für eine akzeptable Münze, wenn der gemessene Phasenverschiebungszählerstand innerhalb des Bereichs der akzeptablen Phasenverschiebungszählerstände fällt.

13. Vorrichtung zur Prüfung einer Münze, die zur Erzeugung eines wechselnden Magnetfeldes betreibbar ist, wobei sich die Wechselfrequenz im Betrieb verändern kann, und die Wirkung einer Münze auf das Feld verglichen wird mit einer akzeptablen Wirkung, die so angelegt ist, um in Übereinstimmung mit den Frequenzänderungen zu variieren, um festzustellen, ob die Münze akzeptabel ist, dadurch gekennzeichnet, daß die Vorrichtung mit Mitteln (30, 80) zur Überwachung der Frequenz der Magnetfeldänderung und Mitteln (80) zur Bestimmung der besagten akzeptablen Wirkung in Reaktion auf die überwachte Frequenz versehen ist.

14. Vorrichtung zur Prüfung von Münzen mit: Mitteln, die einen Münzdurchlaß definieren, Mitteln (C1, R1, T1, R9) zur Erzeugung eines ersten niederfrequenten elektrischen Signals, einem ersten Induktor (32), der mit dem Ausgang der ersten Signalerzeugungsmittel (C1, R1, T1, R9) verbunden ist, wobei der erste Induktor (32) auf einer Seite des Münzdurchlasses angeordnet ist und zur Erzeugung eines elektromagnetischen Feldes im Münzdurchlaß ausgebildet ist, einem zweiten Induktor (32a), der, bezogen auf den ersten Induktor (32), auf der anderen Seite des Münzdurchlasses angeordnet ist, so daß sich



die zu prüfenden Münzen zwischen dem ersten und dem zweiten Induktor (32, 32a) vorbeibewegen, wobei der zweite Induktor (32a) zum Empfang eines Teils des Feldes und zur Erzeugung eines zweiten niederfrequenten Signals an seinem Ausgang ausgebildet ist,

Mitteln (50, 60) zur Messung der Phasenverschiebung zwischen dem ersten Signal und dem zweiten Signal, und

Mitteln (80) zum Vergleich der gemessenen Phasenverschiebung mit einer akzeptablen Phasenverschiebung einer akzeptablen Münze, wobei die Vorrichtung gekennzeichnet ist durch:

Mitteln (30, 80) zur Überwachung der Frequenz des ersten Signals und

Mitteln (80) zur Bestimmung der akzeptablen Phasenverschiebung, basierend auf der überwachten Frequenz des ersten Signals.

15. Vorrichtung nach Anspruch 14, dadurch gekennzeichnet, daß die Frequenz des ersten Signals im Bereich von 1 bis 75 kHz liegt.

16. Vorrichtung nach Anspruch 14, dadurch gekennzeichnet, daß die Frequenz des ersten Signals etwa 5 kHz beträgt.

17. Vorrichtung nach Anspruch 14, 15 oder 16, dadurch gekennzeichnet, daß die Mittel (C1, R1, T1, R9) zur Erzeugung des ersten Signals einen Oszillator umfassen, dessen Ausgang mit dem ersten Induktor (32) verbunden ist.

18. Vorrichtung nach einem der Ansprüche 14 bis 17, dadurch gekennzeichnet, daß die Mittel (30, 80) zur Überwachung der Frequenz des ersten Signals einen ersten Rechteckformer (30) umfassen, der an seinem Ausgang einen ersten Rechteck erzeugt, und dessen Eingang mit dem Ausgang der Mittel (C1, R1, T1, R9) zur Erzeugung des ersten Signals verbunden ist.

19. Vorrichtung nach Anspruch 18, dadurch gekennzeichnet, daß der erste Rechteckformer (30) außerdem einen zweiten, mit einem Vorspannungsschaltkreis verbundenen Eingang umfaßt, und sein Ausgang mit dem ersten Eingang (181) der Logikschaltung (80) verbunden ist.

20. Vorrichtung nach Anspruch 19, dadurch gekennzeichnet, daß die Logikschaltung (80) einen Mikroprozessor mit einer Anzahl von Eingängen umfaßt, wobei der Mikroprozessor (80) programmiert ist, um die Frequenz des an seinem ersten Eingang (181) anliegenden Signals zu bestimmen.

21. Vorrichtung nach Anspruch 20, dadurch gekennzeichnet, daß der Mikroprozessor (80) zur Berechnung der akzeptablen Phasenverschiebung, basierend auf der Frequenz des an seinem ersten Eingang (181) anliegenden Signals, programmiert ist.

Revendications

1. Procédé pour contrôler une pièce de monnaie, consistant à introduire un champ magnétique variable et comparer l'effet de la pièce de monnaie sur le champ magnétique variable à un effet acceptable de manière à déterminer si la pièce de monnaie est acceptable, et selon lequel,

en fonctionnement, la fréquence de variation du champ magnétique peut varier et l'effet acceptable est conçu de manière à être différent en correspondance avec lesdites variations de la fréquence, caractérisé en ce que l'on contrôle la fréquence de variation du champ magnétique et qu'on détermine l'effet acceptable en réponse à la fréquence contrôlée.

2. Procédé selon la revendication 1, selon lequel la fréquence de variation du champ magnétique se situe dans la gamme de 1 à 75 kHz.

3. Procédé selon la revendication 1, selon lequel la fréquence de variation du champ magnétique est égale approximativement à 5 kHz.

4. Procédé selon l'une quelconque des revendications précédentes, incluant les étapes consistant à émettre un premier signal électrique à basse fréquence à l'aide d'une première inductance (32) de manière à produire ledit champ magnétique variable, contrôler la fréquence du premier signal électrique à basse fréquence, recevoir une partie du signal émis à l'aide d'une seconde inductance (32a) et produire un second signal reçu, mesurer le déphasage entre le signal émis et le signal reçu lorsque la pièce de monnaie est située entre les première et seconde inductances (32, 32a), déterminer un déphasage acceptable pour une pièce de monnaie acceptable sur la base de la fréquence contrôlée, et comparer le déphasage mesuré et le déphasage acceptable.

5. Procédé selon la revendication 4, incluant l'étape supplémentaire consistant à produire ledit premier signal à basse fréquence.

6. Procédé selon la revendication 4 ou 5, selon lequel on contrôle la fréquence du premier signal en donnant une forme carrée à ce premier signal de manière à obtenir un premier signal en onde carrée possédant la même fréquence que le premier signal, et contrôler la fréquence du premier signal en onde carrée.

7. Procédé selon la revendication 6, selon lequel on mesure le déphasage entre le premier signal et le second signal en inversant et en donnant une forme carrée au second signal, de manière à produire un second signal en onde carrée déphasé de 180° par rapport au second signal et possédant la même fréquence que ce dernier, produire un signal d'horloge rapide et commander logiquement le premier signal en onde carrée, le second signal en onde carrée et le signal d'horloge rapide de manière à produire une pluralité d'impulsions de sortie sur la sortie de moyens formant porte logique (50), chaque fois que le premier signal en onde carrée, le second signal en onde carrée et le signal d'horloge rapide présentent tous des niveaux élevés coïncidents.

8. Procédé selon la revendication 7, incluant en outre le comptage des impulsions de sortie apparaissant sur la sortie des moyens formant porte logique (50) et produire une première valeur de déphasage indicative du déphasage mesuré entre le premier signal et le second signal.

9. Procédé selon la revendication 8, selon lequel on détermine un déphasage acceptable en utilisant la fréquence du premier signal en onde



carrée pour calculer une valeur de déphasage acceptable.

10. Procédé selon la revendication 9, incluant en outre l'étape consistant à mémoriser l'équation reliant la valeur de déphasage acceptable à la fréquence du premier signal, et selon lequel on calcule la valeur de déphasage acceptable en résolvant l'équation mémorisée moyennant l'utilisation de la fréquence contrôlée du premier signal en onde carrée.

11. Procédé selon l'une quelconque des revendications 4 à 10, selon lequel le déphasage acceptable est constitué par une gamme de valeurs de déphasage acceptables.

12. Procédé selon la revendication 11, incluant en outre les étapes consistant à produire une valeur de déphasage mesurée, sur la base du déphasage mesuré entre les premier et second signaux et produire un signal indicatif d'une pièce de monnaie acceptable lorsque la valeur mesurée du déphasage se situe dans la gamme des valeurs de déphasage acceptables.

13. Appareil pour contrôler une pièce de monnaie, cet appareil pouvant fonctionner en produisant un champ magnétique variable, dont la fréquence de variation peut varier en cours d'utilisation, et comparer l'effet d'une pièce de monnaie sur le champ à un effet acceptable, qui est conçu de manière à différer en correspondance avec lesdites variations de la fréquence, pour déterminer si la pièce de monnaie est acceptable, caractérisé en ce que l'appareil comporte des moyens (30, 80) servant à contrôler la fréquence de variation du champ variable, et des moyens (80) servant à déterminer ledit effet acceptable en réponse à la fréquence contrôlée.

14. Appareil pour examiner des pièces de monnaie, comprenant:

des moyens définissant un passage pour les pièces de monnaie,

des moyens (C1, R1, T1, R9) servant à produire un premier signal électrique à basse fréquence, une première inductance (32) raccordée à la sortie des moyens (C1, R1, T1, R9) de production du premier signal, la première inductance (32) étant située d'un côté du passage des pièces de monnaie et étant agencée de manière à produire un champ électromagnétique dans le passage des pièces de monnaie,

une seconde inductance (32a) située de l'autre côté du passage des pièces de monnaie par rapport à la première inductance (32) de sorte que les pièces de monnaie devant être examinées passent entre les première et seconde induc-

tances (32, 32a), la seconde inductance (32a) étant agencée de manière à recevoir une partie du champ et à produire un second signal à basse fréquence au niveau de sa sortie,

des moyens (50, 60) servant à mesurer le déphasage entre le premier signal et le second signal, et

des moyens (80) servant à comparer le déphasage mesuré et un déphasage acceptable pour une pièce de monnaie acceptable,

l'appareil étant caractérisé par des moyens (30, 80) servant à contrôler la fréquence du premier signal, et

des moyens (80) servant à déterminer ledit déphasage acceptable sur la base de la fréquence contrôlée du premier signal.

15. Appareil selon la revendication 14, dans lequel la fréquence du premier signal se situe dans la gamme de 1 à 75 kHz.

16. Appareil selon la revendication 14, dans lequel la fréquence du premier signal est égale à environ 5 kHz.

17. Appareil selon la revendication 14, 15 ou 16, dans lequel les moyens (C1, R1, T1, R9) servant à produire le premier signal comprennent un oscillateur, dont la sortie est raccordée à la première inductance (32).

18. Appareil selon l'une quelconque des revendications 14 à 17, dans lequel les moyens (30, 80) servant à contrôler la fréquence du premier signal comportent un premier circuit de mise sous forme carrée (30), le premier circuit de mise sous forme carrée (30) produisant une première onde carrée à sa sortie, tandis que son entrée est raccordée à la sortie des moyens (C1, R1, T1, R9) de manière à produire le premier signal.

19. Appareil selon la revendication 18, dans lequel le premier circuit de mise en forme carrée (30) comprend en outre une seconde entrée raccordée à un circuit de polarisation, et dans lequel la sortie du circuit de mise en forme carrée est raccordée à une première entrée (181) de moyens logiques (80).

20. Appareil selon la revendication 19, dans lequel les moyens logiques (80) comprennent un microprocesseur possédant une pluralité d'entrées, le microprocesseur (80) étant programmé de manière à déterminer la fréquence du signal appliqué à sa première entrée (181).

21. Appareil selon la revendication 20, dans lequel le microprocesseur (80) est programmé de manière à calculer le déphasage acceptable sur la base de la fréquence du signal appliqué à sa première entrée (181).

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