SPECIFICATION

Recording circuit

The present invention relates to a recording circuit used for a tape recorder and, more particularly, to a bias circuit for the recording circuit.

It is a common practice that a parallel bias supply system is used in a recording bias circuit typically found found in a combination stereo tape recorder and a radio. In the bias supply system, a recording amplifier as a recording signal source and a bias oscillator as a bias signal source are arranged in parallel circuit fashion. Since the bias voltage applied to a recording head is high, the bias supply system needs a bias strap circuit between the bias oscillator output and a recording amplifier output circuit.

The bias trap is used to prevent the undesirable facts that the recording amplifier is saturated by a high voltage bias and that the output impedance of the recording amplifier serves as a load for the bias oscillator. For this reason, an LC parallel resonance circuit exhibiting an extremely high impedance at the bias oscillating frequency is connected in series as a bias trap between the bias oscillator and the recording amplifier. The provision of the bias trap prevents the high bias voltage from being applied to the recording amplifier and prevents the output circuit of the recording amplifier from serving as a load for the bias oscillator circuit. The LC bias trap must have a high quality factor Q for its purpose. Therefore, the adjustment of the bias trap is critical. In a 2-channel stereo tape recorder, the adjustment of the bias trap for each channel must be performed individually.

To avoid the troublesome adjustment of the bias trap and to reduce the manufacturing cost, there was proposed a series bias supply system in the days prior to stereo. The series bias supply system has the secondary coil of the oscillator transformer of the bias oscillator connected in series between the recording amplifier and the recording head, and a by-pass capacitor connecting to the connecting point between the secondary coil and the recording amplifier. In the system, the output circuit of the recording amplifier does not serve substantially as a load for the bias oscillator. Therefore, no bias trap is necessary.

No stereophonic tape recording which uses the series bias supply system is known hitherto. This is perhaps because it is commonly believed that two secondary coils should be provided for the oscillator transformer when the series bias supply system developed for the monoral type device is employed in the stereophonic device, without any modification. The ends of each of the secondary coils are not grounded. That is to say, these ends are floated, and they are magnetically coupled through the oscillator transformer. Since the recording head is driven in a constant current mode, the impedance of the recording output circuit is high. Due to these facts that the magnetic coupling between the secondary coils and the recording circuit is at a high impedance, and that both ends of the secondary coils float from ground, the channel separation is deteriorated by the electromagnetic coupling, particularly between the two secondary coils. It is for this reason that the bias circuit in the stereo tape recorder inevitably uses the parallel bias supply system needing the bias trap.

A conventional stereo tape recorder with a radio employing the parallel power supply system involves an important problem to be solved, in addition to the need for the bias trap. The problem is that a higher harmonics distortion component of the bias oscillator enters an RF circuit or an IF circuit of an AM tuner so that the interference is frequently recorded.

In general circuit design, the higher harmonics distortion of the bias oscillator is restricted below 1 % or less (approximately 0.3 %). Let us consider a case where the bias oscillator frequency is 60 KHz, the impedance of the recording head is 33 KΩ at 60 KHz and the bias current is 0.3 mA. In this case, about 10 V of bias voltage is applied to the recording head. If the distortion of the 15th harmonic of the bias oscillator is 0.01 %, 1 mV/900 KHz of high frequency voltage is applied to the recording head. The high frequency signal is radiated as an electromagnetic wave from any place of the path from the bias oscillator to the recording head.

The maximum sensitivity of the AM tuner is very high, for example, on the order of several tens dB/m (OdB = 1 V/m). For this reason, a higher harmonics distortion component of the bias oscillator, i.e. that ranging from the 10th (600 KHz) to the 25th (1.5 MHz) is liable to enter the AM tuner section. Therefore, great care must be taken in arranging parts or positioning the shielding within the radio set.

An object of the invention is to provide a recording circuit in use for a multi-channel type tape recorder, particularly a two-channel stereo tape recorder with a radio, which needs no bias trap and prevents an undesirable radiation by higher harmonics component of the bias current frequency.

To achieve the above object, there is provided a recording circuit comprising: a multi-channel recording head of which each channel receives a recording signal and has a first and a second terminal; impedance means for bypassing a bias current connected to a first terminal of the respective channel and an AC potential-zero circuit having substantially zero AC potential; the magnitude of the impedance of the impedance means at the bias current frequency being less than that at the recording signal frequency; a bias oscillator, which constitutes an even number of bias signal sources for providing bias currents with the same frequencies to the respective channels of said recording head, including a first bias signal source which is connected via a first phase terminal to a second terminal of one channel of said recording head and which is connected via a second phase terminal, which is related in antiphase to the first phase terminal, to the AC potential-zero circuit, and including a second bias signal source which is connected via a third phase terminal to a second terminal of another channel of said recording head and which is connected via a fourth phase terminal, which is related in antiphase to the third phase terminal, to the AC potential-zero

circuit; and a first bias supply circuit extending from the first phase terminal, of the first bias signal source, to said one channel of said recording head and a second bias supply circuit extending from the third phase terminal, of the second bias signal source, to said other channel of said recording head, the first and second bias supply circuits being disposed in parallel in order to mitigate electromagnetic fields produced by higher harmonics components of said bias currents radiated from said first and second bias supply circuits.

With such a construction, since the impedance of the impedance element at the bias current frequency is small, the bias voltage appearing across of the impedance element connecting to one end of each channel of the recording head is small. Therefore, the bias trap is unnecessary. The phase (first phase) of the bias current at the other end of one channel is opposite to that (second phase) of the bias current at the other end of another channel. Therefore, an electromagnetic field produced by the bias current at one channel side is cancelled by the electromagnetic field developed by the bias current at another channel side. Accordingly, an electromagnetic field of higher harmonics of the bias current radiated from a bias current supply path has a very weak intensity.

A better understanding of the invention will be obtained from the following detailed description, in connection with the accompanying drawings, in which:

Figure 1 shows a basic construction of a recording circuit according to the invention;

Figure 2 shows a circuit diagram of the basic construction shown in Figure 1;

Figure 3 shows a circuit diagram of a modification of the circuit construction shown in Figure 2;

Figure 4 shows in block form another modification of the circuit construction shown in Figure 1 or 2;

Figures 5 to *11* show circuit constructions of the circuit construction shown in Figure 4.

Before explaining the invention in detail, it is to be understood that the philology and terminology employed herein is for the purpose of description and illustration only, and not for the purpose of limitation. Furthermore, throughout the drawings, like reference symbols are used to designate like or equivalent parts or portions for the purpose of simplicity. Specifically, those parts or portions designated by like symbols among preferred embodiments may be interchanged with, at most, only minor modification.

Reference is first made to Figure 1 illustrating a basic construction of a recording circuit according to the invention. A bias oscillating source 10 is connected to the primary coil of an oscillator transformer 12. The secondary coil of the transformer is divided into two; a first secondary coil 12_1 forming a first bias signal source and a second secondary coil 12_2 forming a second bias signal source. A second phase terminal *b* of the coil 12_1 (the second phase terminal) and a first phase terminal *c* of the second coil 12_2 (the fourth phase terminal) are connected to a circuit of which AC potential is substantially zero. The bifilar winding is preferable for winding the coils 12_1 and 12_2 in the light of the magnetic coupling balance. A usual single winding coil with a center tap may of course be used in place of the bifilar winding.

The first phase termimal *a* of the coil 12_1 is connected through a first bias supply path 14, to the first terminals of a first channel coil 16_1 and a third channel coil 16_3. The second terminals of the first channel coil 16_1 and the third channel coil 16_3 are grounded through impedance elements 18_1 and 18_3, respectively. Similarly, the second phase terminal *d* of the coil 12_2 (the third phase terminal) is connected through a second bias supply path 14_2 to the first terminals of a second channel coil 16_2 and a fourth channel coil 16_4. Coils 16_1 to 16_4 form the recording head 16. The components 10 and 12 cooperatively form a bias oscillator 13 for providing bias currents with the same frequency to the recording head 16. The second terminals of the second channel coil 16_2 and the fourth channel coil 16_4 are grounded through impedance elements 18_2 and 18_4, respectively. Connected to the second terminals of the first to fourth channel coils 16_1 to 16_4 are the output circuits of first to fourth recording amplifiers 20_1 to 20_4, respectively. To the input terminals of the first to fourth recording amplifiers 20_1 to 20_4 are applied AC signals e1 to e4 with audio frequencies to be recorded.

The impedances of the impedance elements 18_1 to 18_4 within the audio frequency band are much larger than those of the coils 16_1 to 16_4 within the same frequency band. For example, when the coils 16_1 to 16_4 each have an inductance of 0.1 H, and the impedance elements 18_1 to 18_4 each have a capacitance 1000 pF, the impedance of each of the impedance elements 18_1 to 18_4 at 1 KHz is 160 KΩ and the impedance of each of the coils 16_1 to 16_4 at 1 KHz is 0.63 KΩ. In such a case, first and third recording currents i1 and i3 derived from the first and third recording amplifiers 20_1 and 20_3 flow into the coils 16_1 and 16_3 without being substantially diverted by impedance elements 18_1 and 18_3. These recording currents i1 and i3 flow through the first bias supply path 14_1 and the coil 12_1 to ground. Similarly, second and fourth recording currents i2 and i4 fed from the second and fourth recording amplifiers 20_2 and 20_4 flow into the coils 16_2 and 16_4, without being substantially diverted by impedance elements 18_2 and 18_4. These recording currents i2 and i4 flow to ground, through the second bias supply path 14_2 and the coil 12_2.

The inductances of the coils 12_1 and 12_2 are selected to be relatively small so that their impendances are small at the audio frequency band. Particularly, when the recording currents i1 + i3 and i2 + i4 are considered to be the same in phase and level, the magnetic flux developed by the coil 12_1 bearing the current i1 + i3 is equal and opposite to the magnetic flux developed by the coil 12_2 bearing the sum i2 + i4. In this case, the effect impedances of the coils 12_1 and 12_2 for the recording circuits i1 to i4 are very small. The coils 12_1 and 12_2 are connected at one end (*b*, *c*) to ground. As seen from the foregoing, the cross-talk between the channel coils 16_1 to 16_4 is sufficiently small. Incidentally, when the cross-talk occurring through the oscillator transformer 12 is

noticeable, the recording currents i1 + i3 and i2 + i4 may be in opposite phase. The opposite phase relation between them does not hinder the achievement of the object of the present invention. In this case, if the wirings of the coils 16_1 and 16_3 or 16_2 and 16_4 are interchanged (the first terminals and the second terminals are interchanged), the signal to be recorded may be all aligned in phase for the respective channels 16_1 to 16_4.

The above description relates to only the recording current path in the audio frequency band; however, a quite different description is needed for the bias current path. Bias voltages e_a and e_d with the same frequencies and given amplitudes as those of the bias oscillating source are induced in the coils 12_1 and 12_2, respectively. In other words, the signal e_a appears at the first phase terminal *a* of the coil 12_1 and the signal e_d with a phase opposite to that of the signal e_a appears at the second phase terminal *d*. The bias current ib1 corresponding to the signal e_a is fed through the bias supply path 14_1 to the first and third channel coils 16_1 and 16_3. The current ib1 is divided into a current flowing through a first circuit including the coil 16_1 and the element 18_1 and a current flowing through a third circuit including the coil 16_3 and the element 18_3. Similarly, the bias current ib2 corresponding to the signal e_d flows through the bias supply path 14_2 to the second and the fourth channel coils 16_2 and 16_4. The current ib2 also is divided into a current flowing through a second circuit of the coil 16_2 and the element 18_3 and a current flowing through a fourth circuit of the coil 16_4 and the element 18_4.

Assume now that the oscillator frequency of the bias oscillating source 10 is 100 KHz, the coils 16_1 to 16_4 have inductances of 0.1 H, and the elements 18_1 to 18_4 have capacitances of 1000 pF. In this case, the elements 18_1 to 18_4 have each impedance of 1.6 KΩ at 100 KHz. In this case, the voltage dividing ratios in the first to the fourth circuits are approximately 40. When the output impedance of each of the recording amplifiers 20_1 to 20_4 is relatively small, the voltage dividing ratios become larger. When a proper bias current for each coil 16_1 to 16_4 is 0.3 mA/100 KHz, the bias voltage appearing at the first terminal of each coil 16_1 to 16_4 is approximately 20 V (63KΩ × 0.3 mA). The bias voltage is divided into 1/40, i.e. 0.5 V. In other words, bias leak voltage appearing at the output terminal of each recording amplifier 20_1 to 20_4 is 0.5 V or less. When the bias leak voltage is this small, no bias trap is needed in the output circuit of each recording amplifier 20_1 to 20_4. When the output impendance of each recording amplifier 20_1 to 20_4 at the bias oscillating frequency is considerably low, the output impedance may be considered to be the impedance elements 18_1 to 18_4.

The circuit construction shown in Figure 1 allows the bias trap to be omitted and reduces the undesired radiation of electromagnetic wave due to the presence of the higher harmonics component of the bias current. The following two reasons reduce the undesired radiation. The first is that terminals (*b* and *c*) of the coil 12_1 and 12_2 are grounded. The ground connection of the terminals shunts to ground most of the higher frequency component of the bias oscillating source 10 appearing at the secondary side due to the electrostatic coupling between the primary and the secondary coils of the oscillating transformer 12. The result is that the higher frequency leak arising from the electrostatic coupling of the transformer 12 is very small. When the coils 12_1 and 12_2 are of the bifilar winding type, the higher frequency leak is well balanced, and thus effectively reduced. The second is that the bias current ib1 flowing through the first bias supply path 14, is opposite in direction to the bias current ib2 flowing through the second bias supply path 14_2. The reason for this is that the bias voltage signals e_a and e_d are opposite in the phase. Because of the antiphase relation between them, the electromagnetic field developed from the first bias supply path 14_1 when the current ib1 flows therethrough is cancelled by that from the second bias supply path 14_2. Therefore, an intensity of the higher harmonics electromagnetic field of the bias current which is developed around the bias supply paths 14_1 and 14_2 becomes very small. The cancellation of the electromagnetic field is most effectively performed when bias supply paths 14_1 and 14_2 are closely disposed and ib1 = ib2. With respect to the balance between the bias currents, if the recording head 16 has the even number of channels, ib1 is substantially equal to ib2.

The cancellation of the electrostatic magnetic field is most pronounced when ib1 = ib2, as mentioned above. However, this does not imply that $e_a = e_d$. Even if ib1 = ib2, a variation of the impedances of the coils 16_1 to 16_4 causes the signals e_a and e_d to vary. In other words, the number of turns of the coil 12_1 is not necessarily coincident with that of the coil 12_2. The necessity for the cancellation of the electromagnetic fields is the relation of ib1 = ib2.

Although a four channel recording head is employed in the embodiment shown in Figure 1, any type of recording head may be used if it has an even number of channels. Further, if a dummy impendance is employed an odd-number of channels may be used. In Figure 1, when the head 16 has three-channels, the 4th channel coil 16_4 and the 4th impedance element 18_4 are substituted by the dummy impedance.

Figure 2 shows a circuit diagram of the details of the basic construction shown in Figure 1. The example of Figure 2 is a bias circuit applied to an ordinary 2-channel tape recorder. The output terminal of the first recording amplifier 20_1 is connected to ground through capacitors $C20_1$ and $C18_1$. Similarly, the output terminal of a second recording amplifier 20_2 is connected to ground through capacitors $C20_2$ and $C18_2$. The capacitors $C20_1$ and $C20_2$ used as DC block capacitors, may also be used to cut low frequency components of the signals e1 and e2. When the DC potentials at the output terminals of the recording amplifiers 20_1 and 20_2 are approximately zero, the capacitors $C20_1$ and $C20_2$ may be omitted. The capacitors $C18_1$ and $C18_2$ correspond to the first and second impedance elements 18_1 and 18_2, respectively.

The connection point between the capacitors $C20_1$ and $C18_1$ is connected to the second terminal of a first channel coil 16_1 of a recording head 16, through

a parallel circuit of a resistor $R24_1$ and a capacitor $C24_1$, which form a first compensation impedance circuit 24_1. The connection point between the capacitors $C20_2$ and $C18_2$ is connected to the second terminal of a second channel coil 16_2 of the recording head 16, through a parallel circuit of a resistor $R24_2$ and a capacitor $C24_2$, which form a second compensation impedance circuit 24_2. The first and the second compensation impedance circuits 24_1 and 24_2 are provided for compensating for the higher frequency components of the recording currents i1 and i2, respectively. The first terminal of the coil 16_1 is connected to the first phase terminal *a* of the secondary coil 12_1 of the oscillator transformer 12. The third phase terminals *d* of the secondary coil 12_2 of the oscillator transformer 12 is connected to the first terminal of the coil 16_2. The third phase terminal *d* is connected to the first phase terminal *a*, through a capacitor C12. The center tap between the secondary coils 12_1 and 12_2 of the transformer 12 is connected to ground. The capacitor C12, together with the secondary coils $12_1 + 12_2$, forms a resonance circuit or a tank circuit. The provision of the tank circuit reduces the distortion of higher harmonics of the bias voltage at the secondary coil and also increases a signal source impedance as viewed from the head 16 side.

The first terminal of the primary coil 12_0 of the oscillating transformer 12 is connected to the third terminal of the primary coil 12_0, through a capacitor $C10_1$, and to the collector of a PNP transistor Q10. The emitter of the transistor Q10 is connected to a positive power source +Vcc, through a resistor $R10_1$. The base of the transistor Q10 is connected to the third terminal of the primary coil 12_0, through a parallel circuit of a resistor $R10_2$ and a capcitor $C10_2$, and to the positive power source +Vcc, via a resistor $R10_3$. The positive power source +Vcc is connected to the second terminal of the primary coil 12_0, via a bypass capacitor $C10_3$. The second terminal of coil 12_0 is grounded by way of a resistor $R10_4$ and is the intermediate tap of the primary coil 12_0 but not necessarily the center tap of it. The bias oscillating source 10 thus constructed cooperates with the oscillator transformer 12 to form a bias oscillator *13* of a single type. The magnitude of the oscillating output from the oscillator *13* may be adjusted by changing the voltage of the positive power source +Vcc or the resistance of the resistor $R10_4$. Incidentally, the bias oscillator *13* may be the ordinary push-pull type. Additionally, the oscillator *13* may also be used as a power source for an erasing head (not shown), in addition to the bias supply. The antiphase current supply method like the case of the bias supplies by 14_1 and 14_2 shown in Figure 1 is preferable for the current supply for the erasing head. When the erasing head is of the single channel type, a dummy impedance should be used.

Figure 3 shows a modification of the circuit construction shown in Figure 2. In the modification, the first and second compensating impedance circuits 24_1 and 24_2 are provided at the oscillator transformer 12 side of coils 16_1 and 16_2. Since the impedance circuits 24_1 and 24_2, and the coils 16_1 and 16_2 constitute series circuits, the circuits of Figures 2 and 3 are equivalent with respect to these series circuits. In the Figure 3 circuit, LC series resonance circuits 18_1 and 18_2 are used for the impedance elements 18_1 and 18_2, respectively. The resonance frequencies of these resonance circuits are made to coincide with the oscillating frequency of the bias oscillator *13*. When such LC resonance circuits 18_1 and 18_2 are used, the resonance frequencies must be adjusted. Therefore, the advantage of eliminating the bias trap used in the conventional circuit disappears. However, the use of such resonance circuits may extremely reduce the bias leak appearing at the output circuit of the recording amplifier.

Unlike the conventional bias trap, the quality factor Q of each of the resonance circuits 18_1 and 18_2 may be low. In this case, even if the Q factor is small, the bias leak may effectively be reduced. Accordingly, if the Q factor is designed to be low, the frequency characteristic of the bias trap is broad. As a result, when variations of the resonance frequenies of the resonance circuits 18_1 and 18_2 and the oscillating frequency of the bias oscillator *13* are small, the adjustment of the resonance circuits 18_1 and 18_2 may be omitted.

Figure 4 shows a modification of the Figure 1 or 2 circuit which is an extension of these. The recording head 16 used in Figure 4 is of the two-channel type, but may be of two or more, i.e. multichannel type. The circuit construction of Figure 4 has some features which are not found in the circuits shown in Figures 1 to 3. In particular, in order to increase the bias supply impedance, a first impedance increase circuit 26 is provided between the secondary coils 12_1 and 12_2 of the oscillator transformer 12, and the channels 16_1 and 16_2 of the recording head 16. Further, a bias adjustment impedance circuit 28 to adjust the magnitude of the bias current is inserted between the secondary coil 12_1 and the circuit 26. In order to adjust the magnitude of the bias current flowing into the coils 16_1 and 16_2, first and second bias adjusting shunt circuits 30_1 and 30_2 are coupled with the coils 16_1 and 16_2 in parallel fashion, respectively. The center tap of the secondary coil of the oscillator transformer 12 is grounded via a second impedance increase circuit 32.

The first impedance increase circuit 26 increases the impedance of the bias signal source as viewed from the head 16 side, at the bias oscillating frequency. In other words, the bias current is fed to the head 16 in the constant current mode. This implies that the supply of a bias current with a constant amplitude is possible irrespective of a variation (usually + 30 %) of the impedance of each coil 16_1 and 16_2. The second impedance increase circuit 32 substantially floats the center tap of the secondary winding of the oscillator transformer 12 only at the bias frequency. That is, the circuit 32 has a very large impedance at the bias current frequency. Further, it implies that the center tap of the secondary winding is substantially grounded in the audio frequency band and at the higher harmonics frequency band of the bias oscillation. Furthermore, when a higher harmonics wave produced in the secondary coil of the oscillator transformer 12 is negligible, the impedance of the second impedance

increase circuit 32 may be large in the higher order harmonics region. In this case, the circuit 32 may be consist of by a mere inductance.

The components 24 to 32 shown in Figure 4 may be used individually or utilized in a suitable combination. Figure 4 construction will be explained in detail with referring to more practical circuit construction.

In Figure 5, a RC circuit of a two-stage stack construction is used for the first and the second compensation elements 24_1 and 24_2. A first RC parallel circuit having $C24_{1a}$ and $R24_{1a}$ or $C24_{2a}$ and $R24_{2a}$ is used for compensating for a first frequency characteristic; a second CR parallel circuit having $C24_{1b}$ and $R24_{1b}$ or $C24_{2b}$ and $R24_{2b}$ for compensating for a second frequency characteristic. When the compensating impedance circuit of a stack constructions is used in this way, a recording frequency characteristic may readily be flat. The stack construction permits complex equalisations to be performed and it is possible to vary the frequency spectrum of the playback sound in many different ways by appropriate selection of the values for the above components. The RC series circuits having $C30_1$ and $R30_1$, and $C30_2$ and $R30_2$ are used for the first and the second bias adjusting shunt circuits 30_1 and 30_2. In the circuit of Figure 5, the amplitude of the bias current fed to the coil 16_1 or 16_2 is adjusted by changing the resistor $R30_1$ or $R30_2$. The bias current adjustment may be performed by changing the capacitor $C30_1$ or $C30_2$.

Two inductors $L26_1$ and $L26_2$ are used for the first impedance increase circuit 26. The bias adjustment impedance circuit 28 and the second impedance increase circuit 32 are omitted. When the bias adjusting shunt circuits 30_1 and 30_2 are used, there is no need for the bias impedance circuit 28. When the impedance from the capacitor $C18_1$ to the first phase terminal *a* of the oscillating transformer 12 is equal to that from the capacitor $C18_2$ to the third phase terminal *d* of the oscillator transformer 12, a potential at the center tap of the secondary winding of the oscillator transformer 12 is approximately zero. Accordingly, if the center tap is grounded, little bias current flows from the center tap to ground. This will be easily understood from a bridge circuit in a balanced condition. Therefore, the second impedance increase circuit may be omitted in the circuit construction shown in Figure 5.

Turning now to Figure 6, there is shown another modification in which the first and the second compensation impedance circuits 24_1 and 24_2 shown in Figure 5 are removed and the first impedance increase circuit 26 is replaced by two LCR parallel resonance circuits. A first LCR circuit including $L26_1$, $C26_1$ and $R26_1$ and a second LCR circuit $L26_2$, $C26_2$ and $R26_2$ have each a maximum impedance at the bias current frequency. These LCR circuits are damped in the Q factor, so that an impedance change, when the frequency is treated as a parameter, is broad. For this, no adjustment is necessary for these LCR circuits.

In Figure 7, a parallel resonance circuit having L32 and C32 is used for the second impedance increase circuit 32. The resonance frequency of the resonance circuit having L32 and C32 is made to coincide with the bias current frequency. In this case, between the terminal *x* on the transformer 12 side of the resonance circuit of L32 and C32 and the terminal *y* on the ground circuit side there of, the impedance at the bias current frequency is substantially infinite. That is, the terminal *x* and the terminal *y* are separated at the bias current frequency. For the higher order harmonics component of the bias current frequency the terminal *x* is effectively connected to the terminal *y*, by way of the low impedance of the capacitor C32. For the audio frequency component much lower than the bias current frequency, the terminal *x* is effectively connected to the terminal *y*, through a low impedance of the inductor L32.

Figure 8 shows an equivalent circuit of the circuit construction shown in Figure 7. A low frequency signal source 20_1 corresponding to the recording amplifier 20_1 supplies a first recording current i1 which in turn flows into a loop including the first channel coil 16_1, the first bias signal source 12_1 and the second impedance increase circuit 32. A low frequency signal source 20_2 corresponding to the recording amplifier 20_2 supplies a second recording current i2 which in turn flows into a loop including the second channel coil 16_2, the second bias signal source 12_2 and the second impedance increase circuit 32. A bias current ib supplied from the first and the second bias signal sources 12_1 and 12_2 flows through a loop including the coil 16_1, the impedance elements 18_1 and 18_2 and the coil 16_2.

When the bias current ib flows through a single loop, the bias currents for the coil 16_1 and the coil 16_2 are essentially equal to each other. Accordingly, no bias adjustment is necessary individually for the coils 16_1 and 16_2. When the potential e_x at the terminal *x* and the potential e_y at the terminal *y* are equal to each other, a part of the bias current ib never flows into the circuit 32, even if the impedance of the circuit 32 is zero. Accordingly, if the relation $e_x = e_y$ substantially holds, the circuit 32 may be a single wire. However, because of a variation of the impedances of the coils 16_1 and 16_2, the relation $e_x = e_y$ hardly holds. In such a case, unless the circuit 32 has not a high impedance at the bias current frequency, the bias current flowing through the coil 16_1 is not always equal to the bias current flowing through the coil 16_2.

Turning now to Figure 9, there is shown a case where the bias adjusting impedance circuit 28 and the compencating impedance circuits 24_1 and 24_2 are added to the circuit construction shown in Figure 7. As seen from the explanation relating to Figure 8, so long as the second impedance increase circuit 32 is provided, the bias current flowing through the coil 16_1 is always equal to that flowing through the coil 16_2. Therefore, if the circuit 28 is inserted in series in any portion of the bias current loop having the components 12_1, 16_1, 24_1, 18_1, 18_2, 24_2, 16_2 and 12_2, the bias current adjustments of the two channels 16_1 and 16_2 may simultaneously be performed by a single circuit 28. In Figure 9, the circuit 28 is provided between the first phase terminal *a* of the secondary side of the oscillator transformer 12 and the first channel coil 16_1.

In Figure 9 for the circuit 28, a variable impedance circuit is used aiming at increasing the impedance of the bias signal source as viewed from the recording head 16 side. Specifically, an LCR parallel resonance circuit having L28, C28 and R28, like the LCR parallel resonance circuit having $L26_1$, $C26_1$ and $R26_1$ or L28, C28 and R28 shown in Figure 6, is used as the bias adjustment impedance circuit 28. The bias current ib can be adjusted by varying L28, C28 and/or R28 of those circuit components of the LCR circuit 28.

Figure 10 shows a modification of the circuit shown in Figure 4 in which the first impedance increase circuit 26 is comprised of choke coils $L26_1$ and $L26_2$ of the double winding type and the circuits 28 and 32 are substituted by a single wire. The choke coils $L26_1$ and $L26_2$ exhibit a high impedance for bias currents ib1 and ib2. The reason for this is that a magnetic flux developed by the coil $L26_1$ bearing the current ib1 and a magnetic flux by the coil $L26_2$ bearing the current ib2 are added to each other. In other words, the inductances of the coils $L26_1$ and $L26_2$ are increased by a mutual inductance between these coils. Therefore, the impedances of the coils $L26_1$ and $L26_2$ at the bias current frequency are higher than those of the Figure 5 construction.

On the other hand, the choke coils $L26_1$ and $L26_2$ exhibit a low impedance for the recording currents i1 and i2. This is because the magnetic flux developed by the coil $L26_1$ with the current i1 and the magnetic flux by the coil $L26_2$ with the current i2 cancel each other. In other words, the inductances $L26_1$ and $L26_2$ are reduced due to the mutual inductance between these coils. Further, since the currents i1 and i2 are signals in the audio frequency band, the impedances of the coils $L26_1$ and $L26_2$ for the currents i1 and i2 are sufficiently small. Thus, the choke coils $L26_1$ and $L26_2$ act to increase the bias signal source impedance with only sightly increasing the crosstalk between the recording currents. Incidentally, when the choke coils $L26_1$ and $L26_2$ contain slidable cores, that is to say, the choke coil is of the variable inductance type, the adjustments of the bias currents ib1 and ib2 may be performed in the circuit 26.

Figure 11 shows an embodiment in which the impedance circuits 24_1, 24_2 and 28 shown in the Figure 4 construction is removed and the first impedance increase circuit 26 is inserted between the recording head 16 and the impedance elements 18_1 and 18_2. The second terminal of the first channel coil 16_1 is grounded through an inductance $L26_1$ and a capacitor $C18_1$. The second terminal of the second channel coil 16_2d is grounded through an inductance $L26_2$ and capacitor $C18_2$. Note here that the inductance $L26_1$ and the capacitor $C18_1$ do not form a resonance circuit for the bias current frequency. The components $L26_1$ and $C18_1$ and the components $L26_2$ and $C18_2$ cooperate to form a low-pass filter (LPF) of 12dB/ oct for the currents ib1 and ib2 of which the cut-off frequency is lower than the bias current frequency. The inductances $L26_1$ and $L26_2$ also are used to increase the impedance of the bias current circuit, that is to say, to make current nearly constant. In Figure 11, the shield of a bias supply pass 14 for the first and second terminals of the head 16 also illustrated.

Although specific constructions have been illustrated and described herein, it is not intended that invention be limited to the elements, devices and/or circuit constructions disclosed. One skilled in the art will recognize that the particular elements, devices or sub-circuits may be used or combined without departing from the scope of the invention.

CLAIMS

1. A recording circuit comprising:

a multi-channel recording head of which each channel receives a recording signal and has a first and a second terminal;

impedance means for bypassing a bias current connected to a first terminal of the respective channel and an AC potential-zero circuit having substantially zero AC potential; the magnitude of the impedance of the impedance means at the bias current frequency being less than that at the recording signal frequency;

a bias oscillator, which constitutes an even number of bias signal sources for providing bias currents with the same frequencies to the respective channels of said recording head, including a first bias signal source which is connected via a first phase terminal to a second terminal of one channel of said recording head and which is connected via a second phase terminal, which is related in antiphase to the first phase terminal, to the AC potential-zero circuit, and including a second bias signal source which is connected via a third phase terminal to a second terminal of another channel of said recording head and which is connected via a fourth phase terminal, which is related in antiphase to the third phase terminal, to the AC potential-zero circuit; and

a first bias supply circuit extending from the first phase terminal, of the first bias signal source, to said one channel of said recording head and a second bias supply circuit extending from the third phase terminal; of the second bias signal source, to said other channel of said recording head, the first and second bias supply circuits being disposed closely in parallel in order to mitigate electromagnetic fields produced by higher harmonics components of said bias currents radiated from said first and second bias supply circuits.

2. A recording circuit according to claim 1, wherein the first and second bias signal sources are formed by the secondary coil of an oscillator transformer of the bias oscillator, the center tap of the secondary coil corresponding to the second phase terminal, of the first bias signal source, and the fourth phase terminal, of the second bias signal source.

3. A recording circuit according to claim 1, wherein the first and second bias signal sources are formed by the secondary coils bifilar wound of an oscillator transformer of said bias oscillator, and the winding end of the first secondary coil and the winding start of the second secondary coil correspond to the second phase terminal, of the first bias signal source, and the fourth phase terminal, of the second bias signal source, respectively.

4. A recording circuit according to any one of

In Figure 9 for the circuit 28, a variable impedance circuit is used aiming at increasing the impedance of the bias signal source as viewed from the recording head 16 side. Specifically, an LCR parallel resonance circuit having L28, C28 and R28, like the LCR parallel resonance circuit having $L26_1$, $C26_1$ and $R26_1$ or L28, C28 and R28 shown in Figure 6, is used as the bias adjustment impedance circuit 28. The bias current ib can be adjusted by varying L28, C28 and/or R28 of those circuit components of the LCR circuit 28.

Figure 10 shows a modification of the circuit shown in Figure 4 in which the first impedance increase circuit 26 is comprised of choke coils $L26_1$ and $L26_2$ of the double winding type and the circuits 28 and 32 are substituted by a single wire. The choke coils $L26_1$ and $L26_2$ exhibit a high impedance for bias currents ib1 and ib2. The reason for this is that a magnetic flux developed by the coil $L26_1$ bearing the current ib1 and a magnetic flux by the coil $L26_2$ bearing the current ib2 are added to each other. In other words, the inductances of the coils $L26_1$ and $L26_2$ are increased by a mutual inductance between these coils. Therefore, the impedances of the coils $L26_1$ and $L26_2$ at the bias current frequency are higher than those of the Figure 5 construction.

On the other hand, the choke coils $L26_1$ and $L26_2$ exhibit a low impedance for the recording currents i1 and i2. This is because the magnetic flux developed by the coil $L26_1$ with the current i1 and the magnetic flux by the coil $L26_2$ with the current i2 cancel each other. In other words, the inductances $L26_1$ and $L26_2$ are reduced due to the mutual inductance between these coils. Further, since the currents i1 and i2 are signals in the audio frequency band, the impedances of the coils $L26_1$ and $L26_2$ for the currents i1 and i2 are sufficiently small. Thus, the choke coils $L26_1$ and $L26_2$ act to increase the bias signal source impedance with only sightly increasing the crosstalk between the recording currents. Incidentally, when the choke coils $L26_1$ and $L26_2$ contain slidable cores, that is to say, the choke coil is of the variable inductance type, the adjustments of the bias currents ib1 and ib2 may be performed in the circuit 26.

Figure 11 shows an embodiment in which the impedance circuits 24_1, 24_2 and 28 shown in the Figure 4 construction is removed and the first impedance increase circuit 26 is inserted between the recording head 16 and the impedance elements 18_1 and 18_2. The second terminal of the first channel coil 16_1 is grounded through an inductance $L26_1$ and a capacitor $C18_1$. The second terminal of the second channel coil 16_2d is grounded through an inductance $L26_2$ and capacitor $C18_2$. Note here that the inductance $L26_1$ and the capacitor $C18_1$ do not form a resonance circuit for the bias current frequency. The components $L26_1$ and $C18_1$ and the components $L26_2$ and $C18_2$ cooperate to form a low-pass filter (LPF) of 12dB/ oct for the currents ib1 and ib2 of which the cut-off frequency is lower than the bias current frequency. The inductances $L26_1$ and $L26_2$ also are used to increase the impedance of the bias current circuit, that is to say, to make current nearly constant. In Figure 11, the shield of a bias supply pass 14 for the first and second terminals of the head 16 also illustrated.

Although specific constructions have been illustrated and described herein, it is not intended that invention be limited to the elements, devices and/or circuit constructions disclosed. One skilled in the art will recognize that the particular elements, devices or sub-circuits may be used or combined without departing from the scope of the invention.

CLAIMS

1. A recording circuit comprising:

a multi-channel recording head of which each channel receives a recording signal and has a first and a second terminal;

impedance means for bypassing a bias current connected to a first terminal of the respective channel and an AC potential-zero circuit having substantially zero AC potential; the magnitude of the impedance of the impedance means at the bias current frequency being less than that at the recording signal frequency;

a bias oscillator, which constitutes an even number of bias signal sources for providing bias currents with the same frequencies to the respective channels of said recording head, including a first bias signal source which is connected via a first phase terminal to a second terminal of one channel of said recording head and which is connected via a second phase terminal, which is related in antiphase to the first phase terminal, to the AC potential-zero circuit, and including a second bias signal source which is connected via a third phase terminal to a second terminal of another channel of said recording head and which is connected via a fourth phase terminal, which is related in antiphase to the third phase terminal, to the AC potential-zero circuit; and

a first bias supply circuit extending from the first phase terminal, of the first bias signal source, to said one channel of said recording head and a second bias supply circuit extending from the third phase terminal, of the second bias signal source, to said other channel of said recording head, the first and second bias supply circuits being disposed closely in parallel in order to mitigate electromagnetic fields produced by higher harmonics components of said bias currents radiated from said first and second bias supply circuits.

2. A recording circuit according to claim 1, wherein the first and second bias signal sources are formed by the secondary coil of an oscillator transformer of the bias oscillator, the center tap of the secondary coil corresponding to the second phase terminal, of the first bias signal source, and the fourth phase terminal, of the second bias signal source.

3. A recording circuit according to claim 1, wherein the first and second bias signal sources are formed by the secondary coils bifilar wound of an oscillator transformer of said bias oscillator, and the winding end of the first secondary coil and the winding start of the second secondary coil correspond to the second phase terminal, of the first bias signal source, and the fourth phase terminal, of the second bias signal source, respectively.

4. A recording circuit according to any one of

claims 1 to 3, wherein said impedance means are capacitors with much smaller impedances at the bias current frequency than the impedances of the respective channels of said recording head at the same frequency.

5. A recording circuit according to any one of claims 1 to 4, wherein said impedance means are series resonance circuits which each possesses a minimum impedance at the bias current frequency.

6. A recording circuit according to any one of claims 1 to 5, wherein compensating impedance circuits for compensating a recording frequency characteristic are connected in series with the respective channels of said recording head.

7. A recording circuit according to any one of claims 1 to 6, wherein the first bias supply circuit and the second bias supply circuit are connected in series with a first impedance increase circuit for making the bias current substantially constant.

8. A recording circuit according to any one of claims 1 to 3 and 6, wherein said impedance means are capacitors, one and another inductors are inserted between one channel of said recording head and one of the capacitors and between another channel of said recording head and another capacitor, said one inductor and one capacitor, and said another inductor and another capacitor form a low pass filter for the bias currents while said one and another inductors form a first impedance increase circuit for making the bias current substantially constant.

9. A recording circuit according to any one of claims 1 to 8, wherein a second impedance increase circuit exhibiting a high impedance at the bias current frequency is provided between the second phase terminal of the first bias signal source, and the fourth phase terminal of the second bias signal source and said AC potential-zero circuit, in order to reduce substantially to zero a bias current flowing between the second phase terminal of the first bias signal source, and the fourth phase terminal of the second bias signal source and said AC potential-zero circuit.

10. A recording circuit according to any one of claims 1 to 9, wherein a bias adjustment impedance circuit for adjusting magnitudes of the bias currents is provided in series with at least either of the first bias supply circuit or a second bias supply circuit.

11. A recording circuit according to claim 7 or 8, wherein bias adjusting shunt circuits are provided in parallel with the respective channels of said recording head in order to adjust the bias currents of the channels.

12. A recording circuit comprising:

a recording head with a plurality of channels each receiving a recording signal and having a first and a second terminal;

capacitors connected between the first terminal of the respective channels of said recording head and a circuit with substantially zero of AC potential in order to bypass bias current; the magnitude of the impedance of said capacitors at the bias current frequency being less than that at the recording signal frequency;

a bias oscillator for providing bias currents with the same frequencies to the respective channels of said recording head, which said bias oscillator includes a first bias signal source connected via a first phase terminal to the second terminal of one channel of said recording head and via a second phase terminal, which is related in antiphase to the first phase terminal, to the AC potential-zero circuit, and a second bias signal source connected via a third phase terminal to the second terminal of another channel of said recording head and via a fourth phase terminal, which is related in antiphase to the third phase terminal, to the AC potential-zero circuit;

a first bias supply path extending from the first phase terminal of said first bias signal source to said one channel of said recording head; and

a second bias supply path extending from the third phase terminal of said second bias signal source to said other channel of said recording head, which is disposed closely and in parallel with said first bias supply path in order to reduce an intensity of an electromagnetic field developed by higher harmonics component of the bias current radiated from a bias current supply path.

13. A recording circuit, substantially as hereinbefore described with reference to the accompanying drawings.

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