

ABSTRACT

Described is a MOS gate-controlled SCR (UGSCR) structure with a U-shaped gate (UMOS) for an ESD protection circuit in an IC device which is compatible with shallow trench isolation (STI) and self-aligned silicide (salicide) fabrication technology. The UMOS gate is located in a p-substrate and is surrounded by an n-well on either side. Adjacent to one side of the UMOS gate, a first n+ diffusion is formed which straddles the first n-well. The n+ diffusion together with a p+ pickup diffused next to it form the cathode of the SCR (thyristor). Adjacent to the other side of the UMOS gate, a second n+ and p+ diffusion are formed in a second n-well. The second n+ and p+ diffusion together with the UMOS gate form the anode of the SCR and the input terminal of the circuit to be protected. The SCR is formed by the first n+ diffusion/n-well (cathode), the p-substrate, the second n-well and the second p+/n+ diffusion (anode). A latchup immune circuit is achieved by creating a U-shaped gate structure which is lined with a thick gate oxide--similar to a field oxide--under the poly gate.

FIGURE 1