1. A semiconductor device comprising:

a stack structure comprising a plurality of conductive layer patterns and a plurality of interlayer insulating layer patterns that are alternately stacked on one another;

a channel hole penetrating the stack structure;

a dielectric layer disposed on a sidewall of the channel hole;

a channel layer disposed on the dielectric layer and in the channel hole;

a passivation layer disposed on the channel layer and in the channel hole, wherein the channel layer is interposed between the passivation layer and the dielectric layer;

an air gap surrounded by the passivation layer; and

a pad disposed in the channel hole and on the passivation layer;

wherein a width of the air gap is larger than a width of the passivation layer;

wherein the passivation layer comprises:

a lower layer disposed on the sidewall of the channel hole,

a horizontal layer disposed on the lower layer, and

a protrusion extending from the horizontal layer into the pad;

wherein the pad comprises a first pad and a second pad,

wherein the first pad is in contact with an upper surface of the horizontal layer, an upper surface of the dielectric layer, an upper surface of the channel layer and a side surface of the protrusion; and

wherein the second pad is in contact with an upper surface of the first pad and an upper surface of the protrusion.

2. The semiconductor device of claim 1, further comprising:

a bit line disposed on the pad.

3. The semiconductor device of claim 1,

wherein a width of the protrusion is smaller than a width of the horizontal layer.

4. The semiconductor device of any one of claims 1 to 3,

wherein the pad covers the horizontal layer, the protrusion, the dielectric layer and the channel layer in the channel hole.

5. The semiconductor device of claim 3 or claim 4,

wherein the first pad and the second pad comprise different materials.

6. The semiconductor device of any one of claims 1 to 5,

wherein a width of the protrusion is smaller than a width of the air gap.

7. A semiconductor device comprising:

a stack structure including a plurality of conductive layer patterns and a plurality of interlayer insulating layer patterns that are alternately and vertically stacked on one another;

an air gap disposed vertically in the stack structure;

a passivation layer covering an upper surface of the air gap;

a channel layer surrounding a side surface of the air gap;

a dielectric layer surrounding a side surface of the channel layer and in contact with the stack structure; and

a pad disposed on the passivation layer and in contact with an uppermost interlayer insulating layer pattern of the plurality of interlayer insulating layer patterns;

wherein the passivation layer comprises a horizontal layer that is in contact with the air gap and has a first width, and a protrusion that extends from the horizontal layer into the pad and has a second width smaller than the first width;

wherein the pad comprises a first pad and a second pad,

wherein the first pad is in contact with an upper surface of the horizontal layer and a side surface of the protrusion, and

wherein the second pad is in contact with an upper surface of the first pad and the upper surface of the protrusion.

8. The semiconductor device of claim 7,

wherein the passivation layer surrounds the side surface of the air gap, and

wherein the channel layer surrounds a side surface of the passivation layer.

9. The semiconductor device of claim 7 or claim 8,

wherein the uppermost interlayer insulating layer pattern of the plurality of interlayer insulating layer patterns is disposed at a top of the stack structure, and

wherein a height of the upper surface of the air gap is greater than a height of an upper surface of an uppermost conductive layer pattern of the plurality of conductive layer patterns in the stack structure.

10. The semiconductor device of any one of claims 7 to 9,

wherein the pad is in contact with the uppermost interlayer insulating layer pattern.

11. The semiconductor device of any one of claims 7 to 10, further comprising:

a bit line extending in a first direction on the pad,

wherein the plurality of conductive layer patterns extend in a second direction intersecting with the first direction.

12. A semiconductor device comprising:

a substrate;

a vertical channel comprising:

an air gap,

a channel layer surrounding a side surface of the air gap,

a dielectric layer surrounding a side surface of the channel layer,

a passivation layer covering an upper surface of the air gap, and

a pad disposed on the passivation layer;

a plurality of interlayer insulating layer patterns surrounding a side surface of the vertical channel and vertically spaced apart from one another; and

a plurality of conductive layer patterns surrounding the side surface of the vertical channel and each of the plurality of conductive layer patterns being disposed between two adjacent interlayer insulating layer patterns of the plurality of interlayer insulating layer patterns,

wherein the passivation layer comprises a horizontal layer that is in contact with the air gap and has a first width, and a protrusion that extends from the horizontal layer into the pad and has a second width smaller than the first width,

wherein a height of an upper surface of the protrusion is lower than an upper surface of the pad;

wherein the pad comprises a first pad and a second pad,

wherein the first pad is in contact with an upper surface of the horizontal layer and a side surface of the protrusion, and

wherein the second pad is in contact with an upper surface of the first pad and the upper surface of the protrusion.

13. The semiconductor device of claim 12,

wherein the dielectric layer comprises

a tunnel insulating layer surrounding the side surface of the channel layer,

a charge trap layer surrounding a side surface of the tunnel insulating layer, and

a blocking insulating layer surrounding a side surface of the charge trap layer.

14. The semiconductor device of claim 12 or 13,

wherein the passivation layer surrounds the side surface of the air gap.

15. The semiconductor device of any one of claims 12 to 14,

wherein the first pad and the second pad comprise different materials.

16. The semiconductor device of any one of claims 12 to 15,

wherein a width of the air gap is greater than a width of the protrusion.