

Description

(1) Field of the Invention

The present invention relates to a circuit for compensating the non-linearity of an input/output characteristic of a parallel comparison type analog-to-digital converter (hereinafter simply referred to as A/D converter).

(2) Background of the Art

In A/D converter, of the before mentioned type, the input/output characteristic is often damaged due to a current flow through each comparator from a resistor chain for generating and outputting each comparison voltage to be compared with an input analog voltage.

Before explaining the linearity of the input/output characteristic in the A/D converter, the construction of the A/D converter will briefly be described.

An N-bit A/D converter generally includes parallel-connected comparators (a comparator group) having a number of 2^N-1 , series-connected resistors (a chain of resistors) having a number of 2^N and equal resistance values for dividing a reference voltage (for example, -2V) into comparison reference voltages having a number of 2^N-1 and whose voltage values are mutually and sequentially different, each comparison voltage being supplied to the corresponding comparator and each comparator comparing the corresponding comparison voltage with an input analog voltage V_{IN} for determining any one of the comparison voltages which is nearest to the input voltage V_{IN} , and an encoder for encoding the comparison result to derive an N-bit digital signal as the output of the A/D converter.

In addition, a linearity compensation circuit is provided for compensating the linearity of the input/output characteristic of the A/D converter damaged due to the presence of a current flow to each comparator from the resistor chain for generating and outputting the comparison reference voltages. The resistor chain comprises series-connected resistors.

In details, since all reference voltage dividing resistors in the resistor chain have mutually the same resistance values, terminal voltages across the respective resistors are mutually equal and a potential at a connection point between each resistor and its adjacent resistor becomes reduced by the same voltage value as the voltage is changed from the reference voltage supply side to a zero voltage side. Therefore, a characteristic curve representing a relationship between each resistor connecting point and comparison voltage generated therefrom should have a perfect linearity.

However, since a constant current actually flows from the resistor chain to each comparator due to an

input characteristic of each comparator, the current flowing through each resistor does not become even and the linearity of the comparison voltages will, therefore, be damaged. This causes the worsened linearity of the above-described relationship input/output characteristic of the A/D converter and provides a source of errors in the output digital indication.

Consequently, it becomes necessary to compensate for the linearity by additionally supplying an auxiliary current to the connecting point corresponding to an amount of the current which has flowed into the comparator group. The linearity compensating circuit serves as such a compensation as described above.

As the number of output terminals of the linearity compensation circuit connected to the resistor chain becomes increased, the compensation described above becomes more perfect.

If the number of output terminals from the compensation circuit is 255 which is one less than the number of resistors in the resistor chain of an 8-bit A/D converter for generating 256 comparison reference voltages and an amount of current by which each connecting point flows into the corresponding comparator is replenished so as to compensate for the current flowing through each corresponding comparator, a most perfect linearity will be achieved.

However, in this case, the construction of the whole linearity compensation circuit becomes complex and the construction of the A/D converter becomes accordingly large-sized. In addition, a power consumption of the whole A/D converter becomes finally increased.

One of improved linearity compensation circuits applied to the A/D converter has already been announced in a general national convention of Electronic and Communication Society of 1983 fiscal year (preliminary manuscripts, page 467) in Japan.

In the announced linearity compensation circuit, a section which determines a current of an ECL (Emitter-Coupled Logic) circuitry used for the comparator group and encoder of the A/D converter is provided. In this section, a current flows into a main transistor thereof which is 384 as great as the current denoted by I flowing into an input circuit of one comparator in the comparator group as an input current (base current). A magnitude of this current $384I$ is divided by six to derive six current flows $64I$, $64I$, $64I$, $64I$, $64I$, and $64I$ by means of a current mirror circuit including four transistors. Then, three of the six currents ($64I$, $64I$, and $64I$ of the six-divided currents) are additionally supplied to three predetermined connecting points separated from one another by the number of the resistors of 64 in the resistor chain. It is noted that the currents which are 64 as great as the above-described input current of each comparator are obtained by six and only three of these six currents are used for the linearity compensation. The remaining three currents are caused to flow wastefully through

a minus terminal of the power supply of the linearity compensation circuit.

In this way, the previously announced linearity compensation circuit produces a current path through which a main current having a magnitude corresponding to a total current flow through all comparators in the A/D converter or corresponding to several times of the total current (in the above-described case, $384i = 1\frac{1}{2}$ times of the total current (256i)) flows. The main current is divided into a plurality of sub currents by means of the current mirror circuit. Some of the sub currents are supplied to appropriate connecting points respectively in the resistor chain of the A/D converter to compensate for the input currents flowing into the comparators.

However, the previously announced linearity compensation circuit has a drawback of increased current loss and consequent increased power consumption.

This is because the above-described main current (384i) flowing through the above-described main transistor of the above-described section is divided into six sub currents by means of the other three transistors constituting the current mirror circuit and three sub currents are supplied to the predetermined three connecting points of the resistor chain. Hence, if a current (emitter current of a transistor) flowing through an input bias circuit of each of the comparators in response to an input current of the comparator is I_E , a total of $384 I_E$ of current flows through the above-described transistors connected between the main transistor and minus terminal of the bias supply of the previously announced linearity compensation circuit. That is to say, to obtain three sub currents 64i having the magnitude 64 as great as the current i to be supplied to the input transistor of the comparator as the base current, the current 384 as great as the emitter current I_E of one transistor in the corresponding input comparator must wastefully be caused to flow.

This causes remarkable increases in current flows through the linearity compensation circuit and in power loss in the A/D converter.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an improved linearity compensation circuit for the A/D converter which can reduce a loss in current flow in the linearity compensation circuit and wasteful consumption of power in the A/D converter with accuracy and miniaturization of the A/D converter maintained.

The above-described object can be achieved by providing a circuit for compensating an input/output non-linearity of an analog-to-digital converter, comprising: (a) first means for providing a first current having a magnitude corresponding to a second current I_E which is an amplification of an input current i

flowing through an input circuit of one of a plurality of comparators in the analog-to-digital converter from a chain of resistors providing each of a plurality of comparison reference voltages for the corresponding one of the comparators; (b) second means for providing a third current kI_E on the basis of the first current, the third current being a multiplication of the second current by a first predetermined multiplication factor k; (c) third means for providing a fourth current k^2I_E on the basis of the third current, the fourth current being a multiplication of the third current by an inverse of an amplification factor of the input circuit of the comparator; and (d) fourth means for providing a fifth current k^3I_E on the basis of the fourth current, the current by a second predetermined multiplication factor and being supplied to the input circuit so as to compensate for a first input current flow totally supplied from a reference voltage supply of the resistor chain to a predetermined group of the input circuits of the comparators via the resistor chain.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a whole circuit configuration of an A/D converter to which the present invention is applicable.

Fig. 2 is a circuit construction of a linearity compensation circuit in a preferred embodiment according to the present invention which is applicable to the A/D converter shown in Fig. 1.

Fig. 3 is a circuit construction of an input circuit of one of comparators in a comparator group shown in Fig. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will hereinafter be made to the drawings in order to facilitate understanding of the present invention.

Fig. 1 shows an 8-bit A/D converter to which the present invention is applicable.

In Fig. 1, a resistor chain 1 includes 256 resistors R1 to R256 which are serially connected to a reference voltage supply, for example, 2 volts (a first resistor is connected to a zero terminal and 256th resistor is connected to a minus 2-volt terminal of the reference power supply). Each resistor connecting point in the resistor chain 1 provides a comparison reference voltage which has a different value from each of the other comparison reference voltages.

Each comparison reference voltage is inputted to a comparator group 2. The comparator group 2 includes 255 comparators COP1, COP2, ---. Each comparator COP1 to COP255 receives one corresponding comparison voltage and compares it with an input voltage (analog input signal) V_{IN} . An output signal of each comparator in the comparator group 2 is supplied to a coincidence detection circuit 3. The co-

Incidence detection circuit 3 detects whether any one of the comparison voltages with which the input voltage V_{IN} substantially coincides, i.e., to which one of the comparison reference voltages the input voltage V_{IN} is nearest. The coincidence circuit 3 includes gates G1, G2, --- for comparing the output signals between one comparator and adjacent comparator, each output signal being transmitted to an encoder 4. Each gate G1, G2, --- produces an output signal when the two input signal do not coincide with each other. When the input voltage V_{IN} is applied to the A/D converter, the output signal from any one of the gates G is produced. When the output signal from any one of the gates G is produced, the digital signal (8 bits) is produced as the output signal of the A/D converter.

A linearity compensation circuit 5 is installed for compensating the non-linearity of an input/output characteristic of the A/D converter damaged by currents i , i , --- flowing through the respective comparators COP from the resistor chain 1. The detailed construction and operation of the linearity compensation circuit 5 will be described later.

Fig. 2 shows a preferred embodiment of the linearity compensation circuit 5 shown in Fig. 1.

Fig. 3 shows an input circuit of one of the comparators COP in the comparator group 3 shown in Fig. 1.

In Fig. 2, a dummy bias circuit 6a is provided in the circuit 5 which has the same construction of a bias circuit 6 which determines a bias point at an input portion of each comparator COP shown in Fig. 3.

Next, in Fig. 3, an input circuit of the comparator COP includes an emitter follower transistor Q1 which receives one of 256 comparison reference voltages derived from the resistor chain 1 shown in Fig. 1 at its base.

An emitter potential of the transistor Q1 is compared with the analog input voltage V_{IN} by means of a comparison section denoted by COMP in Fig. 3 of the comparator COP. A transistor Q2 is connected to the emitter of the transistor Q1. The current flowing through the transistor Q2 is defined so as to have a predetermined value by means of the bias circuit 6. The bias circuit 6 includes transistors Q3 and Q4 and a resistor, as shown in Fig. 3. A predetermined current I_E flows through the transistor Q3. The transistor Q3 constitutes a current mirror circuit together with the above-described transistor Q2 and so on (constant current flow transistors of the comparison section COMP).

Hence, the current I_E having the same value as the current I_E which flows through the transistor Q3 in the bias circuit 6 flows into the transistor Q2. It is noted that a compensation transistor Q4 is incorporated into the bias circuit 6 for increasing a current amplification factor since emitter-grounded current amplification factors of the transistors Q2 and Q3 constituting the current mirror circuit are insufficient due to the presence of base currents flowing through

these transistors Q2 and Q3 are non-negligibly large with respect to values of collector currents thereof.

If a base-grounded current amplification factor of the transistor Q2 is α , the emitter current expressed as αI_E flows through the above-described transistor Q1 so that the current i expressed as $\alpha I_E / \beta$ flows into the transistor Q1 as its base current. It is noted that symbol β denotes an emitter-grounded current amplification factor of, e.g., the transistor Q1. As described above, the current i is determined which flows from the resistor chain 1 shown in Fig. 1 to one comparator COP by means of the bias circuit 6.

The linearity compensation circuit 5 shown in Fig. 2 is provided with the dummy bias circuit 6a formed to have the exactly same construction as the bias circuit 6 for deriving the above-described current I_E .

In the linearity compensation circuit 5, as shown in Fig. 2, a first current multiplier 7 is installed which provides a current multiplication factor k (eight in the preferred embodiment). The current multiplier 7 includes eight parallel transistors Q5₁ to Q5₈ constituting one current mirror circuit together with the emitter follower transistor Q3 of the dummy circuit 6a through which the current I_E of the above-described dummy bias circuit 6a flows as its emitter current, thus providing the total current flow expressed as $8I_E$ to the eight transistors Q5₁ to Q5₈. It is noted that each of the base-grounded current amplification factors α of the transistors Q5₁ to Q5₈ has the same value as that of the transistor Q2 and the current flowing through an interconnected collector of the current multiplier 7 is expressed as $8\alpha I_E$.

Transistors Q6₁ and Q6₂ constitute emitter follower transistors with the current multiplier 7 being functioned as a load, thus functioning to provide the current of $8i$ at the bases of the transistors Q6₁ and Q6₂. Each of the emitter-grounded current amplification factors of the transistors Q6₁ and Q6₂ has the same value as that of the input transistor Q1 of the comparator COP shown in Fig. 3 and, hence, the total sum of the base currents of the transistors Q6₁ and Q6₂ is expressed as $8\alpha I_E / \beta$. This corresponds to the current expressed as $8i$ ($8i = 8\alpha I_E / \beta$).

In addition, a transistor Q7 is a transistor for supplying the base current to the transistors Q6₁ and Q6₂ and the current of $8i$ flows through the transistor Q7 as its collector current.

A second current multiplier 8 is installed in the linearity compensation circuit 5 shown in Fig. 2 which has the current multiplication factor ℓ (8 in the preferred embodiment) for providing the current having the magnitude of $64i$ from the current of $8i$. The second current multiplier 8 includes eight transistors Q8₁ to Q8₈, a total sum of the collector currents of the eight transistors Q8₁ to Q8₈ expressed as $64i$ being supplied to, e.g., predetermined one of the connecting points between the resistors R64 and R65 in the resistor chain 1 denoted by Ndi shown in Fig. 1.

Furthermore, a transistor Q9 is installed in the linearity compensation circuit 5 which functions as the transistor Q4 in the dummy bias circuit 6a and bias circuit 6. The base current of the transistor Q9 is negligible as compared with the base current of 8i in each of the transistors Q6₁ and Q6₂.

It is noted that in the 8-bit A/D converter shown in Fig. 1 the three linearity compensation circuits 5 having the same constructions as shown in Fig. 2 are provided and the other two circuits are connected to the other two connecting points Nd2 and Nd3 for auxiliarily supplying the current flows to the corresponding comparators COPs.

As described above, the linearity compensation circuit 5 shown in Fig. 2 provides the same current as the emitter current $I_E (= \beta i / \alpha)$ flowing through the transistor Q2 of the input circuit of the comparator COP through the dummy bias circuit 6a formed so as to have the same construction as the bias circuit 6 of the input circuit in the one comparator COP. The current I_E produced by the circuit 6a is multiplied by 8 by means of the first current multiplier 7 to provide the current of $8I_E$. After conversion of the current $8I_E$ into the base current of 8i ($8\alpha I_E / \beta$) by means of the transistors Q6₁ and Q6₂, the base current 8i is multiplied by 8 to provide the current 64i (64 times of the input current i) by means of a second current multiplier 8 constituted by the transistors Q8₁ to Q8₈ of the current mirror circuit together with the transistor Q7.

Therefore, according to the linearity compensation circuit described above, the current which must flow wastefully into the transistors Q5₁ to Q5₈ and Q3 of the dummy bias circuit 6a to obtain the same compensation current 64i amounts only to $9I_E$. Consequently, the value of the current ($9I_E + 9I_E + 9I_E = 27I_E$) is remarkably smaller than the current ($84I_E$) in the previously proposed linearity compensation circuit described in the Background of the Art.

In details, in the previously announced linearity compensation circuit, the totally $384I_E$ current must be caused to flow into the transistors connected to the main transistor to obtain the three of the sub currents (64×3). In addition, the current needed to provide the current of 64i amounts to $128I_E$. On the other hand, the linearity compensation circuit shown in Fig. 2 amounts to only $9I_E$ and, therefore, the wastefully consumed current can be reduced by about 1/15. It is noted that each emitter current of the transistor Q3 shown in Figs. 2 and 3 needs not to make exactly equal to the emitter current I_E of the transistor Q2. The dummy bias circuit 6a needs to have the same construction as the bias circuit 6. Then, the emitter load resistance of the transistor Q2 has the same value as that of each resistor of the emitter loads of the transistors Q5₁ to Q5₈. At this time, the emitter current of the transistor Q3 has the substantially same effect even if a value of the emitter current of the transistor Q3 is slightly less than the current I_E .

In addition, if the current amplification factor k of the first current multiplier 7 is varied, the wastefully consumed amount of current in the linearity compensation circuit can remarkably be reduced. For example, if the current multiplication factor k is 4, the current flowing through the current multiplication circuit 7 amounts to only $4I_E$ and the total wastefully consumed current amounts only to $5I_E$ with the current I_E flowing through the dummy bias circuit 6a added.

However, in this case, it is necessary to change the current multiplication factor ℓ of the second current multiplier 8 from 8 to 16. At this time, the number of the parallel transistors used in the second multiplier 8 are slightly increased from 8 to 16.

Hence, preferably, with the degree of two demands to miniaturize the A/D converter to reduce current consumption taken into account, the current multiplication factors k and ℓ of the two multipliers 7 and 8 need to be determined.

As an alternative, number of the current multipliers 8 in the linearity compensation circuit 5 in the preferred embodiment may be three and the current of 64i may be outputted from each of the three current multipliers 8, 8, and 8. In doing so, the dummy bias circuit 6a, current multiplier 7, and transistors Q6₁, Q6₂, and Q7 can be commonized with the three current multipliers 8, 8, and 8 so that the total wastefully consumed current amounts only to $9I_E$ to obtain the sub currents of $3 \times 64i$.

As described hereinabove, in the linearity compensation circuit for the A/D converter according to the present invention, the current $k\ell i$ for the linearity compensation having the magnitude of the input current i of each comparator multiplied by $k\ell$ by means of the plurality of current multipliers can be achieved and the current wastefully consumed for obtaining the current $k\ell i$ can amount only approximately to the current kI_E consumed by means of the first current multiplier. Hence, the current required to achieve the same compensation current for the linearity of the input/output characteristic of the A/D converter can remarkably be reduced. In addition, the A/D converter can be small-sized and the power consumption thereof can accordingly be reduced with high accuracy maintained.

Claims

1. A circuit for compensating an input/output non-linearity of an analog-to-digital converter, comprising:

(a) first means (6a) for providing a first current having a magnitude corresponding to a second current I_E which is an amplification of an input current i flowing through an input circuit of one of a plurality of comparators (2) in the analog-to-digital converter from a chain of re-



Furthermore, a transistor Q9 is installed in the linearity compensation circuit 5 which functions as the transistor Q4 in the dummy bias circuit 6a and bias circuit 6. The base current of the transistor Q9 is negligible as compared with the base current of 8i in each of the transistors Q6₁ and Q6₂.

It is noted that in the 8-bit A/D converter shown in Fig. 1 the three linearity compensation circuits 5 having the same constructions as shown in Fig. 2 are provided and the other two circuits are connected to the other two connecting points Nd2 and Nd3 for aux-
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As described above, the linearity compensation circuit 5 shown in Fig. 2 provides the same current as the emitter current $I_E (= \beta i / \alpha)$ flowing through the transistor Q2 of the input circuit of the comparator COP through the dummy bias circuit 6a formed so as to have the same construction as the bias circuit 6 of the input circuit in the one comparator COP. The current I_E produced by the circuit 6a is multiplied by 8 by means of the first current multiplier 7 to provide the current of $8I_E$. After conversion of the current $8I_E$ into the base current of 8i ($8\alpha I_E / \beta$) by means of the transistors Q6₁ and Q6₂, the base current 8i is multiplied by 8 to provide the current 64i (64 times of the input current i) by means of a second current multiplier 8 constituted by the transistors Q8₁ to Q8₈ of the current mirror circuit together with the transistor Q7.

Therefore, according to the linearity compensation circuit described above, the current which must flow wastefully into the transistors Q5₁ to Q5₈ and Q3 of the dummy bias circuit 6a to obtain the same compensation current 64i amounts only to $9I_E$. Consequently, the value of the current ($9I_E + 9I_E + 9I_E = 27I_E$) is remarkably smaller than the current ($84I_E$) in the previously proposed linearity compensation circuit described in the Background of the Art.

In details, in the previously announced linearity compensation circuit, the totally $384I_E$ current must be caused to flow into the transistors connected to the main transistor to obtain the three of the sub currents (64×3). In addition, the current needed to provide the current of 64i amounts to $128I_E$. On the other hand, the linearity compensation circuit shown in Fig. 2 amounts to only $9I_E$ and, therefore, the wastefully consumed current can be reduced by about 1/15. It is noted that each emitter current of the transistor Q3 shown in Figs. 2 and 3 needs not to make exactly equal to the emitter current I_E of the transistor Q2. The dummy bias circuit 6a needs to have the same construction as the bias circuit 6. Then, the emitter load resistance of the transistor Q2 has the same value as that of each resistor of the emitter loads of the transistors Q5₁ to Q5₈. At this time, the emitter current of the transistor Q3 has the substantially same effect even if a value of the emitter current of the transistor Q3 is slightly less than the current I_E .

In addition, if the current amplification factor k of the first current multiplier 7 is varied, the wastefully consumed amount of current in the linearity compensation circuit can remarkably be reduced. For example, if the current multiplication factor k is 4, the current flowing through the current multiplication circuit 7 amounts to only $4I_E$ and the total wastefully consumed current amounts only to $5I_E$ with the current I_E flowing through the dummy bias circuit 6a added.

However, in this case, it is necessary to change the current multiplication factor ℓ of the second current multiplier 8 from 8 to 16. At this time, the number of the parallel transistors used in the second multiplier 8 are slightly increased from 8 to 16.

Hence, preferably, with the degree of two demands to miniaturize the A/D converter to reduce current consumption taken into account, the current multiplication factors k and ℓ of the two multipliers 7 and 8 need to be determined.

As an alternative, number of the current multipliers 8 in the linearity compensation circuit 5 in the preferred embodiment may be three and the current of 64i may be outputted from each of the three current multipliers 8, 8, and 8. In doing so, the dummy bias circuit 6a, current multiplier 7, and transistors Q6₁, Q6₂, and Q7 can be commonized with the three current multipliers 8, 8, and 8 so that the total wastefully consumed current amounts only to $9I_E$ to obtain the sub currents of $3 \times 64i$.

As described hereinabove, in the linearity compensation circuit for the A/D converter according to the present invention, the current $k\ell i$ for the linearity compensation having the magnitude of the input current i of each comparator multiplied by $k\ell$ by means of the plurality of current multipliers can be achieved and the current wastefully consumed for obtaining the current $k\ell i$ can amount only approximately to the current kI_E consumed by means of the first current multiplier. Hence, the current required to achieve the same compensation current for the linearity of the input/output characteristic of the A/D converter can remarkably be reduced. In addition, the A/D converter can be small-sized and the power consumption thereof can accordingly be reduced with high accuracy maintained.

Claims

1. A circuit for compensating an input/output non-linearity of an analog-to-digital converter, comprising:

(a) first means (6a) for providing a first current having a magnitude corresponding to a second current I_E which is an amplification of an input current i flowing through an input circuit of one of a plurality of comparators (2) in the analog-to-digital converter from a chain of re-



sistors (1) providing each of a plurality of comparison reference voltages for the corresponding one of the comparators;

(b) second means (7) for providing a third current $k \cdot I_E$ on the basis of the first current, the third current being a multiplication of the second current by a first predetermined multiplication factor k ;

(c) third means ($Q6_1$, $Q6_2$) for providing a fourth current $k \cdot I$ on the basis of the third current, the fourth current being a multiplication of the third current by an inverse of an amplification factor of the input circuit of the comparator; and

(d) fourth means (8) for providing a fifth current $k \cdot I \cdot i$ on the basis of the fourth current, the fifth current being a multiplication of the fourth current by a second predetermined multiplication factor i and being supplied to the input circuit so as to compensate for a first input current flow totally supplied from a reference voltage supply of the resistor chain (1) to a predetermined group of the input circuits of the comparators via the resistor chain.

2. A circuit as set forth in claim 1, wherein the first mean (6a) supplies the fifth current to the input circuit of one of the other comparators so as to compensate for a second input current flow totally supplied from the reference voltage supply to a second predetermined group of the input circuits of the comparators subsequent to the predetermined group via the resistor chain (1) and to the input circuit of another one of the other comparators so as to compensate for a third input current flow totally supplied from the reference voltage supply to a third group of input circuits of the comparators via the resistor chain (1) subsequent to the second group.
3. A circuit as set forth in claim 1, wherein the first means (6a) comprises a plurality of first circuits, each first circuit being a dummy bias circuit having the same construction as a bias circuit of each comparator and providing the first current having the magnitude equal to the second current.
4. A circuit as set forth in claim 3, wherein the second means (7) comprises a plurality of first current multipliers each of which multiplies the second current by the first multiplication factor.
5. A circuit as set forth in claim 4, wherein the first multiplication factor is a positive integer.
6. A circuit as set forth in claim 4, wherein the fourth means (8) comprises a plurality of second current multipliers each of which multiplies the fourth cur-

rent by the second multiplication factor.

7. A circuit as set forth in claim 6, wherein the second multiplication factor is a positive integer.
8. A circuit as set forth in claim 4, wherein the first predetermined multiplication factor has a different value from the second predetermined multiplication factor.
9. A circuit as set forth in claim 4, wherein the first predetermined factor has the same value as the second predetermined factor.
10. A circuit as set forth in claim 4, wherein each of the first current multipliers constitutes a first current mirror circuit together with a predetermined emitter follower transistor ($Q3$) of the corresponding first circuit.
11. A circuit as set forth in claim 6, wherein the fourth means (8) further includes a plurality of first emitter follower transistors and wherein each of the second current multipliers constitutes a second mirror circuit together with the corresponding one of the emitter follower transistors.
12. A circuit as set forth in claim 6, wherein the third means comprises a plurality of a set of first transistors each set of the first transistors connected between the corresponding first and second circuits and having an emitter grounded current amplification factor equal to that of an input transistor of the input circuit of the comparator.
13. A circuit as set forth in claim 12, wherein the numbers of the first circuits, first current multipliers, second current multipliers, the set of the first transistors are the mutually the same and are determined on the basis of the number of bits of an output digital signal of the analog-to-digital converter.
14. A circuit as set forth in claim 6, wherein each of the second mirror circuits comprises a plurality of parallel emitter follower transistors whose collectors are interconnected to provide the fifth current and whose bases are interconnected to another transistor for compensating an emitter-grounded current amplification factor of the first and second emitter follower transistors of the corresponding second current mirror circuit.
15. A circuitry as set forth in claim 1 for compensating an input/output non-linearity of an 8-bit analog-to-digital converter,
 - (a) wherein said first means (6a) comprises three first circuits, each first circuit providing



- a first current having a magnitude corresponding to a second current I_E which is an amplification of an input current I flowing through an input circuit of one of a plurality of comparators in the 8-bit analog-to-digital converter from a resistor chain providing each of a plurality of mutually different levels of comparison reference voltages for the corresponding one of the comparators;
- (b) wherein said second means (7) comprises three second circuits, each second circuit providing a third current kI_E on the basis of the first current, the third current kI_E being a multiplication of the second current I_E by a first factor of a positive integer k ;
- (c) wherein said third means ($Q6_1, Q6_2$) comprises three third circuits, each third circuit providing a fourth current kI on the basis of the third current kI_E , the fourth current being a multiplication of the third current kI_E by an inverse of an emitter-grounded current amplification factor β of the input circuit; and
- (d) wherein said fourth means (8) comprises three fourth circuits, each fourth circuit providing a fifth current k^2I on the basis of the fourth current, the fifth current being a multiplication of the fourth current kI by a second factor of a positive integer l and being supplied to a predetermined one of the comparators.
16. A circuitry as set forth in claim 15, wherein the first factor is 8 and the second factor is 8.
 17. A circuitry as set forth in claim 16, wherein one of the three fifth currents $64I$ is supplied to the 64th comparator, one of the other two fifth currents $64I$ is supplied to the 128th comparator, and the remaining fifth current $64I$ is supplied to the 192th comparator.
 18. A circuitry as set forth in claim 15, wherein each of the first circuits has the same construction of a bias circuit of each comparator and includes a first emitter follower transistor and a resistor connected between the first transistor and a minus terminal of a power supply of the circuitry.
 19. A circuitry as set forth in claim 18, wherein each of the second circuits comprises a first current multiplier having the first factor of multiplication and connected to the first transistor of the corresponding one of the first circuits.
 20. A circuitry as set forth in claim 19, wherein the first current multiplier comprises a first current mirror circuit together with the first transistor of the first circuit, the first current mirror circuit having a plurality of parallel-connected second transistors whose bases are interconnected to the base of the first transistor and through each emitter of which the current equal to the first current I_E flows via a resistor.
 21. A circuitry as set forth in claim 20, wherein each of the third circuits comprises two third transistors whose bases, emitter, and collectors are mutually connected and whose emitters are connected to the collectors of the second transistors of the first current mirror circuit so that the current expressed as $\alpha k I_E$ (α denotes a base-grounded current amplification factor) flows into the bases of the third transistors.
 22. A circuitry as set forth in claim 21, wherein each of the fourth circuits comprises a second current multiplier having the second factor of multiplication and connected to the base of the third transistors via an emitter of a fourth transistor.
 23. A circuitry as set forth in claim 22, wherein the second current multiplier comprises a plurality of parallel-connected fifth transistors whose bases are mutually connected and connected to the emitter of the fourth transistor, whose emitters are respectively connected to a zero terminal of the power supply via resistors, and whose collectors are interconnected to supply the fifth current to the predetermined one of the comparators, the plurality of parallel-connected fifth transistors constituting a second current mirror circuit together with a sixth transistor whose emitter is connected to the zero terminal of the power supply via a resistor, whose base is connected to the base of each fifth transistor, and whose collector is connected to the base of the fourth transistor.
 24. A circuitry as set forth in claim 20, wherein a value of the resistor connected between the emitter of the first transistor and minus terminal of the power supply has the same value as each of the resistors connected between the emitter of each corresponding second transistor and the minus terminal.
 25. A circuitry as set forth in claim 22, wherein the first current multiplier has the first multiplication factor of 8 and the second current multiplier has the second multiplication factor of 8.
 26. A circuitry as set forth in claim 22, wherein the first current multiplier has the first multiplication factor of 4 and the second current multiplier has the second multiplication factor of 16.
 27. A circuitry as set forth in claim 23, wherein the



numbers of the second and fifth transistors are varied according to the first multiplication factor.

Patentansprüche

1. Schaltung zur Kompensierung der Nichtlinearität der Eingangs-/Ausgangscharakteristik eines Analog-Digital-Wandlers, mit

(a) einer ersten Einrichtung (6a) zum Erzeugen eines ersten Stroms mit einer Stärke, die dem eines zweiten Stroms I_E entspricht, der das Ergebnis der Verstärkung eines Eingangsstroms (I) ist, der durch eine Eingangsschaltung eines von mehreren Komparatoren (2) im Analog-Digital-Wandler ausgehend von einer Kette von Widerständen (1) fließt, von denen jeder jeweils eine von mehreren Vergleichsbezugsspannungen für den zugehörigen Komparator erzeugt;

(b) einer zweiten Einrichtung (7) zum Erzeugen eines dritten Stroms $k \cdot I_E$ auf Grundlage des ersten Stroms, wobei der dritte Strom das Ergebnis einer Multiplikation des zweiten Stroms mit einem ersten vorgegebenen Multiplikationsfaktor k ist;

(c) einer dritten Einrichtung (Q_{b1} , Q_{b2}) zum Erzeugen eines vierten Stroms $k \cdot I$ auf Grundlage des dritten Stroms, wobei der vierte Strom das Ergebnis einer Multiplikation des dritten Stroms mit dem Inversen des Verstärkungsfaktors der Eingangsschaltung des Komparators ist; und

(d) einer vierten Einrichtung (8) zum Erzeugen eines fünften Stroms $k \cdot I \cdot I$ auf Grundlage des vierten Stroms, wobei der fünfte Strom das Ergebnis einer Multiplikation des vierten Stroms mit einem zweiten vorgegebenen Multiplikationsfaktor l ist, und dieser der Eingangsschaltung zugeführt wird, um einen ersten Eingangsstromfluß zu kompensieren, der insgesamt von einer Bezugsspannungsquelle für die Widerstandskette (1) an eine vorgegebene Gruppe von Eingangsschaltungen der Komparatoren über die Widerstandskette geliefert wird.

2. Schaltung nach Anspruch 1, bei der die erste Einrichtung (6a) den fünften Strom an die Eingangsschaltung einer der anderen Komparatoren liefert, um einen zweiten Eingangsstromfluß zu kompensieren, der vollständig von der Bezugsspannungsquelle an eine zweite vorgegebene Gruppe von Eingangsschaltungen der Komparatoren, anschließend an die vorgegebene Gruppe, über die Widerstandskette (1) geliefert wird, und an die Eingangsschaltung eines anderen der Komparatoren liefert, um einen dritten Eingangs-

strom zu kompensieren, der vollständig von der Bezugsspannungsquelle an eine dritte Gruppe von Eingangsschaltungen der Komparatoren, anschließend an die zweite Gruppe, über die Widerstandskette (1) geliefert wird.

3. Schaltung nach Anspruch 1, bei der die erste Einrichtung (6a) mehrere erste Schaltungen aufweist, wobei jede erste Schaltung eine Blindversorgungsschaltung ist, die denselben Aufbau wie eine Vorversorgungsschaltung jedes Komparators aufweist und den ersten Strom liefert, der eine dem zweiten Strom gleiche Stärke aufweist.

4. Schaltung nach Anspruch 3, bei der die zweite Einrichtung (7) mehrere erste Strommultiplizierer aufweist, von denen jeder den zweiten Strom mit dem ersten Multiplikationsfaktor multipliziert.

5. Schaltung nach Anspruch 4, bei der der erste Multiplikationsfaktor eine positive, ganze Zahl ist.

6. Schaltung nach Anspruch 4, bei der die vierte Einrichtung (8) mehrere zweite Strommultiplizierer aufweist, von denen jeder den vierten Strom mit dem zweiten Multiplikationsfaktor multipliziert.

7. Schaltung nach Anspruch 6, bei der der zweite Multiplikationsfaktor eine positive, ganze Zahl ist.

8. Schaltung nach Anspruch 4, bei der der erste vorgegebene Multiplikationsfaktor einen anderen Wert als der zweite vorgegebene Multiplikationsfaktor aufweist.

9. Schaltung nach Anspruch 4, bei der der erste vorgegebene Faktor denselben Wert wie der zweite vorgegebene Faktor aufweist.

10. Schaltung nach Anspruch 4, bei der jeder der ersten Strommultiplizierer zusammen mit einem vorgegebenen Emitterfolgertransistor (Q_3) der entsprechenden ersten Schaltung eine erste Stromspiegelschaltung bildet.

11. Schaltung nach Anspruch 6, bei der die vierte Einrichtung (8) ferner mehrere erste Emitterfolgertransistoren beinhaltet, und bei der jeder der zweiten Strommultiplizierer zusammen mit dem zugehörigen der Emitterfolgertransistoren eine zweite Stromspiegelschaltung bildet.

12. Schaltung nach Anspruch 6, bei der die dritte Einrichtung mehrere Sätze erster Transistoren aufweist, wobei jeder Satz erster Transistoren zwischen die entsprechenden ersten und zweiten



Schaltungen geschaltet ist und einen emitterbezogenen Stromverstärkungsfaktor aufweist, der demjenigen eines Eingangstransistors der Eingangsschaltung eines Komparators entspricht.

13. Schaltung nach Anspruch 12, bei denen die Anzahlen der ersten Schaltungen, ersten Strommultiplizierer, zweiten Strommultiplizierer und Sätze erster Transistoren jeweils dieselben sind und auf Grundlage der Anzahl von Bits des digitalen Ausgangssignals des Analog-Digital-Wandlers festgelegt sind.

14. Schaltung nach Anspruch 6, bei der jede der zweiten Stromspiegelschaltungen mehrere parallele Emitterfolgertransistoren beinhaltet, deren Kollektoren miteinander verbunden sind, um den fünften Strom zu erzeugen, und deren Basisanschlüsse mit einem anderen Transistor verbunden sind, um einen emitterbezogenen Stromverstärkungsfaktor des ersten und zweiten Emitterfolgertransistors der zugehörigen zweiten Stromspiegelschaltung zu kompensieren.

15. Schaltung nach Anspruch 1 zur Kompensierung der Nichtlinearität der Eingangs-/Ausgangscharakteristik eines 8-Bit-Analog-Digital-Wandlers,

(a) in der die erste Einrichtung (6a) drei erste Schaltungen beinhaltet, wobei jede erste Schaltung einen ersten Strom mit einer Stärke liefert, die einem zweiten Strom I_E entspricht, der das Ergebnis einer Verstärkung eines Eingangstroms I ist, der durch eine Eingangsschaltung einer von mehreren Kompensatoren im 8-Bit-Analog-Digital-Umsetzer ausgehend von einer Widerstandskette fließt, die jeden von mehreren voneinander verschiedenen Pegeln von Vergleichsbezugsspannungen für den zugehörigen Komparator erzeugt;

(b) in der die zweite Einrichtung (7) drei zweite Schaltungen umfaßt, wobei jede zweite Schaltung einen dritten Strom kI_E auf Grundlage des ersten Stroms liefert, der das Ergebnis einer Multiplikation des zweiten Stroms I_E mit einem ersten Faktor entsprechend einer positiven, ganzen Zahl k ist;

(c) in der die dritte Einrichtung (Qb_1, Qb_2) drei dritte Schaltungen umfaßt, wobei jede dritte Schaltung einen vierten Strom kI auf Grundlage des dritten Stroms kI_E erzeugt, wobei der vierte Strom das Ergebnis einer Multiplikation des dritten Stroms kI_E mit dem Inversen des emitterbezogenen Stromverstärkungsfaktors β der Eingangsschaltung ist; und

(d) in der die vierte Einrichtung (8) drei vierte Schaltungen umfaßt, wobei jede vierte Schaltung einen fünften Strom kI auf Grundlage

des vierten Stroms erzeugt, wobei der fünfte Strom das Ergebnis einer Multiplikation des vierten Stroms kI mit einem zweiten Faktor entsprechend einer positiven, ganzen Zahl ℓ ist, und er einem vorgegebenen der Komparatoren zugeführt wird.

16. Schaltung nach Anspruch 15, bei der der erste Faktor 8 ist und der zweite Faktor 8 ist.

17. Schaltung nach Anspruch 16, bei der eine der drei fünften Ströme $64I$ dem 64-ten Komparator zugeführt wird, einer der anderen zwei fünften Ströme $64I$ dem 128-ten Komparator zugeführt wird und der restliche fünfte Strom $64I$ dem 192-ten Komparator zugeführt wird.

18. Schaltung nach Anspruch 15, bei der jede der ersten Schaltungen denselben Aufbau wie eine Vorversorgungsschaltung für jeden Komparator aufweist und sie einen ersten Emitterfolgertransistor und einen zwischen den ersten Transistor und den Minusanschluß einer Spannungsversorgung der Schaltung geschalteten Widerstand beinhaltet.

19. Schaltung nach Anspruch 18, bei der jede der zweiten Schaltungen einen ersten Stromverstärker mit dem ersten Multiplikationsfaktor aufweist, der mit dem ersten Transistor der zugehörigen der ersten Schaltungen verbunden ist.

20. Schaltung nach Anspruch 19, bei der der erste Stromverstärker eine erste Stromspiegelschaltung bildet, zusammen mit dem ersten Transistor der ersten Schaltung, wobei die erste Stromspiegelschaltung mehrere parallelverbundene zweite Transistoren enthält, deren Basisanschlüsse mit der Basis des ersten Transistors verbunden sind, wobei durch jeden Emitter derselben ein Strom über einen Widerstand fließt, der dem ersten Strom I_E entspricht.

21. Schaltung nach Anspruch 20, bei der jede der dritten Schaltungen zwei dritte Transistoren aufweist, deren Basis-, Emitter- und Kollektorsanschlüsse miteinander verbunden sind und deren Emitter mit den Kollektoren der zweiten Transistoren der ersten Stromspiegelschaltung verbunden sind, so daß ein als αkI_E (α bezeichnet den basisbezogenen Stromverstärkungsfaktor) ausgeprägten Strom durch die Basisanschlüsse der dritten Transistoren fließt.

22. Schaltung nach Anspruch 21, bei der jede der vierten Schaltungen einen zweiten Stromverstärker mit dem zweiten Multiplikationsfaktor aufweist, und der mit der Basis der dritten Transisto-



ren über einen Emitter eines vierten Transistors verbunden ist.

23. Schaltung nach Anspruch 22, bei der der zweite Strommultiplizierer mehrere parallelgeschaltete, fünfte Transistoren aufweist, deren Basisanschlüsse miteinander verbunden sind und dem Emitter des vierten Transistors verbunden sind, deren Emitter jeweils mit dem Anschluß null der Spannungsversorgung über Widerstände verbunden sind, und deren Kollektoren so miteinander verbunden sind, daß sie den fünften Strom an den vorgegebenen unter den Komparatoren liefern, wobei die mehreren parallelgeschalteten fünften Transistoren zusammen mit einem sechsten Transistor, dessen Emitter über einen Widerstand mit dem Anschluß null der Spannungsversorgung verbunden ist, dessen Basis mit der Basis jeden fünften Transistors verbunden ist und dessen Kollektor mit der Basis des vierten Transistors verbunden ist, eine zweite Stromspiegelschaltung bilden.
24. Schaltung nach Anspruch 20, bei der der Wert des zwischen den Emitter des ersten Transistors und den Minusanschluß der Spannungsversorgung geschalteten Widerstands denselben Wert hat wie jeder der Widerstände, die zwischen den Emitter jedes entsprechenden zweiten Transistors und den Minusanschluß geschaltet sind.
25. Schaltung nach Anspruch 22, bei der der erste Stromverstärker den ersten Multiplikationsfaktor 8 aufweist und der zweite Stromverstärker den zweiten Multiplikationsfaktor 8 aufweist.
26. Schaltung nach Anspruch 22, bei der der erste Stromverstärker den ersten Multiplikationsfaktor 4 und der zweite Stromverstärker den zweiten Multiplikationsfaktor 16 aufweist.
27. Schaltung nach Anspruch 23, bei der die Anzahlen der zweiten und fünften Transistoren abhängig vom ersten Multiplikationsfaktor verändert werden.

Revendications

1. Circuit pour compenser une non-linéarité d'entrée/sortie d'un convertisseur analogique/numérique, comprenant :
- (a) un premier dispositif (6a) pour fournir un premier courant ayant une valeur correspondant à un second courant I_E qui est une amplification d'un courant d'entrée I traversant un circuit d'entrée d'un comparateur d'une pluralité de comparateurs (2) dans le conver-

tisseur analogique/numérique à partir d'une chaîne de résistances (1) fournissant chaque tension d'une pluralité de tensions de référence de comparaison à un des comparateurs correspondant ;

(b) un second dispositif (7) pour fournir un troisième courant kI sur la base du premier courant, le troisième courant étant une multiplication du second courant par un premier facteur de multiplication prédéterminé k ;

(c) un troisième dispositif ($Q6_1$, $Q6_2$) pour fournir un quatrième courant $k.I$ sur la base du troisième courant, le quatrième courant étant une multiplication du troisième courant par un inverse d'un facteur d'amplification du circuit d'entrée du comparateur ; et

(d) un quatrième dispositif (8) pour fournir un cinquième courant $k.I.I$ sur la base du quatrième courant, le cinquième courant étant une multiplication du quatrième courant par un second facteur de multiplication prédéterminé l et étant appliqué au circuit d'entrée afin de compenser un premier flux de courant d'entrée totalement fourni à partir d'une alimentation de tension de référence de la chaîne de résistances 1 à un groupe prédéterminé de circuits d'entrée des comparateurs via la chaîne de résistances 1.

2. Circuit selon la revendication 1, dans lequel le premier dispositif (6a) fournit le cinquième courant au circuit d'entrée d'un des autres comparateurs afin de compenser un second flux de courant d'entrée totalement fourni par l'alimentation de tension de référence à un second groupe prédéterminé de circuits d'entrée des comparateurs à la suite du groupe prédéterminé via la chaîne de résistance (1) et du circuit d'entrée d'un autre des autres comparateurs afin de compenser un troisième flux de courant d'entrée totalement fourni par l'alimentation de tension de référence à un troisième groupe de circuits d'entrée des comparateurs via la chaîne de résistance (1) à la suite du second groupe.
3. Circuit selon la revendication 1, dans lequel le premier dispositif (6a) comprend une pluralité de premiers circuits, chaque premier circuit étant un circuit de polarisation fictif ayant la même construction qu'un circuit de polarisation de chaque comparateur et fournissant le premier courant ayant une valeur égale au second courant.
4. Circuit selon la revendication 3, dans lequel le second dispositif (7) comprend une pluralité de premiers multiplieurs de courant dont chacun multiplie le second courant par le premier facteur de multiplication.



5. Circuit selon la revendication 4, dans lequel le premier facteur de multiplication est un entier positif.
6. Circuit selon la revendication 4, dans lequel le quatrième dispositif (8) comprend une pluralité de seconds multiplieurs de courant dont chacun multiplie le quatrième courant par le second facteur de multiplication.
7. Circuit selon la revendication 6, dans lequel le second facteur de multiplication est un entier positif.
8. Circuit selon la revendication 4, dans lequel le premier facteur de multiplication prédéterminé a une valeur différente du second facteur de multiplication prédéterminé.
9. Circuit selon la revendication 4, dans lequel le premier facteur prédéterminé a la même valeur que le second facteur prédéterminé.
10. Circuit selon la revendication 4, dans lequel chacun des premiers multiplieurs de courant constituent un premier circuit de miroir de courant ainsi qu'un transistor émetteur-suiveur prédéterminé (Q3) du premier circuit correspondant.
11. Circuit selon la revendication 6, dans lequel le quatrième dispositif (8) comprend de plus une pluralité de premiers transistors émetteur-suiveurs et dans lequel chacun des seconds multiplieurs de courant constituent un second circuit de miroir ainsi qu'un des transistors émetteur-suiveurs correspondant.
12. Circuit selon la revendication 6, dans lequel le troisième dispositif comprend une pluralité de jeux de premiers transistors chaque jeu de premiers transistors relié entre les premier et second circuits correspondants et ayant un facteur d'amplification de courant d'émetteur relié à la masse égal à celui d'un transistor d'entrée du circuit d'entrée du comparateur.
13. Circuit selon la revendication 12, dans lequel les nombres de premiers circuits, de premiers multiplieurs de courant, de seconds multiplieurs de courant, de jeu des premiers transistors sont mutuellement les mêmes et sont déterminés sur la base du nombre de bits d'un signal numérique de sortie du convertisseur analogique/numérique.
14. Circuit selon la revendication 6, dans lequel chacun des seconds circuits de miroir comprend une pluralité de transistors émetteur-suiveurs parallèles dont les collecteurs sont interconnectés pour fournir le cinquième courant et dont les bases sont interconnectées à un autre transistor pour compenser un facteur d'amplification de courant d'émetteur relié à la masse des premier et second transistors émetteur-suiveurs du second circuit de miroir de courant correspondant.
15. Circuit selon la revendication 1 pour compenser une non-linéarité d'entrée/sortie d'un convertisseur analogique/numérique de 8 bits,
 - (a) dans lequel ledit premier dispositif (6a) comprend trois premiers circuits, chaque premier circuit fournissant un premier courant ayant une valeur correspondant à un second courant I_E qui est une amplification d'un courant d'entrée i passant à travers un circuit d'entrée d'un comparateur d'une pluralité de comparateurs dans le convertisseur analogique/numérique de 8 bits à partir d'une chaîne de résistances fournissant chacun d'une pluralité de niveaux mutuellement différents de tension de référence de comparaison pour un des comparateurs correspondants ;
 - (b) dans lequel ledit second dispositif (7) comprend trois seconds circuits, chaque second circuit fournissant un troisième courant kI_E sur la base du premier courant, le troisième courant kI_E étant une multiplication du second courant I_E par un premier facteur d'un entier positif k ;
 - (c) dans lequel ledit troisième dispositif (Q6₁, Q6₂) comprend trois troisièmes circuits, chaque troisième circuit fournissant un quatrième courant k_i sur la base du troisième courant kI_E , le quatrième courant étant une multiplication du troisième courant kI_E par un inverse d'un facteur β d'amplification de courant d'émetteur relié à la masse du circuit d'entrée ; et
 - (d) dans lequel ledit quatrième dispositif (8) comprend trois quatrièmes circuits, chaque quatrième circuit fournissant un cinquième courant $k\lambda i$ sur la base du quatrième courant, le cinquième courant étant une multiplication du quatrième courant k_i par un second facteur d'un entier positif λ et étant appliqué à un des comparateurs prédéterminé.
16. Circuit selon la revendication 15, dans lequel le premier facteur est 8 et le second facteur est 8.
17. Circuit selon la revendication 16, dans lequel un des trois cinquièmes courants 64i est appliqué au 64ième comparateur, un des deux autres cinquième courant 64i est appliqué au 128ième comparateur, et le cinquième courant restant 64i est appliqué au 192ième comparateur.
18. Circuit selon la revendication 15, dans lequel



chacun des premiers circuits a la même construction qu'un circuit de polarisation de chaque comparateur et comprend un premier transistor émetteur suiveur et une résistance reliée entre le premier transistor et une borne moins d'une alimentation de circuit.

19. Circuit selon la revendication 18, dans lequel chacun des seconds circuits comprend un premier multiplieur de courant ayant le premier facteur de multiplication et relié au premier transistor d'un des premiers circuits correspondants.

20. Circuit selon la revendication 19, dans lequel le premier multiplieur de courant comprend un premier circuit de miroir de courant ainsi que le premier transistor du premier circuit, le premier circuit de miroir de courant ayant une pluralité de seconds transistors reliés en parallèle dont les bases sont interconnectées à la base du premier transistor et dont à travers chacun des émetteurs, le courant égal au premier courant I_E passe via une résistance.

21. Circuit selon la revendication 20, dans lequel chacun des troisièmes circuits comprend deux troisièmes transistors dont les bases, émetteurs et collecteurs sont mutuellement reliés et dont les émetteurs sont reliés aux collecteurs des seconds transistors du premier circuit de miroir de courant pour que le courant exprimé par αI_E (α indique un facteur d'amplification de courant de base relié à la masse) passe dans les bases des troisièmes transistors.

22. Circuit selon la revendication 21, dans lequel chacun des quatrièmes circuits comprend un second multiplieur de courant ayant le second facteur de multiplication et relié à la base des troisièmes transistors via un émetteur d'un quatrième transistor.

23. Circuit selon la revendication 22, dans lequel le second multiplieur de courant comprend une pluralité de cinquièmes transistors reliés en parallèle dont les bases sont mutuellement reliées et reliées à l'émetteur du quatrième transistor, dont les émetteurs sont respectivement reliés à une borne zéro de l'alimentation via des résistances, et dont les collecteurs sont interconnectés pour fournir le cinquième courant à un des comparateurs prédéterminé, la pluralité des cinquièmes transistors reliés en parallèle constituant un second circuit de miroir de courant ainsi qu'un sixième transistor dont l'émetteur est relié à une borne de zéro de l'alimentation via une résistance, dont la base est reliée à la base de chaque cinquième transistor, et dont le collecteur est relié à

la base du quatrième transistor.

24. Circuit selon la revendication 20, dans lequel une valeur de la résistance reliée entre l'émetteur du cinquième transistor et une borne moins de l'alimentation a la même valeur que chacune des résistances reliées entre l'émetteur de chaque second transistor correspondant et la borne moins.

25. Circuit selon la revendication 22, dans lequel le premier multiplieur de courant a le premier facteur de multiplication de 8 et le second multiplieur de courant a le second facteur de multiplication de 8.

26. Circuit selon la revendication 22, dans lequel le premier multiplieur de courant a le premier facteur de multiplication de 4 et le second multiplieur de courant a le second facteur de multiplication de 16.

27. Circuit selon la revendication 23, dans lequel les nombres des second et cinquième transistors varient selon le premier facteur de multiplication.