

CLAIMS

1. An apparatus comprising:
 - a memory device having a device identification; and
 - a low power wake circuit configured to receive a low power wake signal and an identification information, and further configured to initiate a transition of the memory device from a low power state to an active state responsive to an active low power wake signal and the identification information matching the device identification,wherein the memory device matches the identification information and the device information prior to exiting the low power state.
2. The apparatus of claim 1, wherein the low power wake circuit is further configured to receive the low power wake signal via a wake bus, wherein the wake bus is configured to provide only the low power wake signal.
3. The apparatus of claim 1, wherein the low power wake circuit is further configured to receive the identification information via a command/address bus coupled to the memory device.
4. The apparatus of claim 3, wherein the memory device is further configured to receive a chip select signal, the chip select signal configured to enable the low power wake circuit to receive the identification information via the command/address bus.
5. The apparatus of claim 1, further comprising a circuit configured to store the device identification.
6. A system comprising:
 - a plurality of memory devices, each memory device of the plurality of memory devices associated with respective device identification information and configured to have at least one low power state and at least one active state;
 - a wake bus coupled to the plurality of memory devices and configured to provide a wake signal to the plurality of memory devices; and

a command bus coupled the plurality of memory devices and configured to provide wake identification information,

wherein each memory device of the plurality of memory devices are configured to transition from a low power state to an active state responsive to an active wake signal and the wake identification information matching the respective device identification information, and to remain in the low power state responsive to the active wake signal and the wake identification information not matching the respective device identification information.

7. The system of claim 6, further comprising:

a memory controller circuit coupled to the wake bus and the command bus and configured to provide the wake signal and the wake identification information.

8. The system of claim 6, further comprising:

a device identification circuit configured to store the respective device identification information.

9. The system of claim 6, wherein each memory device of the plurality of memory devices comprises a low power wake circuit configured to compare the wake identification information to the respective device identification information.

10. The system of claim 6, further comprising:

a chip select bus, configured to provide a chip select signal to the plurality of memory devices to enable the one or more memory devices to detect the wake signal and the wake identification information.

11. A memory device interface comprising:

a first bus configured to convey a wake signal for initiating a transition in a memory device from a low power state to an active state; and

a second bus configured to convey a wake identification signal, corresponding to a device identifier of the memory device, and

wherein the wake identification signal is matched to the device identifier of the memory device prior to exiting the low power state.

12. The memory device interface of claim 11, further comprising:
a third bus configured to convey a chip select signal for enabling one or more memory devices to process the wake identification signal.
13. The memory device interface of claim 12, wherein an active chip select signal is conveyed on the third bus to the memory device when an active wake signal is conveyed to the memory device.
14. The memory device interface of claim 11, further comprising:
a clock enable bus configured to convey a clock enable signal to the memory device, wherein the clock enable signal is uninterrupted by the wake identification signal and the wake signal conveyed to the memory device.
15. A method comprising:
receiving, by a low power wake circuit, a wake signal configured to initiate a low power state exit operation in a memory device;
receiving, by the low power wake circuit, a signal including wake identification information; and
determining, by the low power wake circuit, whether to initiate a low power state exit operation for an associated memory device based on whether the wake identification information matches a device identifier for the associated memory device when an active wake signal is received by the low power wake circuit.
16. The method of claim 15, further comprising:
responsive to determining that the wake identification information matches the device identifier, initiating a low power state exit operation for the associated memory device.
17. The method of claim 16, further comprising:
responsive to determining that the wake identification information does not match the device identifier, maintaining a low power state for the associated memory device.

18. The method of claim 16, wherein the low power wake circuit receives the wake signal via a dedicated wake bus.
19. The method of claim 16, wherein the wake identification information is received via a command/address bus.
20. The method of claim 16, wherein initiating the low power state exit operation comprises transitioning the associated memory device from a low power state to an active state.