

SILICON THIN FILM TRANSISTOR
AND METHOD FOR PRODUCING THE SAME

5 The present invention relates to a silicon thin film transistor for use in an active matrix type liquid crystal display device or the like, and to a method for producing the same.

10 A conventional silicon thin film transistor is shown in Figure 26, and comprises an insulating substrate 21, a gate electrode 22, a gate insulating layer 23, and impurity doped silicon layer 24 containing suitable amounts of donor or acceptor impurities, an intrinsic silicon layer 25 providing an
15 active layer, a protective insulating layer 26, a source electrode 27 and a drain electrode 28.

 Such a silicon thin film transistor, in which the intrinsic silicon layer 25 and the protective insulating layer 26 are continuously formed, has in theory
20 excellent reliability, reproducibility of characteristics and the like, and has been the subject of widely carried out research and development.

 In the production of the above described conventional silicon thin film transistor, the
25 protective insulating layer 26, formed by the use of silicon nitride or silicon oxide, etc., is removed to expose the intrinsic silicon layer 25, and the impurity doped silicon layer 24 is then formed on the exposed intrinsic silicon layer 25.

30 However, the side of the intrinsic silicon layer 25 adjacent the protective insulating layer 26 has a layer in which nitrogen, oxygen or the like contained in the protective insulating layer 26 has diffused, and when the protective insulating layer 26 is removed,

this layer in which nitrogen, oxygen or the like has diffused cannot also be completely removed. Thus, the interface between the intrinsic silicon layer 25 and the impurity doped silicon layer 24 is imperfect, which introduces a deterioration in the transistor characteristics. The present invention seeks to improve the interface between such an intrinsic silicon layer and an impurity doped silicon layer, and to provide a silicon thin film transistor with improved characteristics. The invention further seeks to provide a method for producing such a transistor.

According to one particular aspect of the present invention there is provided a silicon thin film transistor having an insulating substrate, and gate, source and drain electrodes, the gate electrode being provided on the insulating substrate under a gate insulating layer, and the source and drain electrodes being arranged to contact respectively each of the two parts of an impurity doped silicon layer, which parts are formed on the gate insulating layer and are joined by an intrinsic silicon layer formed in overlapping contact on the two parts of the impurity doped silicon layer and on the gate insulating layer in between the two parts.

According to another aspect of the invention, there is provided a method for producing a silicon thin film transistor comprising forming a gate electrode on an insulating substrate, forming a gate insulating layer on the insulating substrate bearing the gate electrode, forming an impurity doped silicon layer in two parts on the gate insulating layer, forming an intrinsic silicon layer in overlapping contact on the two parts of the impurity doped silicon layer and on the gate insulating layer between the two parts of the impurity doped silicon layer, and providing a source

electrode and a drain electrode in contact respectively with each of the two parts of the impurity doped silicon layer.

5 The present invention will be described further, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a plan view showing a first embodiment of silicon thin film transistor according to the present invention;

10 Figures 2 (a) to 2 (c) are sectional views on the line II - II in Figure 1 showing the production of the silicon thin film transistor of Figure 1;

15 Figure 3 is a plan view showing a second embodiment of silicon thin film transistor according to the present invention;

Figure 4 is a sectional view on the line IV - IV in Figure 3;

20 Figure 5 is a plan view showing a third embodiment of silicon thin film transistor according to the present invention;

Figure 6 is a sectional view on the line VI - VI in Figure 5;

25 Figure 7 is a plan view showing a fourth embodiment of silicon thin film transistor according to the present invention;

Figure 8 is a sectional view on the line VIII - VIII in Figure 7;

30 Figures 9 and 10 are plan views showing a fifth embodiment of silicon thin film transistor according to the present invention;

Figures 11 (a) to 11 (c) are sectional views showing the production of a sixth embodiment of silicon thin film transistor according to the present invention;

5 Figures 12 (a) to 12 (c) are sectional views showing the production of a seventh embodiment of silicon thin film transistor according to the present invention;

10 Figure 13 is a sectional view showing an eighth embodiment of silicon thin film transistor according to the present invention;

 Figures 14 (a) to 14 (d) are sectional views showing the production of a ninth embodiment of silicon thin film transistor according to the present invention;

15 Figure 15 is a plan view showing a first application of the silicon thin film transistor according to the present invention in an active matrix type liquid crystal display device;

 Figure 16 is a sectional view on the line XVI - XVI in Figure 15;

20 Figure 17 is a plan view showing a second application of the silicon thin film transistor according to the present invention in an active matrix type liquid crystal display device;

25 Figure 18 is a sectional view on the line XVIII - XVIII in Figure 17;

 Figure 19 is a plan view showing a third application of silicon thin film transistor according to the present invention in an active matrix type liquid crystal display device;

30 Figure 20 is a sectional view on the line XX - XX in Figure 19;

 Figure 21 is a sectional view on the line XXI - XXI in Figure 19;

 Figure 22 is a plan view showing a fourth

application of the silicon thin film transistor according to the present invention in an active matrix type liquid crystal display device;

5 Figure 23 is a sectional view on the line XXIII - XXIII in Figure 22;

Figure 24 is a plan view showing a fifth application of silicon thin film transistor according to the present invention in an active matrix type liquid crystal display device;

10 Figure 25 is a sectional view on the line XXV - XXV in Figure 24; and

Figure 26 is a sectional view through a conventional silicon thin film transistor.

15 A first embodiment of silicon thin film transistor is shown in Figures 1 and 2 and comprises an insulating substrate 1 formed from glass or the like, a gate electrode 2 formed of Cr (chromium), a gate insulating layer 3 formed of silicon nitride or silicon oxide, a first impurity doped silicon layer 4 formed of amorphous silicon containing suitable amounts of donor or acceptor impurities, an intrinsic silicon layer 5 formed of amorphous silicon and providing an active layer, and a protective insulating layer 6 formed of silicon nitride or silicon oxide. A source electrode 7 and a drain electrode 8 formed of ITO (indium tin oxide) are connected to the first impurity doped silicon layer 4 at exposed contact regions 9 of the first impurity doped silicon layer 4.

25 The production method of such a silicon thin film transistor is shown in Figures 2 (a) to 2 (c).

30 Initially, as shown in Figure 2 (a), the gate electrode 2 is formed on the insulating substrate 1. The gate insulating layer 3 is formed on the insulating substrate 1 carrying the gate electrode 2, and the

first impurity doped silicon layer 4 is formed on the gate insulating layer 3 in two parts, the two parts of the first impurity doped silicon layer 4 being formed by etching in such a manner that they transversely cross the terminal part of the gate electrode 2.

The intrinsic silicon layer 5 and the protective insulating layer 6 are each formed as a continuous layer next, and, by the use of a photo-resist as a mask, the protective insulating layer 6 is etched using a buffered fluoric acid solution and, further, the intrinsic silicon layer 5 is etched using a dry etching method involving a CF gas, to expose the first impurity doped silicon layer 4 as shown in Figure 2 (b). After cleaning the surface of the exposed regions of the first impurity doped silicon layer 4 with a fluoric acid diluted by an aqueous solution, the photo-resist is peeled off. In this manner, the intrinsic silicon layer 5 and the protective insulating layer 6 are formed in the same pattern on the gate insulating layer 3 and the two parts of the first impurity doped layer 4.

The source electrode 7 and the drain electrode 8 are then formed as shown in Figure 2 (c) in such a manner that they contact the first impurity doped silicon layer 4 in the exposed contact regions 9.

In the present embodiment, since the intrinsic silicon layer 5 is formed on the first impurity doped silicon layer 4, and the protective insulating layer 6 is formed on the intrinsic silicon layer 5, the join between the first impurity doped silicon layer 4 and the intrinsic silicon layer 5 is improved, and good transistor characteristics may be obtained.

Also, although the impurity doped silicon layer 4 and the intrinsic silicon layer 5 are both discontinuous in the present example, it has been experimentally

determined that, in the case of using an amorphous silicon to produce the first impurity doped silicon layer and the intrinsic silicon layer, a better join can be obtained by forming the intrinsic silicon layer on the first impurity doped silicon layer, and by forming the first impurity doped silicon layer on the intrinsic silicon layer. Therefore, in this respect, the present embodiment is better than the conventional example.

Figures 3 and 4 show a second embodiment of silicon thin film transistor in which the intrinsic silicon layer 5 is formed only over the interior of the gate electrode 2.

In a silicon thin film transistor, and particularly in one in which amorphous silicon is used in the intrinsic silicon layer 5, the off current is increased in the case where the intrinsic silicon layer 5 is irradiated with light.

In the present instance, since the intrinsic silicon layer 5 is formed only above the interior of the gate electrode 2, light passing through the insulating substrate 1 is completely blocked and does not reach the intrinsic silicon layer 5. Therefore, an increase in off current due to light irradiation can be avoided to a large extent.

The present example can, of course, only be realised by changing the mask pattern employed in the case of the first embodiment.

A third embodiment of silicon thin film transistor according to the present invention, in which each contact region 9 is formed outside the area of the gate electrode 2, is shown in Figures 5 and 6.

In the first embodiment, as shown in Figure 2 (c), the contact region 9 is formed over the terminal

part of the gate electrode 2 and the overlap between the gate electrode 2 and the first impurity doped silicon layer 4 becomes $2L$, taking the design limit as L . On the other hand, in the present embodiment as shown in Figure 6, such overlap is simply L .

As is well known, increasing the overlap retards the response speed. Therefore, since, in the present embodiment, the overlap can be halved by comparison with the first embodiment, improvements in the response speed of the transistor can be obtained.

As before, the present embodiment is only possible by changing the mask pattern employed.

Figures 7 and 8 show a fourth embodiment of silicon thin film transistor according to the present invention, in which the terminal part of the intrinsic silicon layer 5 is positioned to extend beyond the edge of the gate electrode 2, and not so far as the edge of the first impurity doped silicon layer 4.

In the present instance, the light passing through the insulating substrate 1 and reaching the portions of the intrinsic silicon layer 5 formed beyond the outside of the gate electrode 2 can be reduced to a large extent over the whole area of the intrinsic silicon layer 5 formed outside the gate electrode 2 by the first impurity doped silicon layer 4. Consequently, the off current of the transistor during light irradiation can be decreased to a large extent.

Again, the present embodiment can only be realised by changing the mask pattern.

Figures 9 and 10 show a fifth embodiment of silicon thin film transistor according to the present invention, in which opposed edges of the two parts of the first impurity doped silicon layer 4 under the intrinsic silicon layer 5 are formed in the shape of

comb teeth. Since both the first impurity doped silicon layer 4 and the intrinsic silicon layer 5 are discontinuous, the join between the two might not be wholly satisfactory, even if it is improved by comparison with that in the conventional case. When the junction is insufficient, parasitic resistance occurs in the region of the join, and the on current of the transistor is lowered. However, since the opposed edges of the two parts of the first impurity doped silicon layer 4 are formed in an uneven shape, the parasitic resistance at the join decreases whereby the lowering of the on current of the transistor may be prevented.

In the example of Figure 9, the two opposed edges are formed such that a convex edge section is opposed to a convex edge section, and a concave edge section is opposed to a concave edge section. In the example of Figure 10, the two opposed edges are formed such that a concave edge section is opposed to a convex edge section.

Again, the present example can only be realised by changing the mask pattern employed.

Figures 11 (a) to 11 (c) show the production of a sixth embodiment of silicon thin film transistor according to the present invention.

First, the gate electrode 2 having light shielding properties is formed on the insulating substrate 1 having light transparent properties, and the gate insulating layer 3 is formed on the insulating substrate 1 bearing the gate electrode 2. The first impurity doped silicon layer 4 is formed on the gate insulating layer 3, and is patterned by etching into two parts formed in such a manner that they transversely cross the terminal part of the gate electrode 2.

Successively, the intrinsic silicon layer 5 and the protective insulating layer 6 are formed on the gate insulating layer 3 and the first impurity doped silicon layer 4, a photo-resist 11 is coated on the protective insulating layer 6, and the rear surface of the insulating substrate 1 is irradiated with ultra-violet rays 12 to expose the photo-resist 11 using the gate electrode 2 as a mask (see Figure 11 (a)).

Next, as shown in Figure 11 (b), the photo-resist 11 is shaped to correspond with the gate electrode 2 by developing the existing photo-resist 11, and the protective insulating layer 6 and the intrinsic silicon layer 5 are etched, using this photo-resist as a mask, to match the shape of the intrinsic silicon layer 5 and the protective insulating layer 6 connecting the two parts of the impurity doped silicon layer 4 to the gate electrode 2.

Following this, the photo-resist is peeled off as shown in Figure 11 (c), and the source electrode 7 and the drain electrode 8 are formed in such a manner that they contact the contact regions 9 of the two parts of the first impurity doped silicon layer 4.

In the silicon thin film transistor produced in the manner just described, since the intrinsic silicon layer 5 and the protective insulating layer 6 are patterned utilising the pattern of the gate electrode 2, the number of photo-masks employed for one sheet can be reduced by comparison with the number employed in the production of the first embodiment.

Since the first impurity doped silicon layer 4 absorbs ultra-violet rays 12, in the present instance it is preferable to make the impurity doped silicon layer as thin as possible.

The production of a seventh embodiment of silicon

thin film transistor according to the present invention is shown in Figures 12 (a) to 12 (c).

5 As before, the gate electrode 2 having light shielding properties is formed on the insulating substrate 1 having light transparent properties, the gate insulating layer 3 is formed on the insulating substrate 1 bearing the gate electrode 2, and the first impurity doped silicon layer is formed on the gate insulating layer 3. The first impurity doped silicon layer 4 is etched to form the layer into two parts in such a manner that they transversely cross the terminal part of the gate electrode 2.

10 Successively, the intrinsic silicon layer 5 and the protective insulating layer 6 are formed on the gate insulating layer 3 and the first impurity doped silicon layer 4, and the photo-resist 11 is coated on the protective insulating layer 6. Ultra-violet rays are directed through the rear surface of the insulating substrate 1 to expose the photo-resist 11, using the gate electrode 2 and the first impurity doped silicon layer 4 as masks, as shown in Figure 12 (a).

20 The photo-resist 11 is then developed to form it into a shape which corresponds with the gate electrode 2 and the first impurity doped silicon layer 4, and the protective insulating layer 6 and the intrinsic silicon layer 5 are etched, using this photo-resist 11 as a mask, to form the intrinsic silicon layer 5 and the protective insulating layer 6 into a pattern corresponding with the gate electrode 2 and the first impurity doped silicon layer 4 and connecting the two parts of the first impurity doped silicon layer 4, as shown in Figure 12 (b).

30 Afterwards, the photo-resist 11 is peeled off, and the source electrode 7 and the drain electrode 8 are

formed in such a manner that they contact the contact regions 9 of the two parts of the first impurity doped silicon layer 4, as shown in Figure 12 (c).

5 In the silicon thin film transistor produced as just described, since the pattern of the intrinsic silicon layer 5 and the protective insulating layer 6 are formed utilising the pattern of the gate electrode 2 and the first impurity doped silicon layer 4, the number of photo-masks employed for one sheet can again
10 be reduced by comparison with the first embodiment.

In this instance, since it is required that the ultra-violet rays are substantially absorbed by the first impurity doped silicon layer 4, it is preferable to make the first impurity doped silicon layer as thick
15 as possible.

Figure 13 shows an eighth embodiment of silicon thin film transistor according to the present invention, in which an auxiliary electrode 10 is formed so as to contact the first impurity doped silicon layer 4 and cover stepped portions of the source electrode 7 and the
20 drain electrode 8 provided at the terminal parts of the first impurity doped layer 4. Thus, even if one of the source electrode 7 and the drain electrode 8 is broken where the step occurs, electrical connection is still ensured by the auxiliary electrode 10.
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The auxiliary electrode 10 may be formed from Ti (titanium) or the like.

Figure 14 (d) shows a ninth embodiment of silicon thin film transistor according to the present invention
30 having an insulating substrate 1, a gate electrode 2 formed of Cr (chromium), a gate insulating layer 3 formed of silicon nitride, a first impurity doped silicon layer 4 comprising amorphous silicon containing n-type impurities such as phosphorous or the like, an

intrinsic silicon layer 5 providing an active layer and also comprising amorphous silicon, and a second impurity doped silicon layer 4a containing impurities of the opposite type from the impurities in the first impurity doped silicon layer 4, that is p-type impurities such as boron or the like. A protective insulating layer 6 of silicon nitride or the like is formed on the layer 4a, and a source electrode 7 and a drain electrode 8 of ITO (indium tin oxide) or a metal are also provided.

The production of this silicon thin film transistor will now be described with reference to Figures 14 (a) to 14 (d).

The gate electrode 2 is formed first on the insulating substrate 1, and the gate insulating layer 3 is then formed on the insulating substrate 1 over the gate electrode 2. The first impurity doped silicon layer 4 is then formed in two parts on the gate insulating layer 3 in such a manner that these parts overlap the gate electrode 2, as shown in Figure 14 (a).

Next, the intrinsic silicon layer 5, the second impurity doped silicon layer 4a, and the protective insulating layer 6 are formed continuously, as shown in Figure 14 (b). The formation of the second impurity doped silicon layer 4a can be by plasma CVD, optical CVD, ion implanting using boron or the like, or electrical discharge using a gas such as B_2H_6 or the like.

By successive etching of the protective insulating layer 6, the second impurity doped silicon layer 4a, and the intrinsic silicon layer 5 using the same mask, the three layers are formed into patterns of the same shape as shown in Figure 14 (c). Pattern formation is

carried out in such a manner that the intrinsic silicon layer 5 connects the two parts of the first impurity doped silicon layer 4.

5 The source electrode 7 and the drain electrode 8 connected to the two parts of the impurity doped silicon layers 4 are then formed as shown in Figure 14 (d).

10 In the present embodiment, since the intrinsic silicon layer 5 and the second impurity doped silicon layer 4a are formed continuously, the interface between the two layers is extremely clean.

Further, since the second impurity doped silicon layer 4a and the protective insulating layer 6 are also formed continuously, a clean interface is obtained between these two layers also.

15 As an alternative to the structure just described, the first impurity doped silicon layer 4 may have p-type impurities, the second impurity doped layer 4a then having n-type impurities.

20 Figures 15 and 16 show the application of the silicon thin film transistor according to the present invention to an active matrix type liquid crystal display device.

25 In this display device, gate wiring 13 is formed at the same time as the formation of the gate electrode 2, and source wiring 14 and a picture element electrode 15 are formed at the same time as the formation of the source electrode 7 and the drain electrode 8. Therefore, the formation of these elements can be achieved without substantially increasing the number of masks.

30 Cr or the like can be used for the gate electrode 2 and the gate wiring 13, and ITO or the like can be used for the source electrode 7, the drain electrode 8, the source wiring 14, and the picture element electrode 15.

In a modification of the display device, as shown in Figures 17 and 18, the first impurity doped silicon layer 4 is provided in parallel with the source wiring 14. In other respects, the display device of Figures 17 and 18 is the same as that of Figures 15 and 16.

However, these display devices may be subjected to various problems as described below:

In the production step shown in Figure 2 (b), it is necessary to clean the exposed surface of the first impurity doped silicon layer 4 by the use of a fluororic acid diluted by an aqueous solution. At this time, the gate insulating layer 3 is also etched, since the silicon nitride and silicon oxide used in the gate insulating layer 3 are readily etched by the diluted fluororic acid, and so the thickness of the gate insulating layer 3 may be considerably reduced due to the etching. Therefore, referring to Figures 15 and 16, poor insulation is apt to occur between the gate wiring 13 and the source wiring 14 at the cross over between the gate wiring and the source wiring.

Therefore, in an application of the silicon thin film transistor according to the invention to an active matrix type liquid crystal display device as shown in Figures 19, 20 and 21, a third impurity doped silicon layer 4b is provided to inhibit the occurrence of poor insulation. The third impurity doped silicon layer 4b is formed at the same time as the first impurity doped silicon layer 4 and in such a manner as to cover the gate insulating layer 3 at the cross over of the gate wiring 13 and the source wiring 14. Due to such an arrangement, the gate insulating layer 3, where it is covered with the third impurity doped silicon layer 4b, is not etched at the time of cleaning the exposed surface of the first impurity doped silicon layer with

the diluted fluoric acid, and so its thickness is not reduced.

However, as shown in Figure 20, the source wiring 14 is required to cross the transverse step between the top of the third impurity doped silicon layer 4b and the adjacent surface of the gate insulating layer 3 generated by the etching by the diluted fluoric acid, and a break in the source wiring is apt to occur at this step.

Therefore, in a modification as shown in Figures 22 and 23, the third impurity doped silicon layer 4b is formed for approximately the whole length of the source wiring 14 to be wider than the width of the source wiring 14.

In this case, as shown in Figure 23, the step in the gate insulating layer 3 generated by the etching by the diluted fluoric acid is absent, and so breakage of the source wiring 14 can be reduced.

Furthermore, since the third impurity doped silicon layer 4 absorbs light, light leakage is reduced and the contrast of the active matrix type liquid crystal display device is improved.

A further application of the silicon thin film transistor according to the present invention in an active matrix type liquid crystal display device is shown in Figures 24 and 25. Again, the third impurity doped silicon layer 4b is formed on the gate insulating layer 3 for almost the whole length of the source wiring 14 in a width wider than that of the source wiring 14.

Moreover, the intrinsic silicon layer 5 and the protective insulating layer 6 are additionally formed as layers 5a and 6a on this third impurity doped silicon layer 4b in such a manner that they cover the cross over between the gate wiring 13 and the source wiring 14.

The intrinsic silicon layer 5a and the protective insulating layer 6a are, of course, provided at the same time as the formation of the intrinsic silicon layer 5 and the protective insulating layer 6.

5 Since the intrinsic silicon layer 5a and the protective insulating layer 6a are formed at the cross over of the gate wiring 13 and the source wiring 14, in addition to the gate insulating layer 3 and the third impurity doped silicon layer 4b, poor insulation
10 between the gate wiring 13 and the source wiring 14 can be reduced to a large extent.

 In the above described embodiments, silicon nitride, silicon oxide or a multi-layered film of silicon nitride and silicon oxide are preferably
15 employed for the gate insulating layer 3. Further, although the use of an amorphous silicon is desirable for each of the impurity doped silicon layer 4 and the intrinsic silicon layer 5, a poly-crystalline silicon or the like can also be used. The protective
20 insulating layer 6 may be silicon nitride, silicon oxide or the like.

 According to the present invention, the interface between the impurity doped silicon layer 4 and the intrinsic silicon layer 5 is improved, and good transistor characteristics can be obtained.
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 The following further advantages can also be obtained by the use of the various modifications as described:

30 By forming the intrinsic silicon layer 5 over the interior of the gate electrode 2, the off current at the time of light irradiation can be reduced to a large extent.

 In the embodiments in which the contact regions 9 are formed outside the edges of the gate electrode 2,

the overlap capacity is reduced and the response properties of the transistor may be enhanced.

5 By positioning the terminal parts of the intrinsic silicon layer 5 outside the area of the gate electrode 2 and inside the area of the impurity doped silicon layer 4, the off current at the time of light irradiation can be reduced to a large extent.

10 By forming the opposing edges of the two parts of the impurity doped silicon layer 4 under the intrinsic silicon layer 5 in the shape of comb teeth, the parasitic resistance is reduced and lowering of the on current of the transistor may be prevented.

15 In the production method in which the photo-resist 11 on the protective insulating layer 6 is exposed from the rear surface of the insulating substrate 1 and developed to form a mask for creating the pattern of the intrinsic silicon layer 5 and the protective insulating layer 6, the number of masks can be decreased, resulting in a cost reduction and an improvement in yield.

20 In the case in which the second impurity doped silicon layer 4a containing impurities of the type opposite to the impurities in the first impurity doped silicon layer 4 is provided, since the impurity doped silicon layer 4 and the protective insulating layer 6 are continuously formed, a clean interface can be obtained.

25 Also, if a plurality of the silicon thin film transistors of the present invention are provided in an array like arrangement, an excellent array with the various above features can be obtained.

30 In such a case in which the third impurity doped silicon layer 4b is formed in such a manner as to cover the gate insulating layer 3 positioned at the cross over

of the gate wiring 13 and the source wiring 14, poor insulation at the cross over can be avoided.

Further, in a silicon thin film transistor array in which the third impurity doped silicon layer 4b is formed over approximately the whole area of the source wiring 14 with a width wider than that of the source wiring, poor insulation between the gate wiring 13 and the source wiring 14 can be reduced to a large extent.

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C L A I M S

1. A silicon thin film transistor having an insulating substrate, and gate, source and drain electrodes, the gate electrode being provided on the insulating substrate under a gate insulating layer, and the source and drain electrodes being arranged to contact respectively each of the two parts of an impurity doped silicon layer, which parts are formed on the gate insulating layer and are joined by an intrinsic silicon layer formed in overlapping contact on the two parts of the impurity doped silicon layer and on the gate insulating layer in between the two parts.
2. A silicon thin film transistor as claimed in claim 1 in which the intrinsic silicon layer is formed within the projected area of the gate electrode.
3. A silicon thin film transistor as claimed in claim 1 in which contact regions, in which the source and drain electrodes contact the two parts of the impurity doped silicon layer, are formed outside the projected area of the gate electrode.
4. A silicon thin film transistor as claimed in claim 1 in which the edge of the intrinsic silicon layer is positioned outside the projected area of the gate electrode and inside the area of the impurity doped silicon layer.
5. A silicon thin film transistor as claimed in any of claims 1 to 4 in which opposed edges of the two parts of the impurity doped silicon layer under the intrinsic silicon layer are formed in the shape of comb teeth.
6. A silicon thin film transistor as claimed in any of claims 1 to 5 further having a protective insulating layer formed on the intrinsic silicon layer to cover the same area.



7. A silicon thin film transistor as claimed in claim 6 in which the intrinsic silicon layer and the protective insulating layer are formed to match the shape of the gate electrode.

8. A silicon thin film transistor as claimed in claim 6 in which the intrinsic silicon layer and the protective insulating layer are formed to match the outline of the gate electrode and the impurity doped silicon layer.

9. A silicon thin film transistor as claimed in any of claims 1 to 5 in which a second impurity doped silicon layer containing impurities of the reverse type to the impurities in the first impurity doped silicon layer is formed on the intrinsic silicon layer in the same shape as the intrinsic silicon layer.

10. A silicon thin film transistor as claimed in claim 9 in which a protective insulating layer is formed on the second impurity doped silicon layer to cover the same area.

11. A silicon thin film transistor array comprising a plurality of silicon thin film transistors as claimed in any preceding claim, gate wiring for inter-connecting the gate electrodes of the silicon thin film transistors, and source wiring for inter-connecting the source electrodes of the silicon thin film transistors.

12. A silicon thin film transistor array as claimed in claim 11 in which each silicon thin film transistor has a further impurity doped silicon layer formed on the gate insulating layer at a cross over of the gate wiring and the source wiring.

13. A silicon thin film transistor array as claimed in claim 12 in which the further impurity doped silicon layer is formed continuously over substantially the whole area of the source wiring so as to be wider than



the source wiring.

14. A method for producing a silicon thin film transistor comprising forming a gate electrode on an insulating substrate, forming a gate insulating layer on the insulating substrate bearing the gate electrode, forming an impurity doped silicon layer in two parts on the gate insulating layer, forming an intrinsic silicon layer in overlapping contact on the two parts of the impurity doped silicon layer and on the gate insulating layer between the two parts of the impurity doped silicon layer, and providing a source electrode and a drain electrode in contact respectively with each of the two parts of the impurity doped silicon layer.

15. A method as claimed in claim 14 further comprising forming a protective insulating layer on the intrinsic silicon layer, coating a photo-resist on the protective insulating layer, exposing a portion of the photo-resist using the gate electrode as a mask to ultra-violet rays passing through the insulating substrate, developing the photo-resist, and using the developed photo-resist as a mask etching the protective insulating layer and the intrinsic silicon layer to match the shape of the gate electrode.

16. A method as claimed in claim 14 further comprising forming a protective insulating layer on the intrinsic silicon layer, coating a photo-resist on the protective insulating layer, exposing a portion of the photo-resist using the gate electrode and the impurity doped silicon layer as masks to ultra-violet rays passing through the insulating substrate, developing the photo-resist, and using the developed photo-resist as a mask etching the protective insulating layer and the intrinsic silicon layer to match the outline of the gate electrode and the impurity doped silicon layer.



17. A method as claimed in claim 14 further comprising forming a second impurity doped silicon layer containing impurities of the reverse type to the impurities in the first impurity doped silicon layer and a protective insulating layer on the intrinsic silicon layer, and patterning the protective insulating layer, the second impurity doped silicon layer, and the intrinsic silicon layer in the same shape.

18. A silicon thin film transistor substantially as herein particularly described with reference to and as illustrated in any of Figures 1 to 14 of the accompanying drawings.

19. A silicon thin film transistor array substantially as herein particularly described with reference to and as illustrated in any of Figures 15 to 25 of the accompanying drawings.

20. A method of producing a silicon thin film transistor substantially as herein particularly described with reference to and as illustrated in any of Figures 2, 11, 12 or 14 of the accompanying drawings.
