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INTEGRATED CIRCUIT ASSEMBLY HAVING OUTPUT PADS WITH APPLICATION SPECIFIC CHARACTERISTICS AND METHOD OF OPERATION

Reference to Related Application

This is a continuation-in-part of U.S. Patent Application Serial Number 08/960,408,
5 entitled "INTEGRATED CIRCUIT ASSEMBLY HAVING OUTPUT PADS WITH
PROGRAMMABLE CHARACTERISTICS AND METHOD OF OPERATION," filed
October 29, 1997.

Field of the Invention

This invention relates to methods and apparatus for driving an integrated circuit (IC)
10 output pad, and more particularly to compensation for application specific electromagnetic
interference (EMI).

Background and Summary of the Invention

Electronic integrated circuits are provided with output pads to which external electronic
circuitry is electrically connected. Output pads may provide a logic signal of "1" or "0", or
15 an elevated or zero voltage to indicate a logic state. To overcome the impedance of the
external circuitry, each pad is provided with a driver, typically in the form of a pair of FET
transistors connected in series, with the junction between the two connected to the output
pad, and the remote connections of the pair connected to a power line and to ground,
respectively.

20 ICs are typically installed on a printed circuit assembly (PCA) with other components,
and other circuit assemblies or devices may be connected to the PCA. The output pad may

be required to drive a load remote from the IC, after transmission via metal traces on the PCA or via other conductors. The interactions of rapidly switching signals on these traces may generate an unwanted EMI problem. While rapid switching may be desirable for high speed circuit operation, this increases EMI noise. Therefore, circuits are evaluated and
5 provided with EMI filtration components where EMI exceeds allowable levels. However, the addition of these components on the lines driven by an output pad changes the impedance of the line, which changes the requirements on the driver on the IC. For certain applications, an IC may be custom designed to have driver capabilities at each output pad precisely matched to the intended application and PCA on which it is to be installed. This
10 would provide driving capabilities that are adequate to overcome external impedance, yet below a level that generates excessive EMI.

However, it is impractical or cost ineffective to design an IC twice: once to prototype the system for EMI analysis, and a second time with adequate drive capabilities to accommodate EMI reduction measures. Even when computer simulations of circuit
15 performance are adequate to predict EMI measures and design adequate drivers in a single iteration, a separate chip design is required for each product or circuit assembly on which the chip is to be used.

Existing ICs have output pads with two drivers per pad, so that a driver may be disabled during operational periods when switching noise within the IC is excessive. Such a system
20 is disclosed in US Patent No. 5,039,878 to Anderson, the disclosure of which is incorporated herein by reference. However, such systems do not accommodate the impedance variations generated by off-chip components and simply respond to excessive noise on a ground line.

Output pad requirements increasingly may require the driving of small loads at very high
25 speeds. These drive speeds may include running at the internal speed of the ASIC, at up to the highest clock frequency. The use of such high frequencies may worsen various of the EMI parasitic parameters, including series inductance due to the ASIC wire bonds and chip package leads, parallel capacitance to adjacent leads and ground, and mutual inductive

coupling between adjacent wires and leads. At the PCA, a transmission line effect may occur, giving rise to signal reflections that may cause serious ringing at the load. Ringing may produce ground bounce, supply line bounce, and EMI. When ringing is significant, it may generate apparent multiple data transitions at the load when only a single transition
5 between logic states has occurred at the input, generating errors.

Ringing may be exacerbated by the effect of component resonances, and when such resonant frequencies are within the range of the data rate, external damping components are required, complicating the circuit design, and possibly requiring unwanted design iterations.

Existing designs have sought to overcome ringing concerns by using larger drivers to
10 provide a faster edge or transition rate, and to delay reading of the signal for an interval to allow ringing to damp out. However, as data rates increase, there is inadequate time between data transitions to permit ringing to damp.

The present invention overcomes the limitations of the prior art by providing an application specific integrated circuit for use with a circuit having particular electrical
15 characteristic such as ringing or impedance. The circuit has an output pad with an output transistor having a drain connected to the output pad, and a gate connected to the drain of a predriver transistor. The output transistor has a gate-source capacitance characteristic, and the predriver transistor has a resistance that produces a time constant above a selected threshold based on the electrical characteristic. The first predriver transistor also has a
20 selected resistance based on the predriver time constant and the gate-source capacitance characteristic, such that the first predriver is operable to switch the output transistor at a sufficiently slow rate to avoid ringing.

Brief Description of the Drawings

Fig. 1 is a schematic block diagram of a circuit according to a preferred embodiment of
25 the invention.

Fig. 2 is a schematic block diagram of a circuit according to an alternative embodiment of the invention.

Fig. 3a is a timing diagrams illustrating operation of a prior art apparatus.

Figs. 3b-3e are a series of timing diagrams illustrating operation of the embodiment of Fig. 2.

Detailed Description of a Preferred Embodiment

Figure 1 shows a printed circuit assembly 10 on which is mounted a chip carrier 12 carrying an integrated circuit (IC) chip 14. The chip includes a microprocessor logic controller 16 that is interconnected to control all chip functions. An output pad 20 represents one of numerous output pads for expressing a digital signal from the chip.

A pad driver circuit 22 has an output line 24 connected to the pad, a voltage line 26 connected to a voltage source Vdd, and a ground line 30 connected to ground. The driver circuit shown has four pad driver transistor pairs 32, 34, 36, 38. Each pair includes a p-channel FET and an n-channel FET connected with the p-FET drain connected to the n-FET drain, with the source of the p-channel FET connected to Vdd line 26 and the source of the n-channel FET connected to ground 30. Pair 32 includes p-FET 40 and n-FET 42. FET 40 has a first line 44 connected to Vdd line 26, a second line 46 connected to the output line 24, and a gate 52. FET 42 has a first line 54 connected to the output line 24 and to the second line 46 of FET 40, a second line 56 connected to the ground line 30, and a gate 60.

FET pairs 34 includes a p-FET 64 and an n-FET 66, pair 36 includes FETs 70 and 72, and pair 38 includes FETs 74 and 76. The p-FETs 40, 64, 70, and 74 are all connected to Vdd line 26, and n-FETs 42, 66, 72, and 76 are connected to ground line 30. The p-FETs 40, 64, 70, and 74 have respective gate lines 52, 80, 82, 84, and n-FETs 42, 66, 72, and 76 have respective gate lines 60, 86, 90, 92.

Each of the gate lines 52, 80, 82, 84 of the p-FETs is connected respectively to the output line of a NAND gate 100, 102, 104, 106. Each of the gate lines 60, 86, 90, 92 of the n-FETs is connected respectively to the output line of a NOR gate 110, 112, 114, 116. Each of the NAND and NOR gates has three inputs: a first data input connected to a DATA line on microprocessor 16, a second enable line connected to an output enable (OE) on the microprocessor, and a control line. An inverter 120 on the OE line between the processor

and the NOR gates provides an inverted OE signal, while the NAND gates directly receive the original OE signal.

A separate control line is connected to each of the NAND gates, and each line is shared with a respective NOR gate. The processor 16 includes three control line outputs 1, 2, and 3, which is one less than the number of FET pairs. Control line 1 connects to NAND gate 102 and NOR gate 112, control line 2 connects to NAND gate 104 and NOR gate 114, control line 3 connects to NAND gate 106 and NOR gate 116. Gates 100 and 110 are wired with their control inputs directly connected to the data line so that they receive a high control bit when the data line is high. This ensures that these gates will always be on, while the others may be selectively utilized based on the processor's control bit output.

The NAND gates conventionally operate to provide a low or "0" output when all three inputs are high (causing an associated p-FET to conduct, and pulling the output line up to Vdd), and provide a high or "1" output when one or more of the inputs are low (preventing p-FET conduction). The NOR gates conventionally operate to provide a low or "0" output when one or more inputs are high (preventing an associated n-FET from conducting), and a high or "1" output when all inputs are low (pulling the output line down to ground.)

Thus, when the enable line OE is high and the data line switches high (as when a "leading edge" of a digital signal occurs) any control lines at high (including the data-following control line of gate 100) will cause their associated NAND gate to send a "0", causing some p-FETs to conduct. Meanwhile, the inverter 120 on the enable line will pass a low "0" signal to the enable lines of each of the NOR gates, which are effectively enabled by a "0" and disabled by a "1". Thus, a single enable bit will affect the entire circuit simultaneously.

On the data line, a "1" effectively enables or operates the NAND gates and disables the NOR gates, while a "0" functions conversely. Consequently, the data line circuit logic prevents enablement of any p-FETs when any n-FET is enabled, and vice versa, avoiding an intolerable connection between Vdd and ground within the chip.

On each of the control lines to the NOR gates, an inverter 122 takes a high control bit and inverts it to the low level needed to activate the gate, and conversely disables the selected gate when the microprocessor outputs a low control bit.

In the preferred embodiment, the FET transistors are sized in incremental multiples of two, providing a wide range of selectable aggregate effective sizes. The first p-FET 40 is the smallest size x , with p-FET 64 at $2x$, p-FET 70 at $4x$, p-FET 74 at $8x$. Thus, with four transistors, the effective size of the transistor may range between $1x$ and $15x$, in quantum increments of $1x$, depending on which permutation of transistors is selected. In the preferred embodiment with FET 40 permanently wired to be on when enabled and data high, the possible aggregate sizes are $1x$, $3x$, $5x$... $15x$. Where finer increments are desired, the first transistor may be wired with a switchable control bit. The n-FETs are similarly sized, although the number of n-FETs may differ from the number of p-FETs, as may the progression of sizes.

As long as all FET outputs connect to the output pad, the FETs need not be arranged physically or conceptually in pairs, except that at least one of each type must be provided for basic pull up and pull down functions.

The chip 12 is supported by a the chip carrier 14, and a tab or wire bond 124 connects the output pad 20 to a land 126 on the carrier. A multitude of other wire bonds connect other pads to other lands. The lands of the chip carrier are electrically connected to conductive terminals 130 on the printed circuit assembly 10 by conventional soldered connections. A conductive trace 132 extends to a filter component 134 near the PCA periphery, where a connector module 136 is connected to the trace, and to an external component or instrument 140 via a cable 142. The filter is typically a resistor, a resistor/capacitor, or a ferrite bead.

The selectable controls on the effective size of the pad drivers is used to optimize the driver strength for a specific application of the chip. In each application, the driver controls are adjusted to compensate for impedances that occur outside the chip, primarily on the PCA. On the PCA, an adjacent trace 144 near trace 132 may exhibit capacitive and inductive coupling with trace 132, generating unwanted EMI noise on either line in response

to switching on the other. Either trace may also be subject to stray capacitances.

Accordingly, after a prototype system is assembled, these EMI problems may be detected and identified. To cure the EMI problems, an appropriate filter 134 is connected to the trace 132 near the connector, to reduce EMI on the signal expressed at the connector to the external device 140. Typically, such filters slow the switching speed of the pad drivers, and additional transistor size is required to compensate. However, a large transistor size adequate for a heavily filtered trace will generate excessive noise on lines or in other applications of the same chip where filtering was not required. Therefore, the combination of transistors may be selected to provide adequate switching speed. In the design process, filtering and driver control codes may be iterated to optimize the settings.

Normally, after the driver control settings are established for each pad, they remain constant throughout use, avoiding the need for sensors, and reducing the demand on the microprocessor during operation. However, where these are not a concern, the system may include noise sensors on the chip or on the PCA circuitry to provide feedback to the microprocessor to enable it to adjust drive levels during normal operation.

To further reduce noise concerns, the microprocessor may trigger the control gates with pulses that are not simultaneous, but which may provide a stair step turn on of the FETs, or which may be slightly randomized. The control bits may be manipulated by an algorithm of the user's choice.

Alternative embodiment

Figure 2 shows a pad driver circuit 200 on an application-specific integrated circuit (ASIC) chip 202 mounted on a printed circuit assembly (PCA) 204, or mounted on a chip carrier 12 mounted to a PCA. The chip includes a microprocessor controller (not shown) that is interconnected to control all chip functions. An output pad 206 represents one of numerous output pads for expressing a digital signal from the chip to other components on the PCA. A wire bond 210 is symbolically shown to illustrate its inherent function as an inductance element 212, and connects to a load 214 on the PCA. The load has capacitive

characteristics, and is symbolized by a capacitor connected to ground 216. In typical applications the load is a CMOS load with a capacitance of 3-100 pF.

The pad driver circuit 200 has an output line 220 connected to the pad, and a data input line 222 connected to other logic circuitry on the chip. The pad driver circuit receives a switching logic signal from the input line and outputs a powered and conditioned signal that corresponds to the input signal. The output signal provided at the pad has adequate power to drive any connected loads, and is conditioned to avoid excessively rapid rise times and sharp transitions that generate ringing, transmission line effect, and other forms of EMI, as discussed above.

10 The pad driver circuit 200 includes a predriver portion 224 and a main driver portion 226. The predriver portion includes a first predriver 230 and a second predriver 232. The main driver portion includes a first main driver 234 and a second main driver 236. Each predriver includes a transistor pair. Each pair includes a p-channel FET and an n-channel FET, with the p-channel FET source connected to a voltage source Vdd, the n-channel FET source connected to a ground line 240, and the p-FET and n-FET drains connected to each other.

The first predriver 230 includes p-FET 242 and n-FET 244, with their drains connected to a predriver output line 246 extending to main driver 234. The gates of FETs 242 and 244 are connected to a first input line branch 248 that extends to the data input line 222. A pair of inverters 250 are serially connected on the first input line branch, and are selected with parameters to avoid simultaneous operation of both main drivers at signal transitions, which would create an unwanted connection between Vdd and ground. The second predriver 232 includes p-FET 252 and n-FET 254, with their drains connected to a predriver output line 256 extending to main driver 236. The gates of FETs 252 and 254 are connected to a second input line branch 258 that extends to the data input line 222.

In the main driver portion 226, the first main driver 234 is a p-FET 260 with its source connected to Vdd, a gate connected to the first predriver output line 246, and a drain connected to output line 220. The second main driver 236 is an n-FET 262 with its source

connected to ground, a gate connected to the second predriver output line 256, and a drain connected to output line 220.

In the illustrated embodiment, the main drivers are static impedance matched to the expected impedance of the circuitry to which they will be connected. Normally, a standard
 5 impedance (in this case 80Ω) is selected, and used as the standard for designing circuitry and for selecting components in the associated device. In some alternative approaches, a custom impedance may be selected to match a particular associated portion of a particular circuit that departs from a nominal standard impedance. By any type of impedance matching, transmission line effects are reduced or avoided.

10 The predriver FETs are sized to provide a relatively slow turn on period or time constant, as will be discussed below with respect to the circuit operating principles. In particular, the n-channel FET 244 and p-channel FET 252 are critical, because they are involved in the activation of their associated main drivers 234, 236. With a time constant established as discussed below to exceed a threshold set to avoid ringing, the impedance of the predriver
 15 FETs is set based on the expected or measured capacitive characteristics of the associated main driver, as measured between the main driver gate and Vdd (in the case of driver 234) or ground (in the case of driver 236). By using standard circuit modeling techniques such as SPICE, the parameters of device 244 may be iteratively adjusted to arrive at a suitable output time constant.

20 In the illustrated embodiment, predriver impedance values in the range of $2\text{-}20\Omega$ are anticipated to be suitable for use with expected circuit ringing resonances, and with expected main driver parameters (selected to match expected circuit impedances). As CMOS or related manufacturing processes advance, the impedance range may shift.

Figures 3a-3e illustrates several electrical characteristics of a circuit without the features
 25 of the illustrated embodiment (Fig. 3a) and of a circuit according to the illustrated embodiment of Fig. 2, all on a common time domain. Fig. 3a illustrates how external circuitry such as a bond wire and off-chip load may respond with high frequency ringing when a relatively fast output driver is given a data signal transition such as shown in Fig.

3b. The data signal is switched from low (0) to high (1) at time t_1 , and the resulting output voltage V_{data} ideally rises from V_0 on a straight, steep ramp 270 to V_{dd} at time t_1' , and continues flat at V_{dd} until further switched.

However, with attached circuitry causing ringing, the actual voltage 272 fluctuates in response to circuit ringing as it rises past V_{dd} , then damps out over time to V_{dd} . The ringing has a frequency that may be measured experimentally or derived theoretically during circuit modeling or design. A period 274 of one full ringing cycle may be easily calculated, and is illustrated in Fig. 3a. When the output overshoots, rising to peaks 276 significantly above V_{dd} , breakdown may occur. The high signal is valid above a high threshold V_{ht} moderately below V_{dd} . Below a low threshold V_{lt} moderately above V_0 , a signal is read as valid low. Between the low and high thresholds, the signal is read as invalid, such as at invalid ringing minima 280. The negative transition of the signal downward through the high threshold at the beginnings of each such minimum may generate a false trigger. While short-lived ringing may be acceptable for less demanding circuits that can wait an interval before reading the V_{data} level, it is unacceptable in faster circuits that must read the voltage as early as time t_2 .

To reduce or effectively eliminate the harmful ringing caused by the high current of a rapid transition, the predriver is sized to turn on slowly, over an interval at least half the ringing period, and preferably at least as great as a full ringing cycle period, with $1-1/4$ periods shown in Fig. 3c. Figure 3c shows voltage V_{pre} measured at the output of a predriver, which rises from V_{p0} to V_{p1} over a relatively straight slope, over a time interval 282, which in the illustrated case is equal to the ringing period 276 shown in Fig. 3a. As discussed above, the interval is set by setting the predriver resistance to a value that provides an appropriate time constant, also based on the capacitance of the main driver.

Figure 3d shows the ideal output voltage 284 rising on a straight and relatively gentle slope from V_0 to V_{dd} over the time interval t_1-t_2 , and proceeding flat after t_2 . Due to ringing effects, the actual output voltage 286 of the main driver (driven by the predriver voltage of Fig 3c) fluctuates above and below the ideal voltage line at the ringing frequency,

which is damped substantially due to the slower turn on period, but which is not eliminated or changed in frequency. With the turn-on ramp period t_1 - t_2 set at 1-1/4 of the ringing period, the second ringing maximum 286 coincides with the transition to an ideally flat signal, providing a relatively sharp peak. The slight ringing-induced variances are within
 5 tolerated thresholds, and damp relatively quickly due to their small initial amplitude.

As with standard FET devices, the main driver provides a response time that is a function of input voltage. When the input voltage is low, the main driver provides very limited current, resulting in a small slope or edge rate. As the input voltage rises to intermediate levels, the output current increases. Only after the input voltage rises to a maximum level,
 10 or to a threshold minimally below the maximum level, does the output current reach potentially maximum rates. However, as shown, the output voltage has already nearly reached the desired output voltage V_1 when the input voltage V_{pre} has peaked. Thus, any ringing response to this maximum current is mitigated by the averaging effect of any response to earlier smaller current, and will occur after the signal has passed a critical
 15 threshold. This avoids retrograde inflection errors that are most critical only during the rise of the signal.

By delaying the full current phase until after at least one half cycle of the ringing frequency has transpired, the downward inflection that can occur at one half cycle will be mitigated. By delaying the full current phase to a full cycle, further mitigation is provided,
 20 and subsequent ringing is damped. For the most sensitive applications, the turn on phase interval 276 may be increased to the full interval between t_1 and t_2 during which the output is expected to rise. Setting the predriver parameters need only be limited by the speed of the circuit, with the slow predriver and fast main driver combining to provide versatile operation to drive circuits operating at high speeds, and having a wide range of load
 25 requirements.

The resulting effective impedance Z of the main driver is shown in Fig. 3e, which shows the impedance at an infinite level before t_1 , then dropping asymptotically during a first dynamic damping phase between t_1 and t_2 to Z_1 , which is set as discussed above to match

the impedance of the main driver to the external circuitry. Following t_2 , the impedance is statically matched.

While the above is discussed in terms of preferred and alternative embodiments, the invention is not intended to be so limited. For instance, while the graphs of Figs. 3b-3e
5 show a rising signal switching from low to high, the same principles apply to a falling signal.

Claims:

1. A method of designing an application specific integrated circuit (202) for a circuit having a selected circuit portion (212, 214) with an impedance characteristic and a ringing frequency, the method comprising the steps:
 - 5 establishing an output driver size (260, 262) to substantially match the impedance characteristic of the selected circuit portion;
 - determining the capacitance of the output driver;
 - determining a predriver (244) time constant greater than a selected threshold based on the ringing frequency; and
 - 10 establishing a predriver size based on the time constant and the output driver capacitance.
2. A method of designing an application specific integrated circuit according to claim 1 wherein the ringing frequency has a cycle period, and wherein the predriver (244) time constant is at least half of the cycle period.
- 15 3. A method of designing an application specific integrated circuit according to claim 1 or claim 2 wherein the ringing frequency has a cycle period, and wherein the predriver time constant is at least the cycle period.
4. A method of designing an application specific integrated circuit according to any one of claims 1 to 3 wherein determining the circuit ringing frequency includes determining an
20 inductance (212) and capacitance (214) value for the selected circuit portion.
5. A method of designing an application specific integrated circuit according to any one of claims 1 to 4 wherein establishing an output driver impedance includes substantially matching the output driver impedance to an impedance value associated with the selected circuit portion.



6. An application specific integrated circuit (202) for use with a circuit (212, 214) having a selected circuit portion having at least a first electrical characteristic, the integrated circuit comprising:
 - an output pad (206);
 - 5 a first output transistor (260) having a drain connected to the output pad, and a gate (246);
 - a first predriver transistor (244) having a drain connected to the gate of the output transistor;
 - the output transistor having a gate-source capacitance characteristic;
 - 10 the first predriver transistor having a predriver time constant above a selected threshold based on the first electrical characteristic; and
 - the first predriver transistor having a selected resistance based on the predriver time constant and the gate-source capacitance characteristic, such that the first predriver is operable to switch the output transistor at a sufficiently slow rate to avoid ringing.
- 15 7. An application specific integrated circuit according to claim 6 wherein the first electrical characteristic is a ringing frequency based on an inductance (212) and capacitance (214) of the selected circuit portion.
8. An application specific integrated circuit according to claim 6 or claim 7 wherein the first output transistor (260) is sized to provide a selected impedance.
- 20 9. An application specific integrated circuit according to any one of claims 6 to 8 including a second output transistor (262), and wherein the first output transistor is connected to a first voltage potential (V_{dd}), and wherein the second output transistor is connected to a different second voltage potential.
10. An application specific integrated circuit according to any one of claims 6 to 9 wherein
 - 25 only one of the first output transistor (260) and the first predriver transistor (244) is an n-channel device, and the other is a p-channel device.

