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DRAWINGS ATTACHED

982.941

982.941



Date of Application and filing Complete Specification: May 1, 1961.

No. 15722/61.

Application made In United States of America (No. 26136) on May 2, 1960.

Complete Specification Published: Feb. 10, 1965.

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Index at acceptance:—H3 T(1A1, 2T2Z, 2T3J, 2T3X, 3N, 3X, 4A2, 4A3, 4C, 5S); H1 K(1A1, 1C1, 2S1, 2S2, 2S10, 2S20, 4F1)

Int. Cl.:—H 03 f // H 01 I

COMPLETE SPECIFICATION

Improvements in Transistor Amplifiers

5 We, TEXAS INSTRUMENTS INCORPORATED of 13500 N-Central Expressway, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 This invention relates to improvements in transistor amplifier circuits and more particularly to such circuits which feature transistor active elements with high effective input impedances.

15 Semiconductor circuits or networks have heretofore been proposed, illustrative of which are those described in the specification of our copending British Patent Application No. 3633/60 (Serial No. 945,734). According to that application, entire electronic circuits can be fabricated in or on semiconductor wafers wherein various portions of the wafer act as the discrete circuit elements necessary to perform the desired circuit function.

20 Although the subject matter of the above application constitutes a major breakthrough in the art of circuit miniaturization, and although through its practice any of a wide variety of electronic circuits can be formed within a single tiny wafer of semiconductor material, problems have arisen when the frequency characteristics of some of the circuits have been lowered to include the audio range. Thus, for example, when it has been desired to form a complete low frequency amplifier within a tiny wafer of semiconductor material, the input impedance of the amplifier has been so low as to require the inclusion of relatively high-valued capacitors.

40 The problem that low input impedance presents in terms of a requirement for high values of capacitance will be appreciated when it is recognized that frequency response characteristics of an amplifier are in large measure

determined by the ratio of coupling and bypass capacitor reactances to the impedances presented at the electrodes of the amplifier active elements (e.g., transistors). Thus, since the input impedances of bipolar transistors are relatively low, the capacitive reactances required for the associated capacitors must be correspondingly low at the frequencies involved, and this in turn required that in low frequency embodiments the values of the capacitors be relatively high.

55 It is generally recognized that one of the major factors influencing the capacitance presented by a capacitor relates to the effective areas of the capacitor electrodes. Thus, the value of capacitance available in a given design will vary directly as a function of the area thereof; and, although relatively large values of capacitance can be obtained by increasing the size of the semiconductor wafers proposed in the foregoing application, an inordinate increase in such size would tend to offset one of the major advantages thereof, namely, the extremely small size of the semiconductor circuit. Consequently, it has not been found practicable to exceed certain values of capacitance if the full advantage of small size is to be obtained. An object of the present invention is to obviate or mitigate this disadvantage.

75 The present invention is an amplifier circuit comprising a transistor having base, emitter and collector electrodes, a field-effect transistor having its channel ohmically connected between the base and collector electrodes, an input applied to the gate electrode of said field-effect transistor and an output connected to the collector or emitter electrode.

80 The present invention is also an audio amplifier circuit comprising a transistor having collector, base and emitter electrodes, a field-effect transistor having its channel ohmically connected between the collector and base electrodes, a capacitor coupled to the gate electrode of said field-effect transistor for applying an input thereto, an output connected

to the collector electrode and negative feedback means interconnecting the output and said gate electrode.

As will be apparent to one skilled in the art, ohmic connections are those which exhibit symmetry and linearity in terms of resistance to flow of current therethrough in any available direction.

Embodiments of the invention will now be described by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a schematic diagram of an audio amplifier in accordance with the present invention;

Fig. 2 is a schematic diagram of a low pass filter circuit utilizing resistors;

Fig. 3 is a schematic diagram of a low pass filter circuit utilizing field-effect transistors;

Fig. 4a is a perspective view of a semiconductor circuit embodying the present invention;

Fig. 4b is a circuit diagram of Fig. 4a;

Fig. 4c is a perspective view of another semiconductor circuit embodying the present invention;

Fig. 4d is a circuit diagram of Fig. 4c;

Fig. 5a is a perspective view of a still yet another semiconductor circuit embodying the present invention; and

Fig. 5b is a circuit diagram of Fig. 5a.

A feature of this invention is to provide audio amplifier designs compatible with semiconductor circuit technology as taught in the specification of our aforementioned co-pending British Patent Application No. 3633/60 (Serial No. 945,734). Two main problems are encountered in designing audio circuits to be incorporated in a single piece of semiconductor material. The input to a transistor amplifier stage inherently has a low impedance; therefore, a large coupling capacitor, one to ten microfarads, is required to match impedance. It is hard to design a semiconductor circuit that has such a large capacitance because of the large area that would be required. More reasonable capacitor values would be 0.001 to 0.010 microfarads. 0.001 microfarad is a convenient size capacitor to build into a semiconductor circuit. Another problem encountered is the temperature dependence of the semiconductor material parameters, and their effect upon device and circuit performance. This problem manifests itself by instability of the D.C. bias voltages of the amplifier.

The problems dealt with in the preceding paragraph are overcome in the circuit shown in Fig. 1. An input 21 is connected directly to coupling capacitor 14 which connects into the gate 26 of field effect transistor 15. This gate circuit is inherently a high-impedance circuit, and therefore, a small coupling capacitor can be used. The channel of the field effect transistor is defined between the source 30 and the drain 28 of the transistor. The drain 28 is connected to the base of an NPN

transistor 16. The emitter of transistor 16 is connected to ground. The channel circuit of the field effect transistor is inherently a low-impedance circuit, and therefore matches to the low-input impedance of the base of the transistor 16. Load resistor 19 is connected to the collector of transistor 16 and to a supply voltage terminal 23. The source 30 of the field-effect transistor 15 is connected to terminal 27 between the load resistor 19 and transistor 16. The field effect transistor 15, transistor 16 and resistor 19 form a first amplification stage which is similar in operation to a "cathode follower" circuit in that it has an amplification factor of less than unity, high input impedance and low output impedance. The second stage of amplification is also an NPN transistor 18 with its collector connected into a load resistor 20, which is connected to voltage supply terminal 23. The emitter of transistor 18 is grounded. Under normal operating conditions the point 27 will be at a potential of approximately one half that at terminal 23. It is desirable to drive the base of the second amplification stage at approximately six-tenths of a volt. Therefore, some means is required to drop the voltage from point 27 of the first stage to approximately 0.6 volts at the input of the second stage. A device that would regulate the voltage on the input of the second stage at this value and also be satisfactory from an impedance standpoint is a Zener diode. Thus, Zener diode 17 is used to couple point 27 of the first stage to the base of transistor 18, thereby maintaining the input voltage of the second stage at approximately 0.6 volts.

To overcome temperature instability of the d-c bias conditions it is necessary to incorporate some means to stabilize the voltage on the gate of the field-effect transistor 15. This is accomplished by using negative feedback from the output 22 of the second stage to the gate 26 via a low-pass filter 30.

An example of a typical low-pass filter is given in Fig. 2. It consists of two resistors 40 and 41 in series, with a capacitor 42 connected between the two resistors and ground 45. Terminal 43 is connected to the gate 26 of the field-effect transistor 15 and terminal 44 is connected to the output 22 of the second stage. Because of the high-input impedance to the gate of the field-effect transistor 15, reasonably large resistors are necessary in the low-pass filter. These resistors should be in the order of 10⁷ ohms. Another reason for using high values of resistance for resistor 40 and resistor 41 is to allow capacitor 42 to be of relatively low capacitance but still achieve good attenuation of the a-c signal in the feedback loop. This low-pass filter then allows the a.c. to be filtered out to ground 45, blocks the d.c. from passing to ground 45, and allows a negative feedback d.c. voltage to be impressed on the gate 26 of the field effect tran-

sistor 15 to stabilize d.c. bias conditions.

Repeating, the resistors of the low-pass filters must be reasonably large; in the order of 10^7 ohms. First, this is to match the impedance of the gate circuit of the field effect transistor 15 and, secondly, to allow a small capacitor 42 to be used between terminal 46 and ground 45.

It must be noted that large resistors cannot easily be incorporated in a semiconductor circuit and retain the concept of smallness, and the Fig. 2 form of filter would only be used if smallness is not a requirement. A low pass filter using field effect transistors is used in the place of a filter using resistors at least in cases where smallness is a requirement. Fig. 3 shows two field effect transistors 60 and 61 connected in series, and in combination with capacitor 62 to form a low pass filter in accordance with the invention disclosed in our co-pending patent application No. 3123/62 (Serial No. 982,942). The characteristics of the channel of the field effect transistors is such that with a reasonably large gate voltage the field effect device is "pinched off" and the resistance of the channel circuit becomes very high, requiring a large voltage across the channel circuit of the field effect transistor in order to produce an appreciable current. With high enough voltage on the gates of the field effect transistors, the resistance of the channel circuits can be made in the order of 10^7 ohms. In Fig. 3, the source of one transistor 60 and the drain of the other transistor 61 are connected to a common terminal 66. The gates of the transistors are connected together by lead 68 and to a battery 65. These field-effect transistors are in effect used as voltage variable resistors. They lend themselves to semiconductor circuitry as they can be incorporated as high resistances, and allow the use of a small capacitor 62 which may be in the order of 0.001 microfarad. The battery 65 can be replaced by another potential source. For example, lead 68 can be connected to a tap on the load resistance 20 to provide a high enough gate voltage to make the channel portions of the field effect transistors of sufficiently high resistance to be usable in a low pass filter.

A semiconductor circuit in accordance with this invention, is shown in Fig. 4a. Starting with an n-type single crystal silicon substrate 100 (7 to 9 ohm-cm and 3 to 5 mils thick), it is first optically polished on one side. After cleaning, the polished wafer is diffused with gallium from a surface concentration of about 3×10^{15} atoms per cubic centimetre to a depth of approximately 0.1 mils to form a p-type layer 102 which constitutes the channel of a field effect transistor device. The wafer is then given a second diffusion of phosphorus from a surface concentration of about 10^{20} atoms per cubic centimetre to a depth of from about 0.05 to 0.08 mils. By use of oxide masking, this

diffusion is restricted to the area identified by the reference numeral 104. This n-type diffusion produces the gate region of the field effect device. Aluminium can then be evaporated and alloyed to the device as gate, source and drain contacts. It will be appreciated that the unwanted diffused layers on the back and side of the substrate can be removed by lapping. In Fig. 4a, ohmic contacts 106 and 104 constitute the source and gate contacts to the field effect device. The drain contact is not shown for reasons that will appear hereinafter. With the device as described, transconductance of the order of 50 μ mho-per-mil of gate width have been achieved. Also, typical units have been found to have a pinch-off voltage of about 3 volts, and a gate-to-channel breakdown voltage of about 20 volts.

In the foregoing description silicon is noted as the semiconductor material. It should be understood that other semiconductor materials may be employed in the present invention in place of silicon. Thus, such materials as germanium, gallium arsenide, indium antimonide, and other semiconductor materials can be employed. The use of silicon, however, is believed to produce superior results as it lends itself more readily to the fabricating techniques required. This material also has several other advantages that will become more evident as the description of the invention proceeds.

The diffusion operations described above are carried out in a conventional way using suitable temperatures and times as is known in the art. Although the specific illustration given above demonstrating the diffusion steps affords a good understanding of these processes, it will be appreciated that the p-type layer 102 can be produced using any impurity material that will function as required. The diffusion processes are conducted, for example, at an elevated temperature of approximately 1200° C. using an amount of impurity to produce the desired surface concentration. The diffusion time is selected to produce penetration of the impurity atoms and the establishment of a PN diffused junction at the desired depth. Masking is utilized, as is known in the art, during the second diffusion step conducted to introduce the n-type impurity into the P-type diffused layer 102 to define the N-type region 104. The depth of penetration of the n-type impurity atoms to establish a PN junction is controlled to leave a p-type conductivity channel beneath the diffused n-type conductivity region 104 approximately 0.02 mils in thickness. The width of the region 104 is approximately 1 mil. It is, therefore, evident that the channel of the field-effect transistor produced by the technique above is approximately 1 mil in length and approximately 0.02 mils in thickness. In the foregoing, the reference to specific materials, times, and temperatures are merely illustrative and not limitative. In fact, the conductivity types of all

regions can be reversed as is known in the art and it is equally possible to start with a p-type wafer.

5 Fig. 4a shows a unipolar field-effect transistor, a bipolar transistor and a load resistor combined on a single wafer to produce a device having high input impedance. The channel 102 of the unipolar transistor is extended to become base region 112 of the bipolar transistor.

10 The main body of the wafer 100 directly beneath the region 112 constitutes the collector region 121 of the bipolar transistor. There is diffused into the upper surface of the region 112 a suitable n-type impurity to establish a region 120 of n-type conductivity to function as the emitter region of the bipolar transistor. A suitable ohmic contact 122 is made to the surface of the emitter region 120.

15 A lead 124 connects the contact 122 with a tab 126 functioning as the ground connection for the device. The lead 124 is joined to a contact 128 on the tab 126 by any conventional soldering technique as is well known in the art.

20 A signal voltage applied via input tab 114, lead 116 and contact 110 to the gate of the unipolar transistor modulates the base current of the bipolar transistor. The reason why the drain contact has been omitted is now evident. The drain end of the unipolar device is contiguous with the base region 112.

25 The over-all transconductance of the combined device is equal to the product of the g_m of the unipolar region and the h_{oe} of the bipolar region. This circuit is somewhat similar in operation to a "cathode-follower." The bulk resistance of the n-type semiconductor material in the region 130 contiguous to collector region 121 is used as a load resistor. Tab 132 attached to the opposite end of region 130 serves as a load voltage supply connection (B+). Tab 134, connected to the collector region 121, would, ordinarily, be used as an output for this circuit arrangement.

30 Lead 136 connects tab 134 to source contact 106. This circuit has the valuable properties of low distortion, high input impedance and low output impedance.

35 A method of coupling to the input of a bipolar amplifier stage from the collector of a preceding stage is also shown in Figure 4a. Here a Zener diode 140 having the desired breakdown voltage serves as the coupling element. Diode 140 is formed by diffusing an n-type impurity onto p-type diffused base layer 142 of the second bipolar transistor. Once the diode breakdown voltage has been exceeded, it has low incremental resistance, and thus, a high coupling efficiency. Emitter 144 is also formed by diffusing an n-type impurity onto p-type diffused base layer 142. Region 146 of wafer 100 serves as the collector. The bulk resistance of region 148 contiguous to collector region 146 serves as a load resistor

for the second bipolar transistor. Tab 150 attached to collector region 146 serves as an output for the over-all combination of elements.

To complete the circuit interconnections, lead 152 connects tab 126 with emitter region 144, and lead 154 connects tab 134 with Zener diode 140. Due to 100% negative feedback, the voltage amplification of the first stage (left half of crystal) will be approximately unity and its output impedance will be low. The voltage amplification of the second stage (right half of crystal) will be equal to the product of the resistance of region 148 and the transconductance, g_m , of the bipolar transistor (142, 144, 146). Since this stage is being driven from a low impedance source, its voltage amplification will be fairly independent of the h_{oe} of the bipolar transistor (142, 144, 146). Also, it can be shown that if the product of the resistance of region 148 and collector current (I_c) of the bipolar transistor (142, 144, 146), can be held constant, the amplification will not be sensitive to moderate changes in the value of resistance of region 148. If the value of resistance of region 130 is several times the input impedance of the bipolar transistor (142, 144, 146), for example 10K ohms, then moderate changes in its value will have little effect on the amplifier performance. Thus, the tolerance on the values of the resistance of regions 148 and 130 need not be tight.

However, with the circuit as shown, the output transistor (142, 144, 146) will likely not be biased in its active region. A few tenths of a volt variation in the voltage at the collector 121 of the first bipolar transistor will drive the other bipolar transistor either into saturation or cutoff. Even if the second bipolar transistor is biased in its active region, the voltage amplification will be approximately a linear function of the resistance of region 148 and the collector current of the second bipolar transistor. These problems can be greatly reduced by applying a large amount of d-c negative feedback to the amplifier, thus maintaining the bias voltage of the output stage substantially fairly constant. Since the input impedance of the amplifier is high, the resistance of the feedback loop can be large without appreciably reducing the d-c gain of the feedback loop. A low pass filter, as shown in Figs. 2 and 3, can be used. The low pass filter of Fig. 3 is preferred if the entire circuit is to be integrated into a single crystal of silicon. The circuit diagram of the semiconductor circuit of Fig. 4a is shown in Fig. 4b.

The amplifier shown in Fig. 4a may be fabricated with a low-pass R—C feedback network as illustrated in Fig. 2, consisting of two 10 Megohm resistors and a 0.001- μ f capacitor, and a 0.001- μ f input coupling capacitor added as illustrated by capacitor 14, Fig. 1. Thus

70	5
75	10
80	15
85	20
90	25
95	30
100	35
105	40
110	45
115	50
120	55
125	60
130	65

connected, the circuit had a mid-frequency voltage amplification of about 40 db, a band-pass of about 100 to 100,000 cps.

The first stage of the arrangement shown in Fig. 4a, as described, consists of a field-effect transistor in combination with a bipolar transistor having a load resistor in the collector circuit. As shown in Fig. 4c, this same general arrangement can be utilized, but in place of connecting the load resistor in the collector circuit, it can be connected in the emitter circuit. In Fig. 4c, a semiconductor wafer 400, for example of n-type conductivity, is provided, in which the upper surface thereof contains a diffused layer 402 of p-type conductivity. This can be produced in the same manner as was described with reference to Fig. 4a. Also contained in the diffused layer are second and third diffused regions 404 and 406 which are both of n-type conductivity in order to establish the gate of the field-effect transistor and the emitter region of the bipolar transistor. Since the load resistor is to be in the emitter circuit as contrasted with being in the collector circuit, the diffused p-type layer 402 over the remaining portion of the wafer is left intact. A slot 408 is cut adjacent to the bipolar transistor in order to electrically insulate by mechanical shaping the remainder of the p-type diffused layer 402 from that portion which actively is employed in the field-effect transistor and the bipolar transistor. Since the load resistor constituted by the remainder of the p-type region is to be in the emitter circuit, a suitable lead 410 connects the emitter region 406 of the bipolar transistor with one end of the remaining p-type diffused layer identified by reference numeral 412. The opposite end of the remaining p-type diffused layer 412 is connected via a suitable lead 414 to a ground terminal 416. The source end 418 of the unipolar field-effect transistor has connected thereto by an ohmic contact 420, a lead 422 which terminates at a terminal 424 to be connected with a suitable voltage supply. The input to the device is via the gate region 404 of the unipolar transistor by means of a lead 426 attached thereto. A suitable input terminal 428 is provided attached to the opposite end of the lead 426. A suitable output terminal 430 is connected to the lead 410. A suitable contact 432 is made to the collector region of the bipolar transistor, and a lead 434 is attached thereto, for making connection to a voltage supply source. The circuit diagram for the semiconductor circuit of Fig. 4c is shown in Fig. 4d.

The semiconductor circuit combining the features of Fig. 4a and Fig. 3, as previously described, is illustrated in Fig. 5a and 5b. As shown, an input terminal 160 connects with a coupling capacitor 162, which is connected to the gate region of a field-effect coupling transistor generally designated by the reference numeral 164. The construction of

this portion of the device is the same as described in conjunction with Fig. 4a. The channel of the field-effect transistor 164 connects with the base region of a bipolar transistor, generally designated by the reference numeral 166. This arrangement is again the same as illustrated in Fig. 4a. The load resistance for the bipolar transistor 166 is constituted by the bulk resistance of the region of the semiconductor body 168 contiguous with the collector region of the bipolar transistor 166. A suitable lead 170 interconnects the source end of the field-effect transistor 164 with the collector region of the bipolar transistor 166. A suitable voltage supply is attached to the end of the region 168 remote from the bipolar transistor 166. This attachment is indicated generally by the reference numeral 172. At the opposite end of the semiconductor body, there is located a second stage consisting of a bipolar transistor, designated generally by the reference numeral 174. A Zener diode 176 connects with the base region of the transistor 174. A lead 178 connects the other side of the diode 176 with the collector of the transistor 166. Thus far, the description of the semiconductor network is the same as that for Fig. 4a. The method of manufacturing this semiconductor network is the same as previously given, namely, starting with an n-type wafer of silicon into which is diffused a suitable p-type impurity to produce the base regions of the bipolar transistors and the channel of the field-effect transistor. Thereafter, the emitter regions of the bipolar transistors as well as the gate region of the field-effect transistor, are produced by a subsequent diffusion of an n-type impurity. It will be appreciated that in some cases it will be possible to utilize an alloying technique to establish the emitter regions of the bipolar transistors in the p-diffused layer. Conceivably, an alloy technique can be utilized to establish the gate region for the field-effect transistors. Alloy techniques, however, are not the equivalent of diffusion processes for the reason that they are more difficult to control, and less susceptible of reproducible results. The region between the collector of the transistor 174 and the attachment or contact 172 is generally designated by the numeral 180, and functions as the load resistor for the bipolar transistor 174. In this regard, the bulk resistance of the semiconductor body furnishes the load resistance. An output terminal 182 is attached to the collector region of the transistor 174 by means of a lead 184.

Formed on the semiconductor body above the region 180 are two field-effect transistors joined together and in combination with a capacitor 186 for the purpose of providing a low-pass filter between the output of the transistor 174 and the input to the gate of the field-effect transistor 164. The two field-effect transistors are formed by a p-diffused

layer 188 into which has been further diffused two n-type regions 190. Each n-type region defines beneath it the channel for its respective field-effect transistor. The two n-type regions 190 constitute the gates for the field-effect devices, and are connected together by means of a lead 191 and to an intermediate portion of the region 180 by means of lead 192. To stabilize the bias on the gates 190, a Zener diode is formed on the region 180 intermediate the output 182 and supply terminal 172 and connected by lead 199 to the output 182. Lead 193 connects the output lead 184 with one end of the field-effect devices at contact 194. The other end of the field-effect devices at contact 195 is connected by means of lead 196 back to the gate of field-effect transistor 164. The region intermediate the two n-type diffused regions 190 is connected by means of a contact 197 and lead 198 to capacitor 186, the other side of which is grounded. The emitter region of transistor 174 is connected to ground. The emitter region of transistor 166 is also connected to ground. By connected to ground is meant that a suitable terminal or tab is provided to which the emitter regions are connected either by leads or other means for the purpose of grounding these areas. The circuit diagram for the semiconductor circuit shown in Fig. 5a is illustrated in Fig. 5b.

It will be appreciated that the problem of d-c bias stability is overcome to a large extent in this semiconductor circuit by means of the large amount of d-c negative feedback that is furnished from the output lead 184 to the gate of the field-effect transistor 164 via the low pass filter constituted by the field-effect devices located above the region 180 and the capacitor 186. In this connection, the field-effect devices function as voltage-variable resistors and provide resistances in the order of meg-ohms for attenuation, whereas the capacitor 186 functions as an a-c shunt or bypass. Thus, the d.c. is fed back without difficulty, whereas the a-c component of the output signal is shunted out of the feedback loop.

In the semiconductor circuit of Fig. 5a, capacitors 162 and 186 are external of wafer used for the circuit and may be provided in other wafers. It is possible, however, to fabricate these capacitors from the same wafer used for the circuit of Fig. 5a simply by widening the wafer and using the additional space for the fabrication of capacitors 162 and 186. These capacitors can be made either as PN junction types or as oxide types as shown in the specification of our co-pending Patent Application No. 3633/60 (Serial No. 945,734).

By this means, the capacitors can be fabricated at the same time as the semiconductor circuit. After completion, the wafer can be etched through or otherwise divided to separate the circuit and the capacitors. The three semiconductor parts can then be mounted on

a ceramic wafer using tabs and appropriate interconnections.

The present invention therefore advantageously overcomes the problem of obtaining large capacitance values in tiny integrated electronic circuits by advantageously increasing the input impedance of the active elements by several orders of magnitude. Consequently, since the frequency response is largely dependent upon the ratio of input impedance to capacitance (i.e., coupling capacitance, bypass capacitance, etc.), frequency response can be extended many octaves without changing capacitance values. Thus, full advantage may be taken of the remarkable characteristics of the prior art proposals in low frequency embodiments without sacrifice to extreme reduction in size.

Among the other advantages of this invention are that greater versatility is imparted to semiconductor circuits, that the frequency range over which circuits of minimum size can be effectively operated is extended, that the effective input impedance of active elements within integrated electronic circuits is considerably increased, and that the ratios between impedances present at active element electrodes and the reactances presented by associated capacitors are optimized.

WHAT WE CLAIM IS:—

1. An amplifier circuit comprising a transistor having base, emitter and collector electrodes, a field-effect transistor having its channel ohmically connected between the base and collector electrodes, an input applied to the gate electrode of said field-effect transistor and an output connected to the collector or emitter electrode. 95
2. An amplifier circuit according to claim 1, further including a capacitor coupled to said gate electrode for applying said input thereto. 100
3. An amplifier circuit according to claim 1 or 2, wherein said output is connected to said collector electrode, further including a second transistor having collector, base and emitter electrodes, wherein said output is connected to the base of said second transistor. 110
4. An amplifier circuit according to claim 3, further including negative feedback means interconnecting the collector electrode of said second transistor and the gate electrode of said field-effect transistor. 115
5. An amplifier circuit according to claim 4, wherein said negative feedback means includes a low pass filter. 120
6. An amplifier circuit according to claim 3, 4 or 5 wherein the output connection to the base of said second transistor includes a Zener diode. 125
7. An audio amplifier circuit comprising a transistor having collector, base and emitter electrodes, a field-effect transistor having its channel ohmically connected between the collector and base electrodes, a capacitor coupled to the gate electrode of said field-effect tran- 130



layer 188 into which has been further diffused two n-type regions 190. Each n-type region defines beneath it the channel for its respective field-effect transistor. The two n-type regions 190 constitute the gates for the field-effect devices, and are connected together by means of a lead 191 and to an intermediate portion of the region 180 by means of lead 192. To stabilize the bias on the gates 190, a Zener diode is formed on the region 180 intermediate the output 182 and supply terminal 172 and connected by lead 199 to the output 182. Lead 193 connects the output lead 184 with one end of the field-effect devices at contact 194. The other end of the field-effect devices at contact 195 is connected by means of lead 196 back to the gate of field-effect transistor 164. The region intermediate the two n-type diffused regions 190 is connected by means of a contact 197 and lead 198 to capacitor 186, the other side of which is grounded. The emitter region of transistor 174 is connected to ground. The emitter region of transistor 166 is also connected to ground. By connected to ground is meant that a suitable terminal or tab is provided to which the emitter regions are connected either by leads or other means for the purpose of grounding these areas. The circuit diagram for the semiconductor circuit shown in Fig. 5a is illustrated in Fig. 5b.

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In the semiconductor circuit of Fig. 5a, capacitors 162 and 186 are external of wafer used for the circuit and may be provided in other wafers. It is possible, however, to fabricate these capacitors from the same wafer used for the circuit of Fig. 5a simply by widening the wafer and using the additional space for the fabrication of capacitors 162 and 186. These capacitors can be made either as PN junction types or as oxide types as shown in the specification of our co-pending Patent Application No. 3633/60 (Serial No. 945,734).

By this means, the capacitors can be fabricated at the same time as the semiconductor circuit. After completion, the wafer can be etched through or otherwise divided to separate the circuit and the capacitors. The three semiconductor parts can then be mounted on

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Among the other advantages of this invention are that greater versatility is imparted to semiconductor circuits, that the frequency range over which circuits of minimum size can be effectively operated is extended, that the effective input impedance of active elements within integrated electronic circuits is considerably increased, and that the ratios between impedances present at active element electrodes and the reactances presented by associated capacitors are optimized.

WHAT WE CLAIM IS:—

1. An amplifier circuit comprising a transistor having base, emitter and collector electrodes, a field-effect transistor having its channel ohmically connected between the base and collector electrodes, an input applied to the gate electrode of said field-effect transistor and an output connected to the collector or emitter electrode.
2. An amplifier circuit according to claim 1, further including a capacitor coupled to said gate electrode for applying said input thereto.
3. An amplifier circuit according to claim 1 or 2, wherein said output is connected to said collector electrode, further including a second transistor having collector, base and emitter electrodes, wherein said output is connected to the base of said second transistor.
4. An amplifier circuit according to claim 3, further including negative feedback means interconnecting the collector electrode of said second transistor and the gate electrode of said field-effect transistor.
5. An amplifier circuit according to claim 4, wherein said negative feedback means includes a low pass filter.
6. An amplifier circuit according to claim 3, 4 or 5 wherein the output connection to the base of said second transistor includes a Zener diode.
7. An audio amplifier circuit comprising a transistor having collector, base and emitter electrodes, a field-effect transistor having its channel ohmically connected between the collector and base electrodes, a capacitor coupled to the gate electrode of said field-effect tran-

sistor for applying an input thereto, an output connected to the collector electrode and negative feedback means interconnecting the output and said gate electrode.

- 5 8. An amplifier circuit according to any preceding claim, comprising a semiconductor wafer having therein or thereon the gate electrode, the collector base junction and the base-emitter junction of said transistor all adjacent one and the same major wafer face.

- 10 9. An amplifier circuit according to claim 8 and claim 3, 4, 5 or 6, wherein said wafer includes the collector-base junction and the base-emitter junction of said second transistor adjacent said one major wafer face.

- 15 10. An amplifier circuit according to claim 8 or 9, wherein said wafer includes a diffused layer having a conductivity type opposite to that of the semiconductor material underlying it, wherein one region of said diffused layer functions as the channel of said field-effect transistor and a contiguous region of said diffused layer functions as the base of said transistor.

11. An amplifier circuit according to any of claims 8 to 10, wherein said wafer includes one or more elongated portions thereof defining one or more resistors, each elongated portion lying on said one major wafer face and being electrically connected in the circuit.

12. An amplifier circuit according to any preceding claim including a plurality of additional field-effect transistors having their channels connected in series and their gates reverse biased and being electrically connected in the circuit.

13. An amplifier circuit substantially as hereinbefore described with reference to Fig. 1, 4b, 4d or 5b of the accompanying drawings.

14. An amplifier circuit substantially as hereinbefore described with reference to Figs. 4a and 4b, 4c and 4d or 5a and 5b of the accompanying drawings.

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Leamington Spa: Printed for Her Majesty's Stationery Office, by the Courier Press (Leamington) Ltd.—1965. Published by The Patent Office, 25 Southampton Buildings, London, W.C.2, from which copies may be obtained.

