ABSTRACT

A semiconductor memory device includes a semiconductor substrate; a device isolation layer defining an active portion in the semiconductor substrate; a bit line structure intersecting the active portion on the semiconductor substrate; a first conductive pad between the bit line structure and the active portion; a bit line contact pattern between the first conductive pad and the bit line structure; a first bit line contact spacer covering a first sidewall of the first conductive pad; and a second bit line contact spacer covering a second sidewall of the first conductive pad, wherein the first conductive pad has a flat bottom surface that is in contact with a top surface of the active portion, and a width of the first bit line contact spacer is different from a width of the second bit line contact spacer.

FIG. 2A