

**PROCESSOR THAT INDICATES SYSTEM BUS OWNERSHIP IN AN
UPGRADABLE MULTIPROCESSOR COMPUTER SYSTEM**

BACKGROUND OF THE INVENTION

5 1. **FIELD OF THE INVENTION:**

The present invention pertains to the field of computer systems. More particularly, this invention relates to a processor for an upgradable multiprocessor computer system that provides an external indication of system bus ownership.

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2. **BACKGROUND:**

Prior conventional computer systems typically include a single central processing unit. Typically, such a central processing unit is coupled to a system bus that provides communication to a variety of input/output
15 devices. In such a computer system, the central processing unit typically fetches an instruction stream from a memory subsystem over the system bus and executes each instruction in the instruction stream. Such a central processing unit typically maintains a set of data structures in the memory subsystem and performs input/output accesses to the input/output
20 devices over the system bus.

Such a prior single processor system usually implements an interrupt mechanism for handling external hardware exceptions in the system. For example, an input/output device controller in such a system
25 typically causes a system interrupt to the central processing unit if an

access is attempted to an input/output device that is in a powered down or a suspended state. The system interrupt indicates to the central processing unit that the input/output device requires exception handling. Typically, the system interrupt directs control of the central processing unit to an
5 interrupt routine that restores power to the powered down or suspended input/output device. Thereafter, the central processing unit reissues the input/output access to the input/output device and continues normal execution.

10 Other prior computer systems may provide multiple central processing units to improve instruction execution performance. Each central processing unit in such a system is typically coupled to a system bus that provides communication to a memory subsystem and a set of input/output devices. Such a multiprocessor system usually yields
15 improved instruction execution performance in comparison to a system having a single central processing unit because the instruction execution functions are shared among multiple central processing units.

Such a multiprocessor computer system typically provides
20 mechanisms for sharing the external memory subsystem and the input/output devices coupled to the system bus among the multiple central processing units. For example, such a prior multiprocessor system usually implements a bus arbitration mechanism that enables each central processing unit to request and obtain access to the system bus.

Such a prior multiprocessor system also usually implements an interrupt mechanism for handling hardware exceptions in the system. In such a multiprocessor system, an access over the system bus that causes an exception may originate from any of the multiple central processing units coupled to the system bus. An input/output device controller in such a system typically directs a system interrupt to the central processing unit that originated the access that caused the exception.

Typically, an input/output device controller in such a system monitors the system bus and records ownership changes of the system bus between the multiple central processing units. Such an input/output device controller accordingly directs the system interrupt to the central processing unit that owned the system bus during the access that caused the exception. Unfortunately, such a prior system requires the implementation of relatively complex external hardware in the input/output device controller to monitor system bus ownership. Such complex hardware mechanisms usually increase the cost of such prior computer systems.

In addition, such mechanisms are impractical for a computer system that is upgradable from a single processor system to a multiple processor system. In such an upgradable system, a hardware mechanism for monitoring bus ownership and directing system interrupts would not be used if only one central processing unit is installed in the system.

Moreover, the addition of such hardware to the system during upgrade would require extensive hardware modification to the system.

SUMMARY AND OBJECTS OF THE INVENTION

One object of the present invention is to provide an indication of system bus ownership in an upgradable multiprocessor computer system.

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Another object of the present invention is to indicate bus ownership between an OEM processor and an upgrade processor in an upgradable computer system.

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Another object of the present invention is to provide a processor with an upgrade/OEM output pin that indicates bus ownership between an OEM processor and an upgrade processor in an upgradable computer system.

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A further object of the present invention is provide a system wherein the OEM processor is determined by a type input pin of the processor, and wherein the OEM processor drives the upgrade/OEM signal over the system bus.

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These and other objects of the invention are provided by a computer system comprising a processor having a type input pin that indicates whether the processor is coupled as an OEM processor a single processor or a dual processor computer system or as an upgrade processor in the dual processor computer system. The processor includes an

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upgrade/OEM output pin coupled to transfer an upgrade/OEM signal over

a system bus if the type input pin indicates the OEM processor. The upgrade/OEM signal indicates whether the OEM processor or the upgrade processor is a bus owner of the system bus.

- 5 The computer system further comprises a device controller coupled to sample the upgrade/OEM signal to determine whether the OEM processor or the upgrade processor is the bus owner of the system bus. The device controller is coupled to transfer an interrupt to the OEM processor if the upgrade/OEM signal indicates that the OEM processor is the bus
- 10 owner of the system bus during an access over the system bus that causes an exception. The device controller is coupled to transfer an interrupt to the upgrade processor if the upgrade/OEM signal indicates that the upgrade processor is the bus owner of the system bus during the access over the system bus that causes the exception.

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Other objects, features and advantages of the present invention will be apparent from the accompanying drawings, and from the detailed description that follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings in which like
5 references indicate similar elements, and in which:

Figure 1 illustrates a computer system for one embodiment which comprises a pair of processors, a memory subsystem, a display device, a disk subsystem, and a device power control circuit;

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Figure 2 illustrates a processor for one embodiment which comprises a processor core, an interrupt control circuit, a dual processor control circuit, a bus interface circuit, and a cache memory;

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Figure 3 shows a timing diagram that illustrates a pair of pipelined communication transactions over the system bus by the OEM and upgrade processors for one embodiment;

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Figure 4 shows a flow diagram that illustrates the processing of an input/output access over the system bus by the device power control circuit for one embodiment.

DETAILED DESCRIPTION

Figure 1 illustrates a computer system 100 for one embodiment. The computer system 100 comprises a pair of processors 10 and 12, a memory subsystem 14, a display device 18, a disk subsystem 19, and a device power control circuit 20. The input/output devices of the computer system 100 comprise the memory subsystem 14, the display device 18, and the disk subsystem 19. The processors 10 and 12 communicate with the input/output devices of the computer system 100 over a system bus 16.

The device power control circuit 20 provides a set of power mode functions for the display device 18 and the disk subsystem 19. The device power control circuit 20 selects a power on state, a power off state, and a set of sleep mode states for the display device 18 and the disk subsystem 19 via a set of power control signals 25.

The device power control circuit 20 monitors accesses to the display device 18 and the disk subsystem 19 over the system bus 16. The accesses to the display device 18 and the disk subsystem 19 may originate from either the processor 10 or the processor 12. The device power control circuit 20 sets the disk subsystem 19 to a power off or a sleep mode state if an input/output access to the disk subsystem 19 is not detected for a predetermined time interval. The device power control circuit 20 powers down the disk subsystem 19 in order to reduce electrical current demands

on a battery (not shown) for the computer system 100. The device power control circuit 20 performs a similar function for the display device 18.

The processor 10 is substantially similar to the processor 12. The
5 processors 10 and 12 each function in either an original equipment
manufacture (OEM) processor mode or an upgrade processor mode. The
OEM or upgrade processor mode for each processor 10 and 12 is
determined by a voltage input at a corresponding CPU_TYPE pin. A low
voltage on a CPU_TYPE pin 22 of the processor 10 causes the processor 10
10 to function in the OEM processor mode. A high voltage level on a
CPU_TYPE pin 24 of the processor 12 causes the processor 12 to function in
the upgrade processor mode.

The processors 10 and 12 each contain an internal interrupt
15 controller. The internal interrupt controllers in the processors 10 and 12
communicate receive external interrupt requests via an interrupt portion
of the system bus 16. The external interrupt requests to the processors 10
and 12 include system management interrupts (SMIs). The device power
control circuit 20 issues a system management interrupt over the interrupt
20 portion of the system bus 16 to indicate that a device timeout has occurred
during an access by the processor 10 or the processor 12 to an input/output
device in a powered off or sleep mode state.

The processors 10 and 12 each contain an internal bus interface
25 circuit that enables communication over the system bus 16. The internal

bus interface circuits in the processors 10 and 12 implement a bus arbitration mechanism for coordinating ownership of the system bus 16. The arbitration mechanism enables each of the processors 10 and 12 to request ownership of the system bus to obtain ownership over the system bus and to thereafter relinquish control of the system bus 16.

The OEM processor 10 drives an upgrade/OEM signal over the system bus 16. The upgrade/OEM signal indicates whether the OEM processor 10 or the upgrade processor 12 is the current bus master of the system bus 16. For one embodiment, the upgrade/OEM signal on the system bus 16 is always driven by the OEM processor 10 as determined by the CPU_TYPE pin 22.

The device power control circuit 20 monitors the system bus 16 and detects input/output cycles on the system bus 16 that are targeted for the display device 18 or the disk subsystem 19. The device power control circuit 20 detects a bus time-out condition on the system bus 16 for an access to a device in a powered down or sleep mode state. The bus time-out condition is indicated if the addressed input/output device for an access does not return a ready signal over the system bus 16 within a predetermined time interval.

If a bus time-out to the display device 18 or the disk subsystem 19 is detected, then the device power control circuit 20 senses the state of the upgrade/OEM signal on the system bus 16 to determine whether the OEM

processor 10 or the upgrade processor 12 initiated the input/output access that caused the bus time-out. The device power control circuit 20 accordingly directs the system management interrupt to the internal interrupt controller of the OEM processor 10 or to the internal interrupt
5 controller of the upgrade processor 12. The OEM processor 10 or the upgrade processor 12 then executes a system management mode interrupt routine to restore the addressed input/output device to an appropriate state for subsequent access.

10 **Figure 2** illustrates the processor 10 for one embodiment. The processor 10 comprises a processor core 40, an interrupt control circuit 42, a dual processor control circuit 44, a bus interface circuit 46, and a cache memory 50. The processor 12 is substantially similar to the processor 10.

15 The processor core 40 comprises a set of instruction fetch circuitry and instruction decode circuitry for fetching instructions over the system bus 16 and for decoding the fetched instructions. The processor core 40 further comprises a set of execution units for executing the fetched
20 instructions. For one embodiment, the processor core 40 fetches and executes instructions over the system bus 16 according to the Intel Microprocessor Architecture.

 The processor 10 functions in either the OEM processor mode or the upgrade processor mode according to the state of the CPU_TYPE pin 22.
25 The dual processor control circuit 44 samples the state of the CPU_TYPE

pin 22 upon assertion of a reset (RESET) signal on the system bus 16. The dual processor control circuit 44 then sets the processor 10 into the OEM processor mode because the CPU_TYPE pin 22 is at a low voltage level.

- 5 In a similar manner, a dual processor control circuit in the processor 12 samples a high voltage state on the CPU_TYPE pin 24 and accordingly sets the processor 12 into the upgrade processor mode.

 The interrupt control circuit 42 is coupled to a set of interrupt
10 control lines of the system bus 16. The interrupt control lines of the system bus 16 include a programmable interrupt controller clock (PIC_CLK) signal, a pair of programmable interrupt controller data (PIC_DATA_0 and PIC_DATA_1) signals, and a system management interrupt active (SMI_ACTIVE) signal.

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 The interrupt control circuit 42 receives interrupt messages over the system bus 16 that indicate external hardware interrupts in the computer system 100. The external interrupts on the system bus 16 are targeted for either the processor 10 or the processor 12 according to a programmable
20 interrupt controller identifier transferred over the PIC_DATA_0 and PIC_DATA_1 signals. The processor 10 and the processor 12 each maintain a unique internal programmable interrupt identifier that enables external hardware to target an interrupt message to either the processor 10 or the processor 12. System management interrupts are

directed to the processors 10 and 12 via corresponding system management interrupt (SMI) pins.

The bus interface circuit 46 enables communication transactions for the processor 10 over the system bus 16. The processor 10 arbitrates for control of the system bus 16 with the processor 12 via a set of request (REQUEST) and grant (GRANT) signal lines on the system bus 16. The bus interface circuit 46 uses the request and grant signal lines on the system bus 16 to obtain control over the system bus 16 as a bus master and to relinquish control over the system bus 16 to the processor 12.

The bus interface circuit 46 is coupled to a set of address (ADDRESS) signal lines, and a set of data (DATA) signal lines on the system bus 16. The address and data signal lines of the system bus 16 enable the processor 10 to perform memory accesses and input/output accesses over the system bus 16 as well as instruction fetch cycles over the system bus 16.

The bus interface circuit 46 is also coupled to a set of byte enable (BE[0:3]) signal lines on the system bus 16. The byte enable lines indicate the valid data bytes transferred over the data signal lines of the system bus 16.

In addition, the byte enable signal lines of the system bus 16 provide a programmable interrupt controller identifier (PIC_ID) for the processors 10 and 12 during reset of the computer system 100. The bus interface

circuit 46 latches the PIC_ID from the byte enable signal lines as the reset signal is asserted on the system bus 16. The PIC_ID is driven onto the byte enable signal lines of the system bus 16 at reset by the device power control circuit 20.

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The processor 10 in the OEM processor mode uses the PIC_ID sampled on the byte enable signal lines at reset as the unique internal programmable interrupt identifier for the interrupt control circuit 42.

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A bus interface circuit in the processor 12 in the upgrade processor mode determines a programmable interrupt identifier for the internal interrupt controller of the processor 12 by sampling the byte enable signals of the system bus 16 at reset and by inverting the least significant bit of the sampled PIC_ID from the byte enable signal lines. The upgrade processor 12 inverts the least significant bit of the PIC_ID to ensure that the OEM processor 10 and the upgrade processor 12 use different programmable interrupt controller identifiers to determine the proper target for interrupt messages transferred over the system bus 16 via the PIC_DATA_0,1 signals.

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The device power control circuit 20 stores the programmable interrupt identifier for the OEM processor 10 and the upgrade processor 12 which differ only in the least significant bit. The differing programmable interrupt identifiers PIC_ID enable the device power control circuit 20 to properly direct a system management interrupt to either the OEM

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processor 10 or the upgrade processor 12 over the system bus 16.

Alternatively, the device power control circuit 20 directs system management interrupts via separate SMI input signals to the SMI pins of the processors 10 and 12.

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The bus interface circuit 46 is coupled to a clock (CLOCK) signal line for the system bus 16 as well as an address strobe (ADDRESS_STROBE) signal line, a next address (NEXT_ADDRESS) signal line and a cache enable (CACHE_ENABLE) signal line of the system bus 16. The address
10 strobe signal indicates that a valid address is driven over the address lines of the system bus 16. The next address signal indicates whether a new address cycle is allowed on the system bus 16 and the cache enable signal line indicates whether the current data transfer cycle on the system bus 16 is cacheable to the cache memory 50.

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The bus interface circuit 46 is also coupled to a WRITE/READ signal line, a WRITEBACK/WRITETHRU signal line, and a BURST_READY signal line of the system bus 16. The WRITE/READ signal of the system
bus 16 indicates whether current cycle on the system bus 16 is a write or a
20 read cycle. The WRITEBACK/WRITETHRU signal line on the system bus 16 indicates whether the current cache line transferred over the system bus 16 causes a cache line state transition to an exclusive or a shared state.

The bus interface circuit 46 always drives the UPGRADE/OEM
25 signal line of the system bus 16. The bus interface circuit 46 drives the

UPGRADE/OEM signal line to indicate whether the OEM processor 10 or the UPGRADE processor 12 is the current owner of the system bus 16 according to the bus arbitration performed via the REQUEST and the GRANT signal lines of the system bus 16.

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The UPGRADE/OEM signal in conjunction with the SMI_ACTIVE signal indicates whether the processor 10 or whether the processor 12 is in a system management mode (SMM) for power management functions in the computer system 100. The SMM indication provided by the
10 UPGRADE/OEM and SMI_ACTIVE signals is useful for hardware and software debugging in the computer system 100.

Figure 3 is a timing diagram that illustrates a pair of pipelined communication transactions over the system bus 16 by the processors 10
15 and 12 for one embodiment.

The ADDRESS_STROBE signal line of the system bus 16 is driven by either the processor 10 or the processor 12 according to the current bus ownership of the system bus 16. The WRITE/READ signal line of the
20 system bus 16 as well as the address, data, and byte enable signal lines of the system bus 16 are driven by either the OEM processor 10 or the upgrade processor 12 according to the current bus ownership of the system bus 16.

The CLOCK signal line of the system bus 16 is driven by external
25 hardware in the computer system 100. The NEXT_ADDRESS, the

CACHE_ENABLE, the WRITEBACK/WRITETHRU, and the BURST_READY signal lines are driven by devices coupled to the system bus 16 according to the type of communication transaction underway.

- 5 The UPGRADE/OEM signal line on the system bus 16 is always driven by the OEM processor 10. The UPGRADE/OEM signal line does not change ownership according to changes in bus ownership of the system bus 16 between the processors 10 and 12.

- 10 At time t2, the OEM processor 10 asserts the ADDRESS_STROBE signal to indicate a valid address on the address lines of the system bus 16 for a data transfer cycle initiated by the OEM processor 10. At time t5, the upgrade processor 12 asserts the ADDRESS_STROBE signal on the system bus 16 to indicate a valid address on the address lines of the system bus 16
15 for a data transfer cycle initiated by the upgrade processor 12.

- Between times t3 and t4 the UPGRADE_OEM signal transitions from a high to low state to indicate that the OEM processor 10 is bus master during the data transfer sequence that occurs between times t6 and
20 t10 as indicated by the BURST_READY signal line.

 The device power control circuit 20 senses the state of the UPGRADE_OEM signal line on the system bus 16 to determine whether the processor 10 or the processor 12 originated the data transfer cycle

between times t6 and t10 to the addressed input/output device indicated by the address signal lines of the system bus 16 during time t2.

If the addressed input/output device, either the display device 18 or the disk subsystem 19, is in a powered down or sleep mode state, then the device power control circuit 20 samples the UPGRADE/OEM signal line to determine whether to direct a system management interrupt to either the OEM processor 10 or the upgrade processor 12. The device power control circuit 20 accordingly selects the appropriate PIC_ID for the processor 10 or 12 and transfers a system management interrupt message via the PIC_DATA signal lines of the system bus 16 with the selected PIC_ID. Alternatively, the device power control circuit 20 accordingly selects either the SMI input to the processor 10 or the SMI input to the processor 12 to direct the system management interrupt.

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Figure 4 is a flow diagram that illustrates the processing of an input/output access over the system bus 16 by the device power control circuit 20 for one embodiment. At block 70, the device power control circuit 20 senses an access over the system bus 16 to one of the input/output devices including the display device 18 and the disk subsystem 19.

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Thereafter at decision block 72, if a device time-out does not occur to the addressed input/output device then the transaction over the system bus continues as normal. If a device time-out to the addressed

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input/output device does occur at decision block 72, then control proceeds to decision block 74.

At decision block 74, the device power control circuit 20 determines
5 whether the UPGRADE/OEM signal on the system bus 16 is asserted. If the UPGRADE/OEM signal is asserted at decision block 74, then control proceeds to block 78.

At block 78, the device power control circuit 20 issues a system
10 management interrupt to the upgrade processor 12. The device power control circuit 20 identifies the upgrade processor 12 as the target for the system management interrupt by transferring the PIC_ID corresponding to the upgrade processor 12 over the PIC_DATA lines during the system management interrupt message.

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If the UPGRADE/OEM signal is not asserted at decision block 74, then control proceeds to block 76. At block 76, the device power control circuit 20 issues a system management interrupt to the OEM processor 10. The device power control circuit 20 identifies the OEM processor 10 as a
20 target for the system management interrupt by transferring the PIC_ID corresponding to the OEM processor 10 over the PIC_DATA lines during the interrupt message.

The UPGRADE/OEM signal can also direct the BURST_READY signal to either the processor 10 or 12 as appropriate in a system having separate BURST_READY inputs to the processors 10 and 12.

- 5 In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are
- 10 accordingly to be regarded as illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

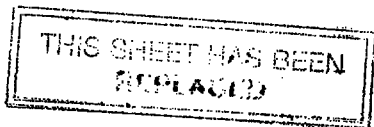


1. A computer system comprising a processor having a type input pin
5 that indicates whether the processor is coupled as an OEM processor in a
single processor or a dual processor computer system or as an upgrade
processor in the dual processor computer system, the processor having an
upgrade/OEM output pin coupled to transfer an upgrade/OEM signal over
a system bus if the type input pin indicates the OEM processor, the
10 upgrade/OEM signal indicating whether the OEM processor or the
upgrade processor is a bus owner of the system bus.
2. The computer system of claim 1, wherein the processor comprises a
bus interface circuit coupled to sample an interrupt identifier on a set of
15 signal lines, the bus interface circuit inverting a least significant bit of the
interrupt identifier if the type input pin indicates that the processor is the
upgrade processor.
3. The computer system of claim 2, wherein the signal lines comprise
20 a set of byte enable signal lines of a system bus that are sampled on a low to
high transition of a reset pin of the processor.
4. The computer system of claim 2, further comprising a device
controller coupled to transfer the interrupt identifier over the signal lines.

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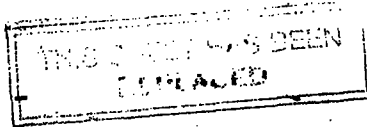
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5. The computer system of claim 4, wherein the device controller samples the upgrade/OEM signal to determine whether the OEM processor or the upgrade processor is the bus owner of the system bus.
- 5 6. The computer system of claim 5, wherein the device controller is coupled to transfer an interrupt to the OEM processor if the upgrade/OEM signal indicates that the OEM processor is the bus owner of the system bus during an access over the system bus that requires the interrupt.
- 10 7. The computer system of claim 5, wherein the device controller is coupled to transfer an interrupt to the upgrade processor if the upgrade/OEM signal indicates that the upgrade processor is the bus owner of the system bus during an access over the system bus that requires the interrupt.
- 15 8. A method for indicating bus ownership in an upgradable multiprocessor computer system, comprising the steps of:
- 20 sampling a type input pin that indicates an OEM processor in a single processor or a dual processor computer system or an upgrade processor in the dual processor computer system;
- transferring an upgrade/OEM signal over a system bus if the type input pin indicates the OEM processor, the upgrade/OEM signal indicating whether the OEM processor or the upgrade processor is a bus owner of the system bus.





9. The method of claim 8, further comprising the steps of sampling an interrupt identifier on a set of signal lines, and inverting a least significant bit of the interrupt identifier if the type input pin indicates the upgrade processor.

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10. The method of claim 9, wherein the signal lines comprise a set of byte enable signal lines of a system bus that are sampled on a low to high transition of a reset pin.

10 11. The method of claim 9, wherein the interrupt identifier is transferred over the signal lines by a device controller in the computer system.

12. The method of claim 11, further comprising the step of sampling
15 the upgrade/OEM signal to determine whether the OEM processor or the upgrade processor is the bus owner of the system bus.

13. The method of claim 12, further comprising the step of transferring
an interrupt to the OEM processor if the upgrade/OEM signal indicates
20 that the OEM processor is the bus owner of the system bus during an access over the system bus that requires the interrupt.

14. The method of claim 12, further comprising the step of transferring an interrupt to the upgrade processor if the upgrade/OEM signal indicates

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that the upgrade processor is the bus owner of the system bus during an access over the system bus that requires the interrupt.

