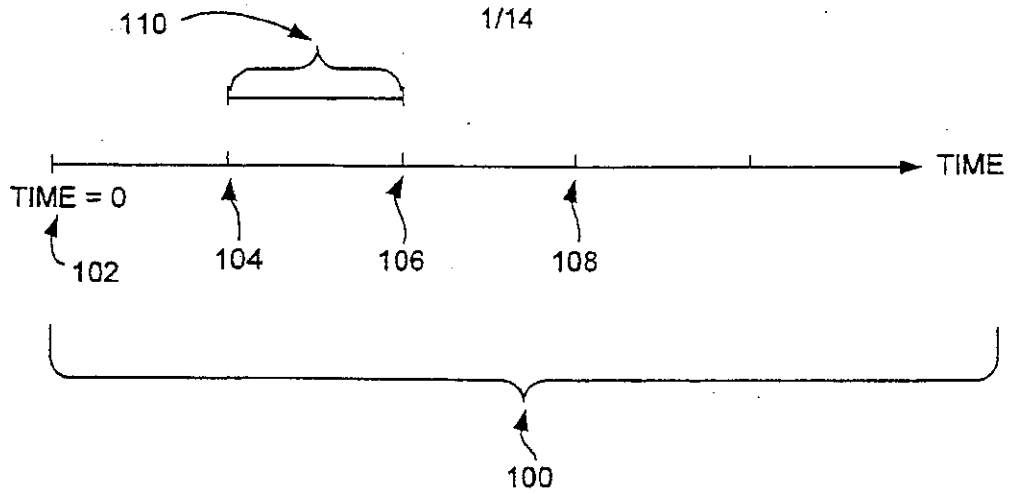

110
TIME
TIME = 0
102
104
106
108
100

FIG. 1

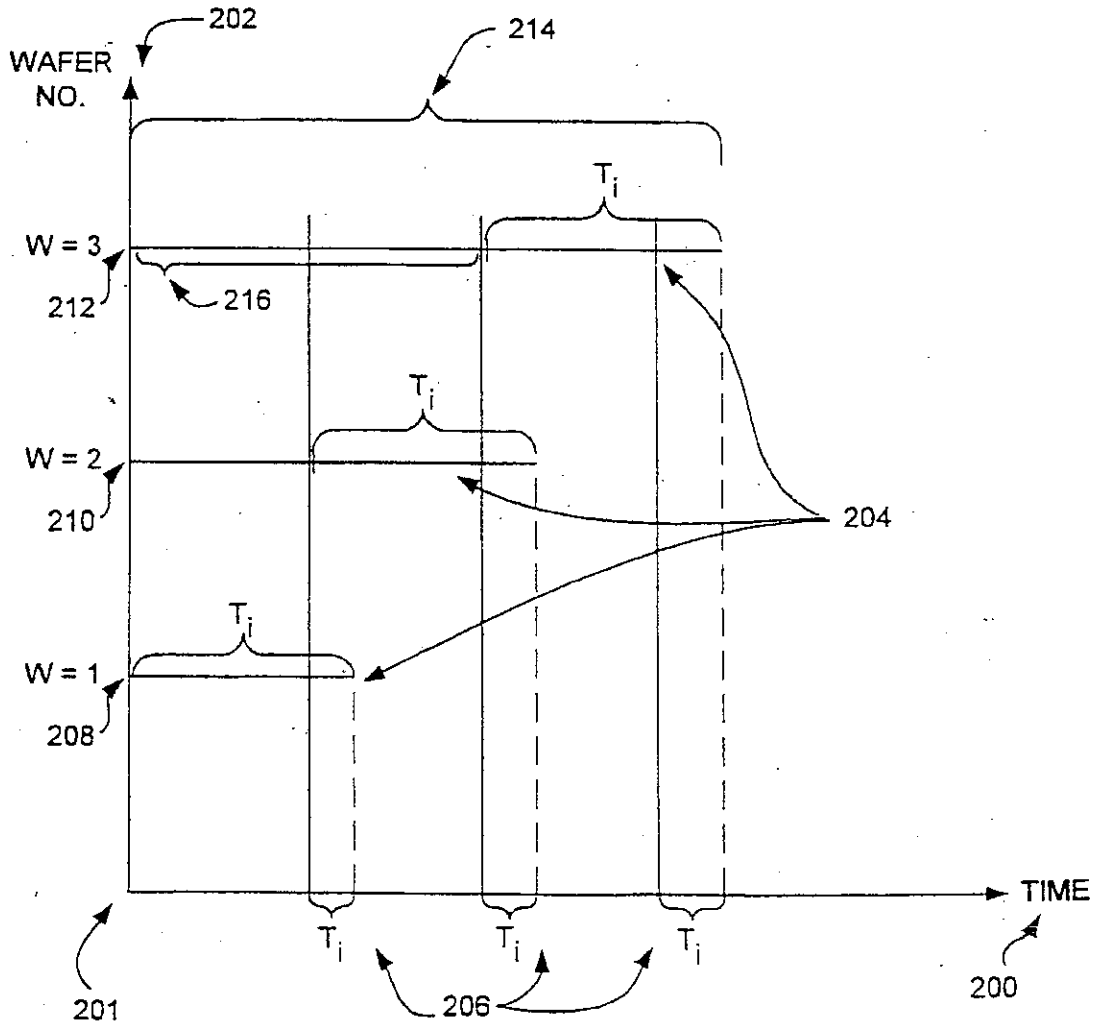

202
214
WAFER NO.
T_i
W = 3
212
216
W = 2
210
204
W = 1
208
TIME
201
206
200

FIG. 2

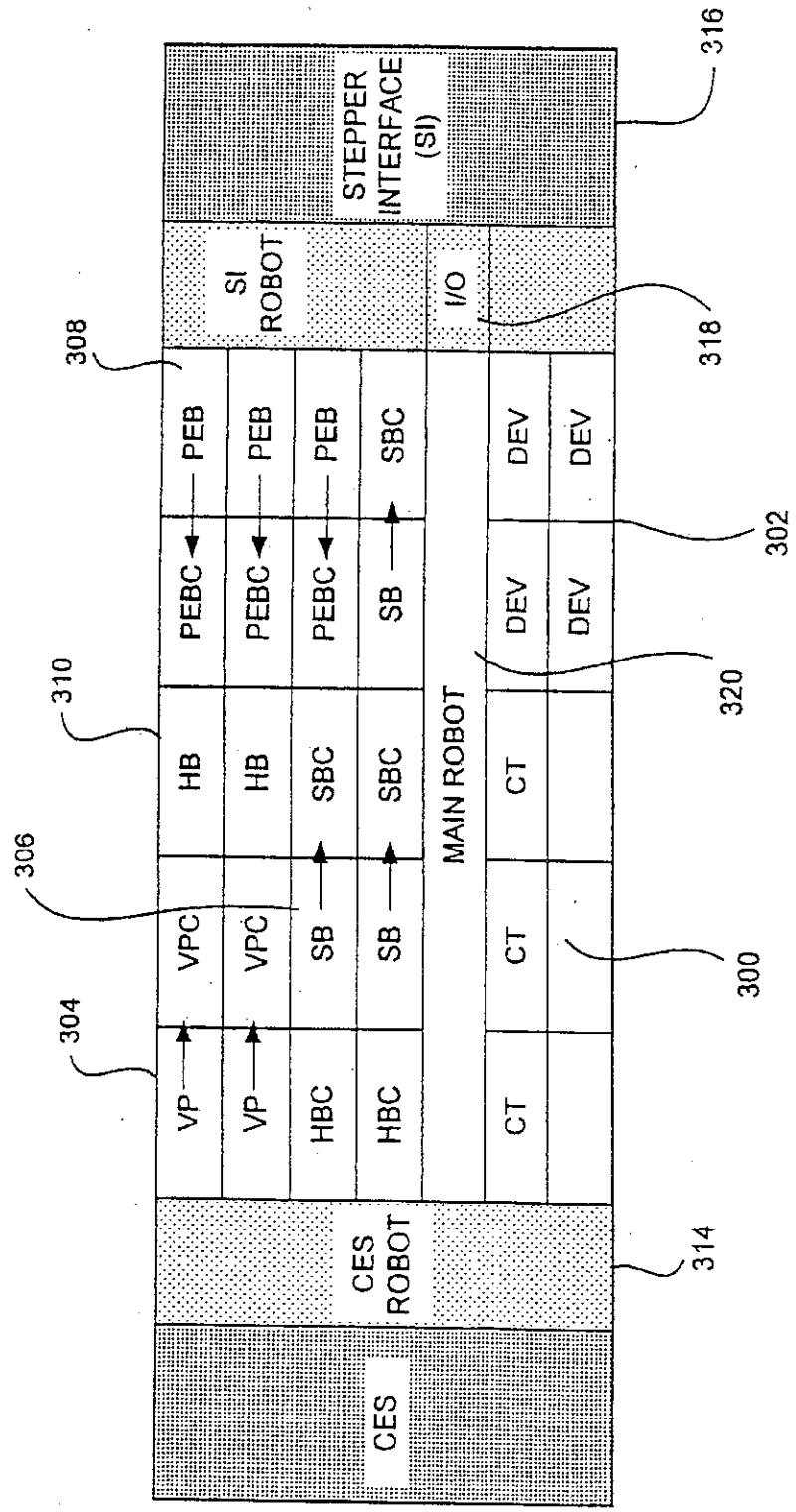
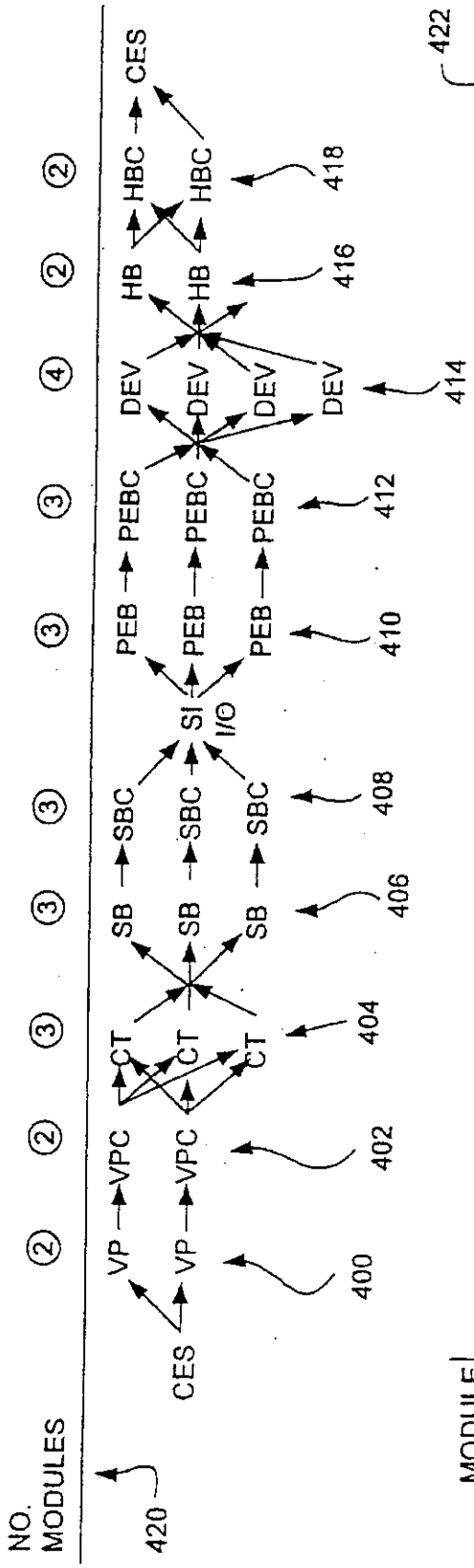

STEPPER INTERFACE (SI)
316
SI ROBOT
I/O
318
308
PEB
PEB
PEB
SBC
DEV
DEV
302
PEBC
PEBC
PEBC
SB
DEV
DEV
310
HB
HB
SBC
SBC
CT
320
306
VPC
VPC
SB
SB
MAIN ROBOT
CT
300
304
VP
VP
HBC
HBC
CT
CES ROBOT
314
CES
KEY: THE ARROWS → REPRESENT IBTAs
312

FIG. 3



422

MODULE PATH	VP	VPC	CT	SB	SBC	PEB	PEBC	DEV	HB	HBC
①	1	1	1	1	1	1	1	1	1	1
②	2	2	2	2	2	2	2	2	2	2
③	1	1	3	3	3	3	3	3	1	1
④	2	2	1	1	1	1	1	4	2	2
⑤	1	1	2	2	2	2	2	1	1	1
⑥	2	2	3	3	3	3	3	2	2	2
⑦	1	1	1	1	1	1	1	3	1	1
⑧	2	2	2	2	2	2	2	4	2	2
⑨	1	1	3	3	3	3	3	1	1	1
⑩	2	2	1	1	1	1	1	2	2	2
⑪	1	1	2	2	2	2	2	3	1	1
⑫	2	2	3	3	3	3	3	4	2	2

FIG. 4

MODULE TYPE TYPE	PRO-CESS TIME	OVER-HEAD TIME	PROCESS+ OVER-HEAD
VP	52	10	62
VPC	60	5	65
CT	46	10	56
SB	60	7	67
SBC	45	5	50
PEB	60	5	65
PEBC	45	5	50
DEV	100	10	110
HB	25	10	35
HBC	22	10	32
EXPOSURE	10	15	25
OEBR	20	5	25
TARC	60	10	70
BARC	60	6	66
MORE?			

TRANSPORT TYPE	TRANSPORT TIME
CES	6
CAPTIVE-1	6
CAPTIVE-2	6
SI	6
IBTA	5
MORE?	

LOAD-LOCK=CASSETTE

FIG. 5A

500

SYSTEM THROUGHPUT, (WPH) → 80

SYSTEM TAKT TIME (SEC/WAFER) → 45

PROCESS STEP	MODULE TYPE TRANSPORT USED USED	PROCESS + OVERHEAD TIME (504)	TRANS-PORT TIME	MODULE TAKT TIME (506)	NUMBER OF MODULES REQUIRED	FUNDA-MENTAL PERIOD (508)
0	CASSETTE	0		0		
	CES		6			
1	VP	62		74	2	20.00
	IBTA		5			
2	VPC	65		75	2	38.00
	C-1		6			
3	CT	56		68	2	38.50
	C-1		6			
4	SB	67		79	2	38.50
	IBTA		5			
5	SBC	50		60	2	20.00
	C-1		5			
6	EXPOSURE	25		35	1	28.00
	SI		6			
7	PEB	65		77	2	34.25
	IBTA		5			
8	PEBC	50		60	2	37.50
	C-1		6			
9	DEV	110		122	3	35.00
	C-1		6			
10	HB	35		47	2	35.00
	C-1		6			
11	HBC	32		44	1	37.50
	CES		6			
12	CASSETTE	0		12	1	32.50
13	VACANT					
14	VACANT					
15	VACANT					
16	VACANT					
17	VACANT					
18	VACANT					

502

NO. OF MODULES → 22

MINIMUM SENDING RATE → 38.5

ACTUAL SENDING RATE → 45

FIG. 5B

ACTUAL SENDING PERIOD →

PROCESS STEP	MODULE TYPE TRANSPORT TYPE	PROCESS + OVERHEAD TIME	TRANS-PORT TIME	TIME MODULE NEED TO BE SERVED		
				ACTUAL	Ti NORM-ALIZED	Ti NORM-ALIZED
0	CASSETTE	0		0	0.000	0.000
	CES		6			
1	VP	62		68	1.511	0.511
	IBTA		5			
2	VPC	65		138	3.067	0.067
	C-1		6			
3	CT	56		200	4.444	0.444
	C-1		6			
4	SB	67		273	6.067	0.067
	IBTA		5			
5	SBC	50		328	7.289	0.289
	C-1		5			
6	EXPOSURE	25		358	7.956	0.956
	SI		6			
7	PEB	65		429	9.533	0.533
	IBTA		5			
8	PEBC	50		484	10.756	0.756
	C-1		6			
9	DEV	110		600	13.333	0.333
	C-1		6			
10	HB	35		641	14.244	0.244
	C-1		6			
11	HBC	32		679	15.089	0.089
	CES		6			
12	CASSETTE	0		685	15.222	0.222
	0		0			
13	VACANT	0		685	0.000	0.000
	0		0			
14	VACANT	0		685	0.000	0.000
	0		0			
15	VACANT	0		685	0.000	0.000
	0		0			
16	VACANT	0		685	0.000	0.000
	0		0			
17	VACANT	0		685	0.000	0.000
	0		0			
18	VACANT	0		685	0.000	0.000
			0			

602, 604, 600, 606, 608, 610

FIG. 6A

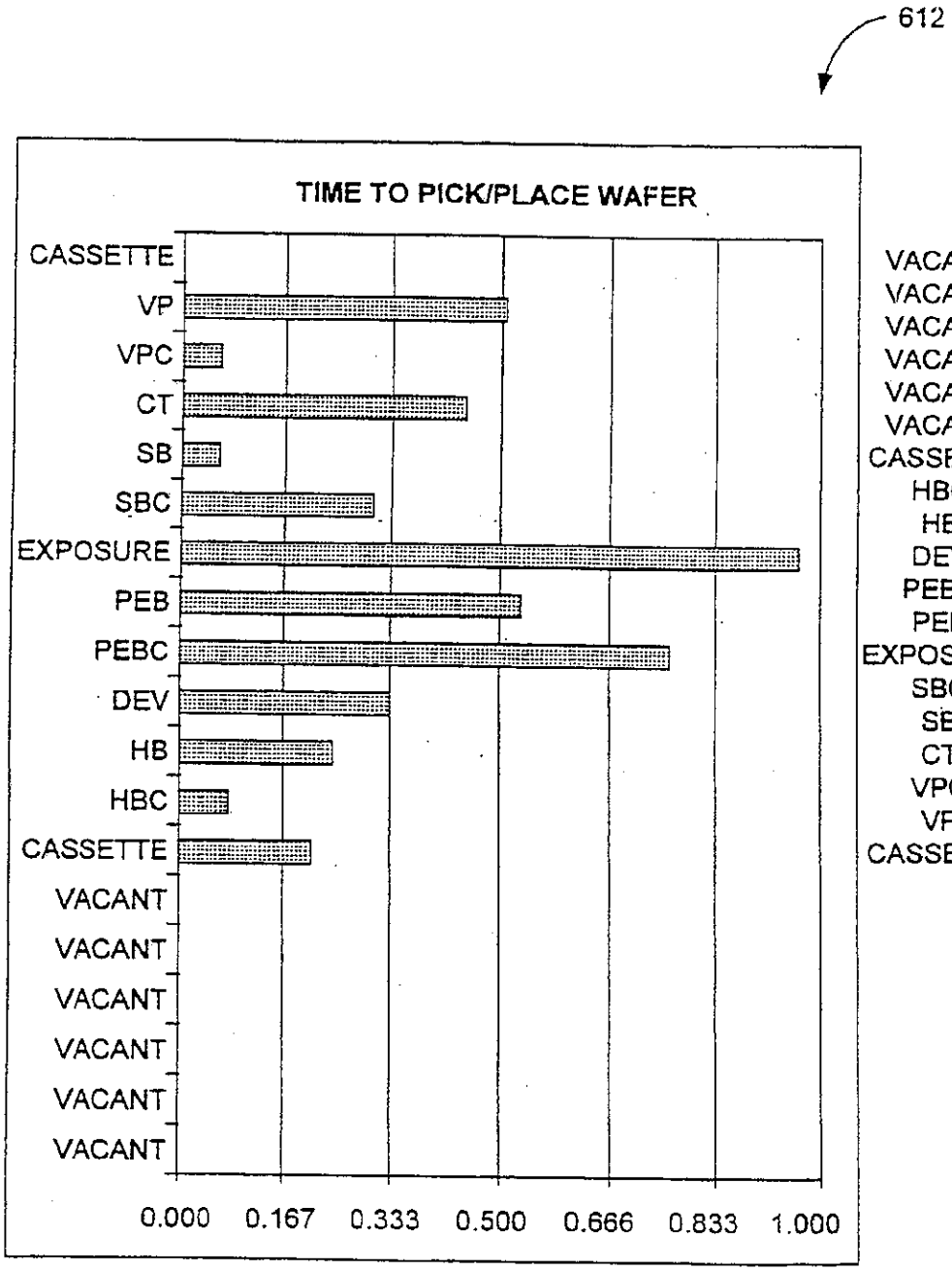

612
TIME TO PICK/PLACE WAFER
CASSETTE
VP
VPC
CT
SB
SBC
EXPOSURE
PEB
PEBC
DEV
HB
HBC
CASSETTE
VACANT
VACANT
VACANT
VACANT
VACANT
VACANT
0.000
0.167
0.333
0.500
0.666
0.833
1.000
VACANT 0.000
VACANT 0.000
VACANT 0.000
VACANT 0.000
VACANT 0.000
VACANT 0.000
CASSETTE 0.222
HBC 0.089
HB 0.244
DEV 0.333
PEBC 0.756
PEB 0.533
EXPOSURE 0.956
SBC 0.289
SB 0.067
CT 0.444
VPC 0.067
VP 0.511
CASSETTE 0.000

FIG. 6B

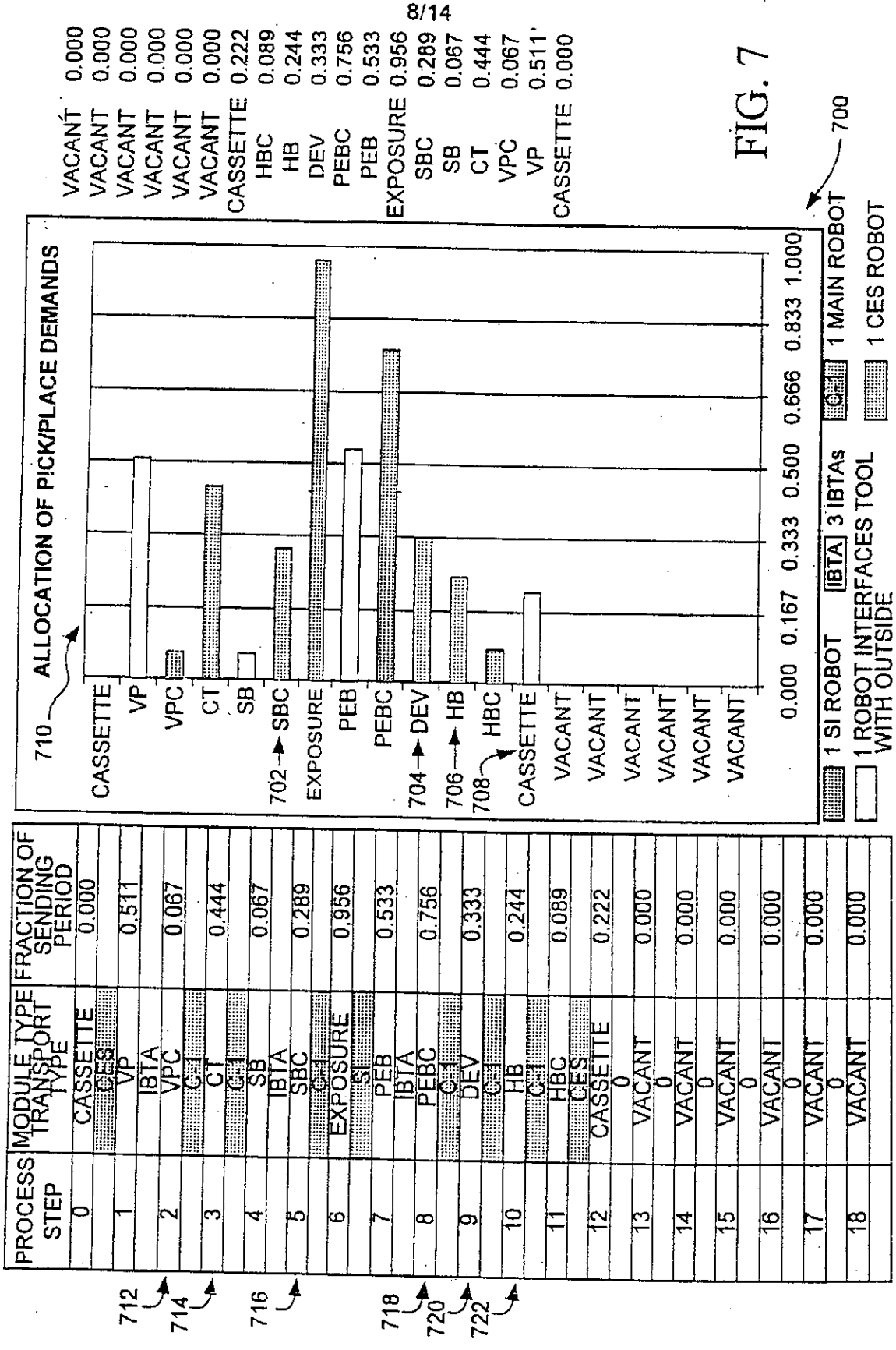
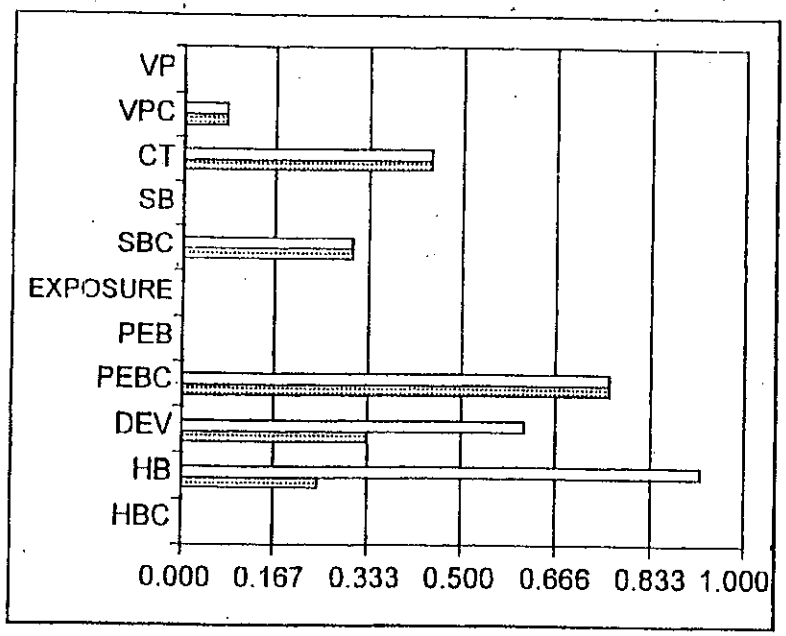

ALLOCATION OF PICK/PLACE DEMANDS
710
CASSETTE
VP
VPC
CT
SB
SBC
EXPOSURE
PEB
PEBC
DEV
HB
HBC
CASSETTE
VACANT
0.000 0.167 0.333 0.500 0.666 0.833 1.000
1 SI ROBOT
3 IBTAs
1 MAIN ROBOT
1 ROBOT INTERFACES TOOL WITH OUTSIDE
1 CES ROBOT
700
PROCESS STEP
MODULE TYPE TRANSPORT TYPE
FRACTION OF SENDING PERIOD
712
714
716
718
720
722
VACANT 0.000
VACANT 0.000
VACANT 0.000
VACANT 0.000
VACANT 0.000
CASSETTE 0.222
HBC 0.089
HB 0.244
DEV 0.333
PEBC 0.756
PEB 0.533
EXPOSURE 0.956
SBC 0.289
SB 0.067
CT 0.444
VPC 0.067
VP 0.511
CASSETTE 0.000

FIG. 7

SUBSTITUTE SHEET (RULE 26)

TABLE 1

PROCESS STEP (1)	MODULE TYPE (2)	τ AS - IS (3)	τ* TARGET (4)	τ*- τ GAP (5)	q QUE (6)	ACTUAL QUE (7)
0	CASSETTE	0.000	0.000	0.000	0.000	0.000
1	VP	0.511	0.511	0.000	0.000	0.000
2	VPC	0.067	0.067	0.000	0.000	0.000
3	CT	0.444	0.444	0.000	0.000	0.000
4	SB	0.067	0.067	0.000	0.000	0.000
5	SBC	0.289	0.289	0.000	0.000	0.000
6	EXPOSURE	0.956	0.956	0.000	0.000	0.000
7	PEB	0.533	0.533	0.000	0.000	0.000
8	PEBC	0.756	0.756	0.000	0.000	0.000
9	DEV	0.333	0.600	0.267	0.267	12.000
10	HB	0.244	0.922	0.678	0.411	18.490
11	HBC	0.089	0.089	0.000	0.322	14.510
12	CASSETTE	0.222	0.222	0.000	0.000	0.000
13	VACANT	0.000	0.000	0.000	0.000	0.000
14	VACANT	0.000	0.000	0.000	0.000	0.000



800, 802, 804, 806, 808, 809, 810, 812, 814, 816, 818, 826, 828

FIG. 8A

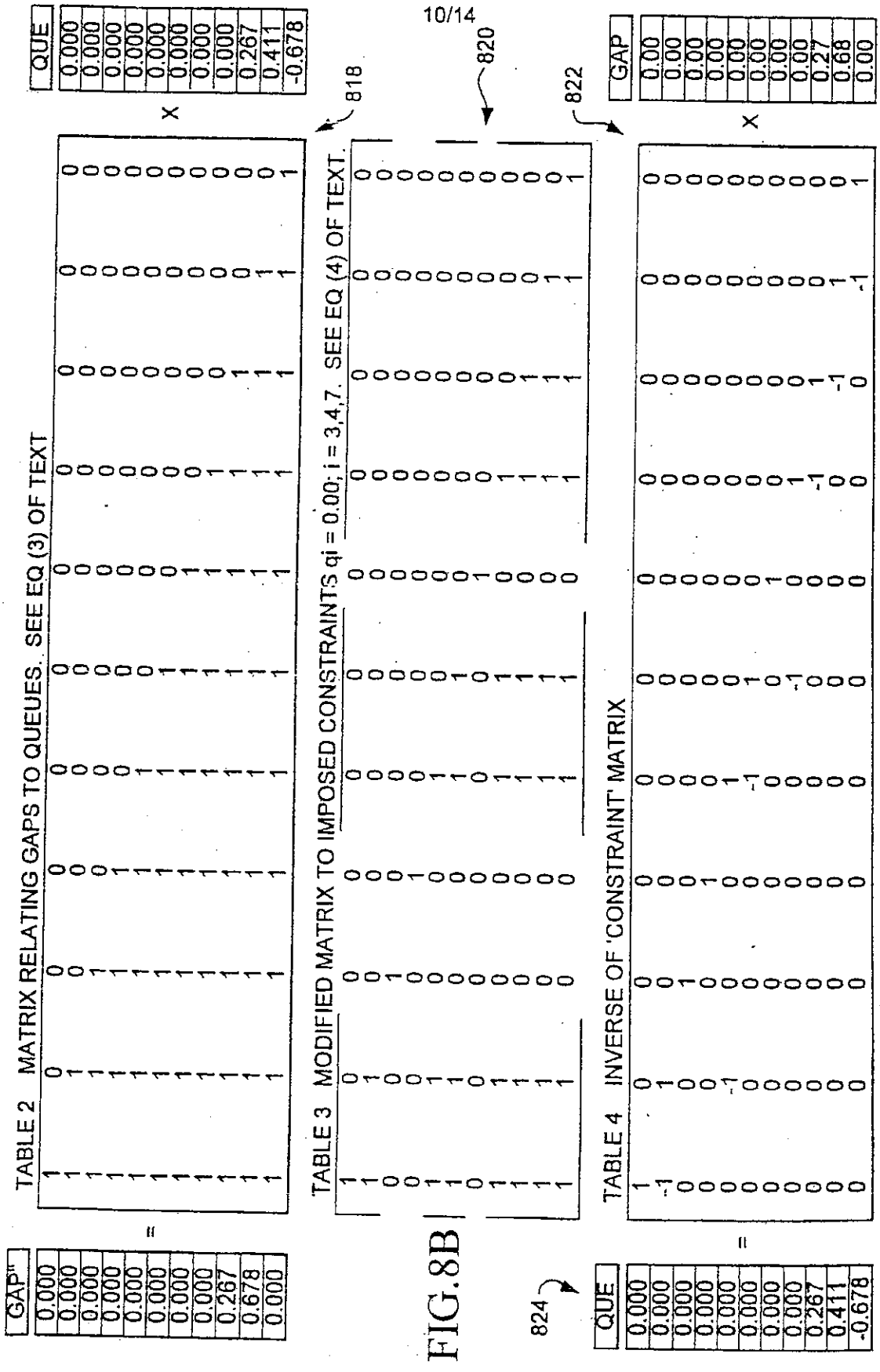

TABLE 2 MATRIX RELATING GAPS TO QUEUES. SEE EQ (3) OF TEXT
TABLE 3 MODIFIED MATRIX TO IMPOSED CONSTRAINTS qi = 0.00; i = 3,4,7. SEE EQ (4) OF TEXT.
TABLE 4 INVERSE OF 'CONSTRAINT' MATRIX
QUE
GAP
GAP''
QUE
818
820
822
824
=
X
=
X

FIG.8B

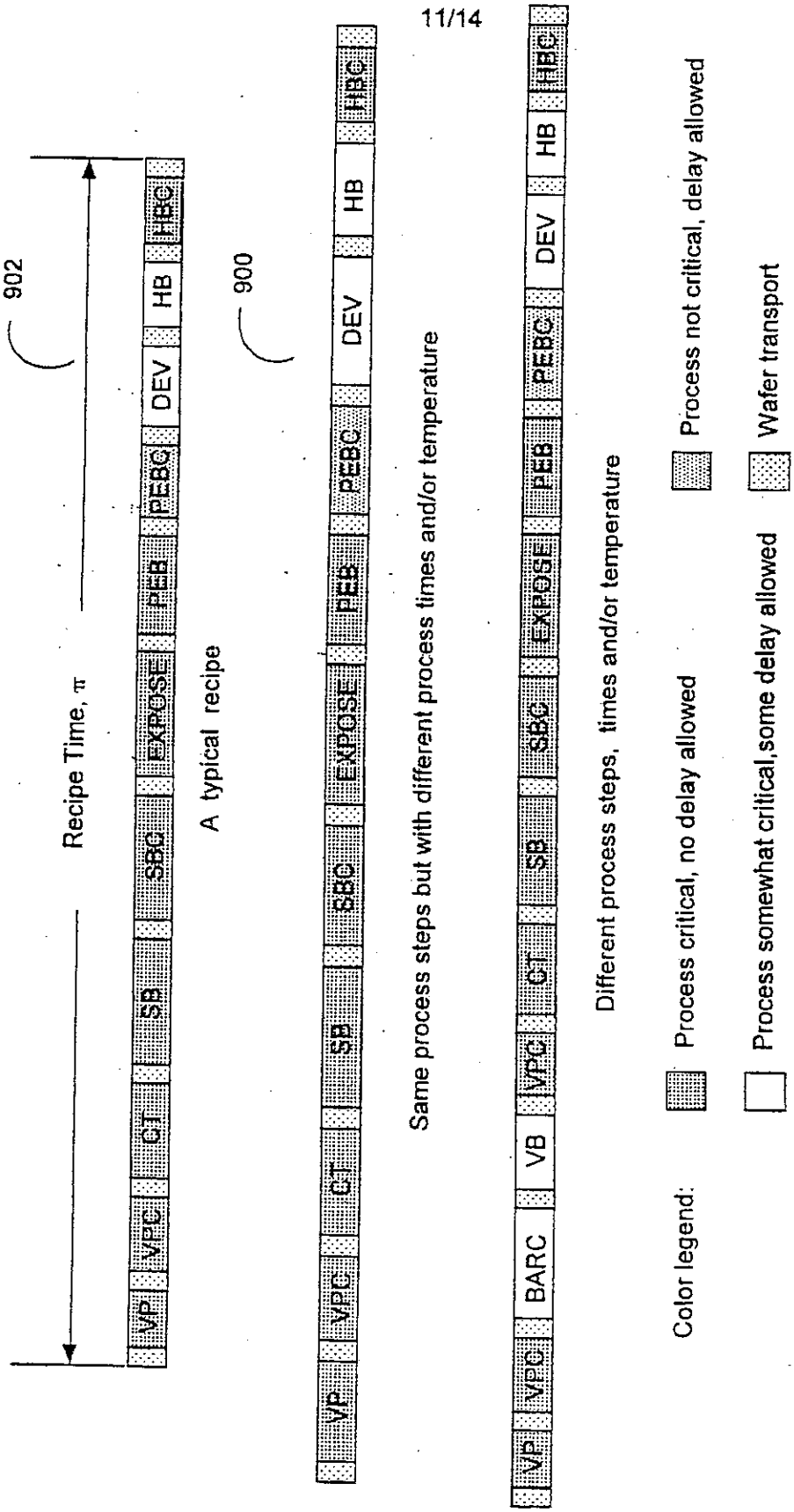

902
Recipe Time, T
900
A typical recipe
VP
VPC
CT
SB
SBC
EXPOSE
PEB
PEBC
DEV
HB
HBC
Same process steps but with different process times and/or temperature
VP
VPC
CT
SB
SBC
EXPOSE
PEB
PEBC
DEV
HB
HBC
Different process steps, times and/or temperature
VP
VPC
BARC
VB
VPC
CT
SB
SBC
EXPOSE
PEB
PEBC
DEV
HB
HBC
Color legend:
Process critical, no delay allowed
Process not critical, delay allowed
Process somewhat critical,some delay allowed
Wafer transport

FIG. 9

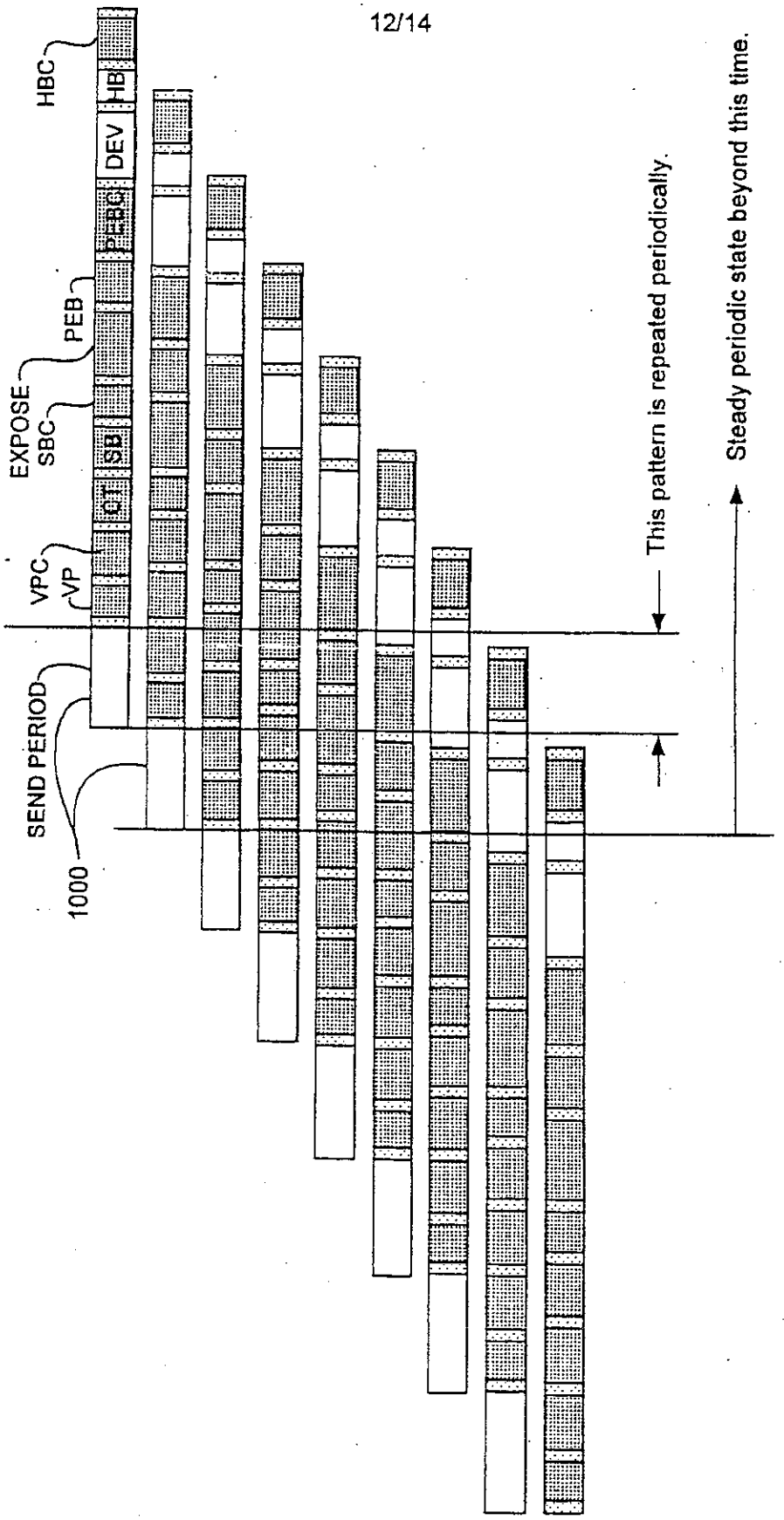

HBC
HB
DEV
PEB
PEB
EXPOSE
SBC
SB
CT
VPC
VP
SEND PERIOD
1000
This pattern is repeated periodically.
Steady periodic state beyond this time.

FIG. 10

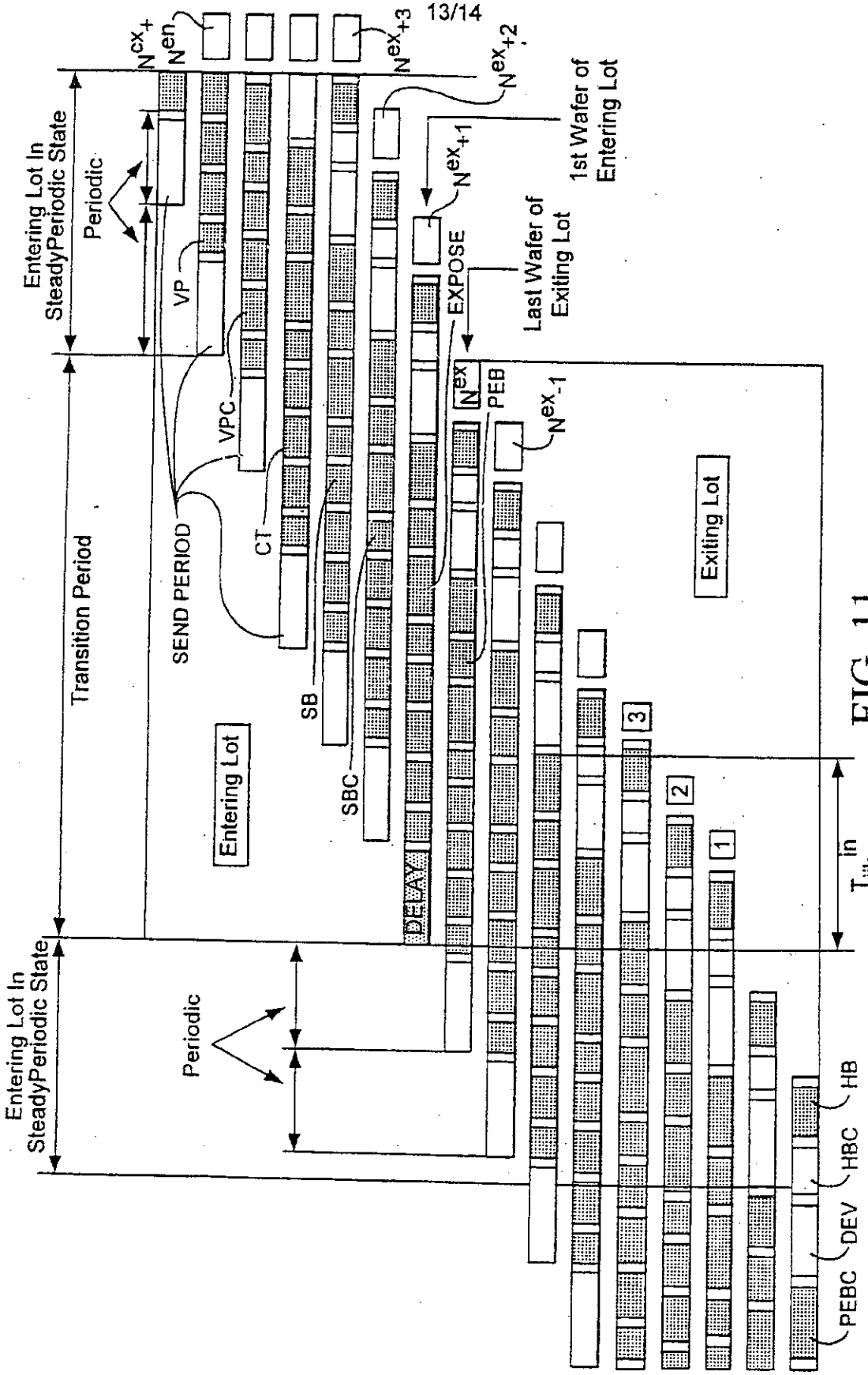

Entering Lot In SteadyPeriodic State
Periodic
Transition Period
SEND PERIOD
VP
VPC
CT
SB
SBC
DELAY
EXPOSE
PEB
Entering Lot
Exiting Lot
Last Wafer of Exiting Lot
1st Wafer of Entering Lot
HB
HBC
DEV
PEBC
1
2
3

FIG. 11

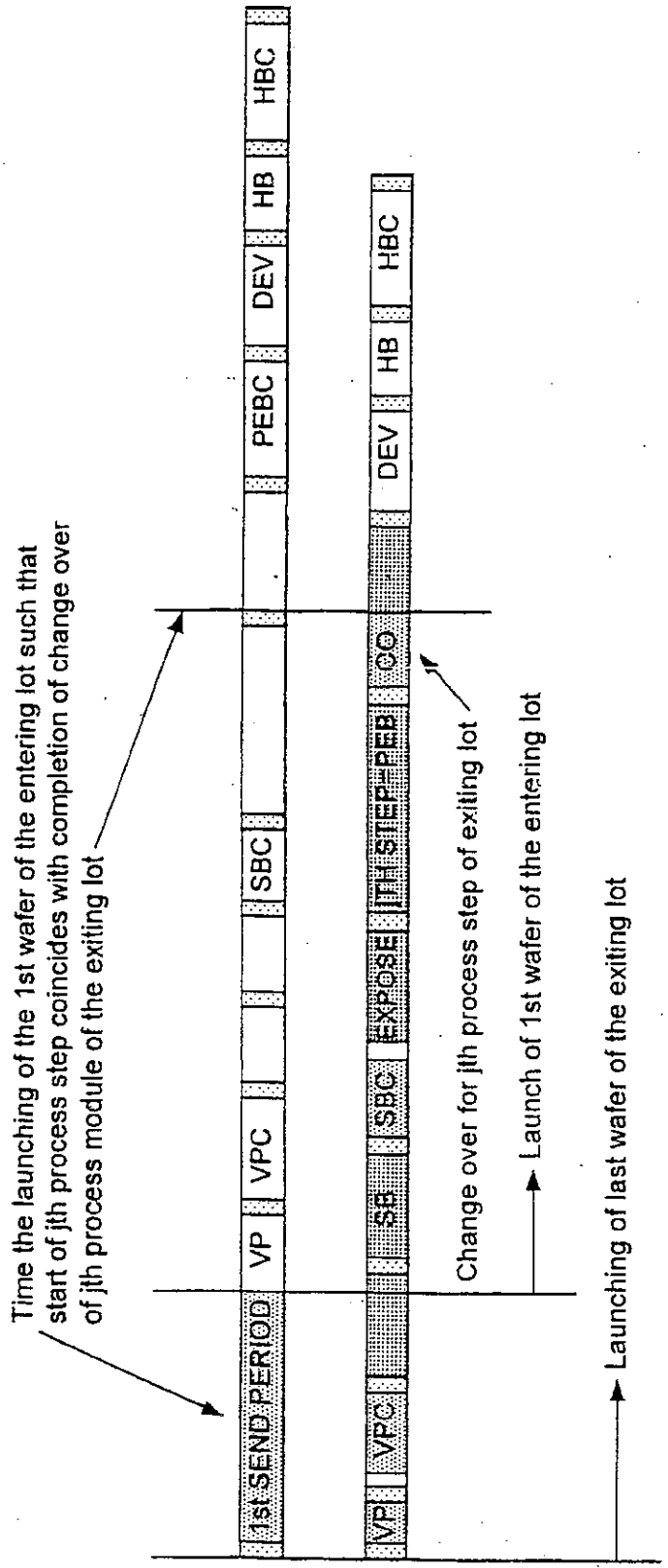

1st SEND PERIOD
VP
VPC
SBC
PEBC
DEV
HB
HBC
VP
VPC
SB
SBC
EXPOSE
ITH STEP PEB
CO
DEV
HB
HBC
Time the launching of the 1st wafer of the entering lot such that start of jth process step coincides with completion of change over of jth process module of the exiting lot
Change over for jth process step of exiting lot
Launch of 1st wafer of the entering lot
Launching of last wafer of the exiting lot

FIG. 12