CLAIMS

1. An NCFET transistor comprising a semiconductor-on-insulator substrate for a field-effect transistor, comprising, in succession from its base to its surface:
   - a semiconductor support substrate ~~(1)~~,
   - a single ferroelectric layer ~~(2)~~, arranged in direct contact with the support substrate ~~(1)~~, suitable for being polarized so as to form a negative capacitance, and
   - an active layer ~~(3)~~ of a semiconductor material, suitable for forming the channel of the transistor, arranged in direct contact with the ferroelectric layer ~~(2)~~,

   said NCFET transistor furthermore comprising a channel ~~(3b)~~ arranged in the active layer ~~(3a)~~, a source ~~(11)~~ and a drain ~~(12)~~ that are arranged in the active layer ~~(3a)~~ on either side of the channel ~~(3b)~~, and a gate ~~(10)~~ arranged on the channel ~~(3b)~~, insulated from said channel ~~(3b)~~ by a gate dielectric ~~(30)~~.

2. The NCFET transistor as claimed in claim 1, wherein the ferroelectric layer ~~(2)~~ contained in the substrate has a thickness of between 1 and 30 nm, and more advantageously of between 1 and 10 nm.

3. The NCFET transistor as claimed in claim 1 or claim 2, wherein the ferroelectric layer ~~(2)~~ has a relative dielectric permittivity greater than 10, preferably greater than 20.

4. The NCFET transistor as claimed in one of the preceding claims, wherein the ferroelectric layer ~~(2)~~ comprises hafnium oxide, zirconium oxide, yttrium oxide, lanthanum oxide, hafnium aluminate or an alloy comprising one or more of said materials.

5. The NCFET transistor as claimed in one of the preceding claims, wherein the active layer ~~(3)~~ has a thickness of between 1 nm and 100 nm.

6. The NCFET transistor as claimed in one of the preceding claims, wherein the active layer ~~(3)~~ contained in the substrate comprises silicon, germanium, a silicon-germanium alloy, gallium arsenide, indium phosphide, gallium-indium arsenide, graphene or tungsten disulfide.

7. A process for fabricating an NCFET transistor as claimed in one of claims 1 to 6, said process comprising:
    - providing the semiconductor support substrate ~~(1)~~,
    - providing a semiconductor donor substrate ~~(8)~~,
    - forming at least one ferroelectric layer ~~(2; 2a, 2b)~~ on a surface of the support substrate ~~(1)~~ and/or of the donor substrate ~~(8)~~,
    - forming a weakened zone ~~(7)~~ in the donor substrate ~~(8)~~, so as to delimit a semiconductor layer ~~(3)~~ to be transferred,
    - bonding the donor substrate ~~(8)~~ to the support substrate ~~(1)~~, each ferroelectric layer ~~(2; 2a, 2b)~~ being arranged at the bonding interface,
    - detaching the donor substrate ~~(8)~~ along the weakened zone ~~(7)~~, so as to transfer the semiconductor layer ~~(3)~~ onto the support substrate ~~(1)~~, said semiconductor layer ~~(3)~~ forming the active layer of the transistor,
    - forming a channel ~~(3b)~~ in the active layer ~~(3a)~~,
    - forming a source ~~(11)~~ and a drain ~~(12)~~ in the active layer ~~(3a)~~ on either side of the channel ~~(3b)~~,
    - depositing a gate dielectric ~~(30)~~ on the channel ~~(3b)~~ and forming a gate ~~(10)~~ on the channel ~~(3b)~~, said gate being electrically insulated from said channel ~~(3b)~~ by said gate dielectric ~~(30)~~.

8. The fabrication process as claimed in claim 7, wherein said at least one ferroelectric layer is formed by thin atomic layer deposition or by pulsed laser ablation.

9. The fabrication process as claimed in claim 7 or 8, comprising heat-treating said at least one ferroelectric layer before bonding.

10. The fabrication process as claimed in claim 9, wherein the heat treatment is carried out at a temperature of between 500°C and 1000°C.

11. The fabrication process as claimed in claim 9 or 10, wherein the heat treatment is carried out for a duration less than two hours.

12. The fabrication process as claimed in one of claims 7 to 11, wherein forming the weakened zone comprises implanting hydrogen and/or helium atoms into the donor substrate.

13. The fabrication process as claimed in one of claims 7 to 12, comprising, before bonding, one or more surface treatments on said at least one ferroelectric layer, said treatments comprising cleaning, plasma treatment and/or chemical-mechanical polishing.

14. The fabrication process as claimed in one of claims 7 to 13, comprising, after the transfer step, annealing at a temperature less than or equal to 1000°C.