FIG. 1

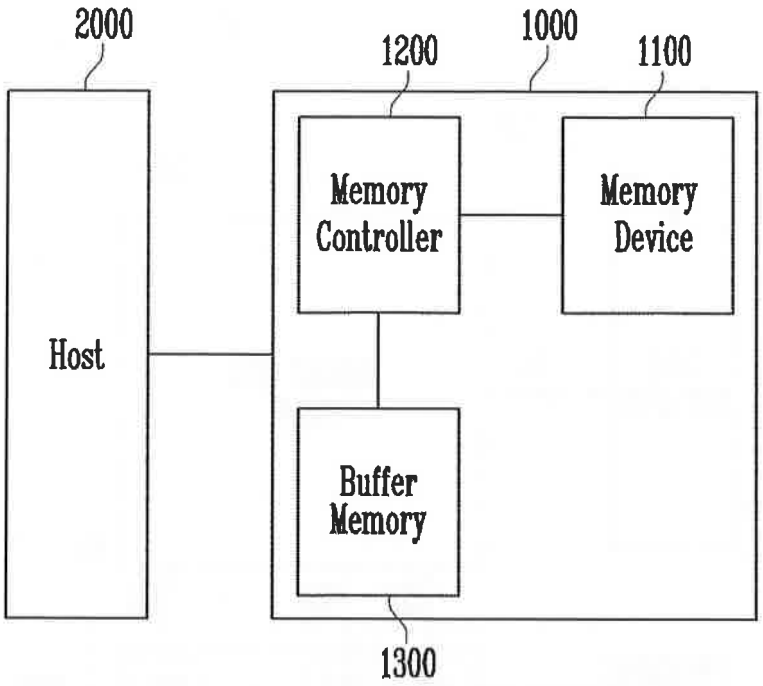

2000
1200
1000
1100
Memory Controller
Memory Device
Host
Buffer Memory
1300

FIG. 2

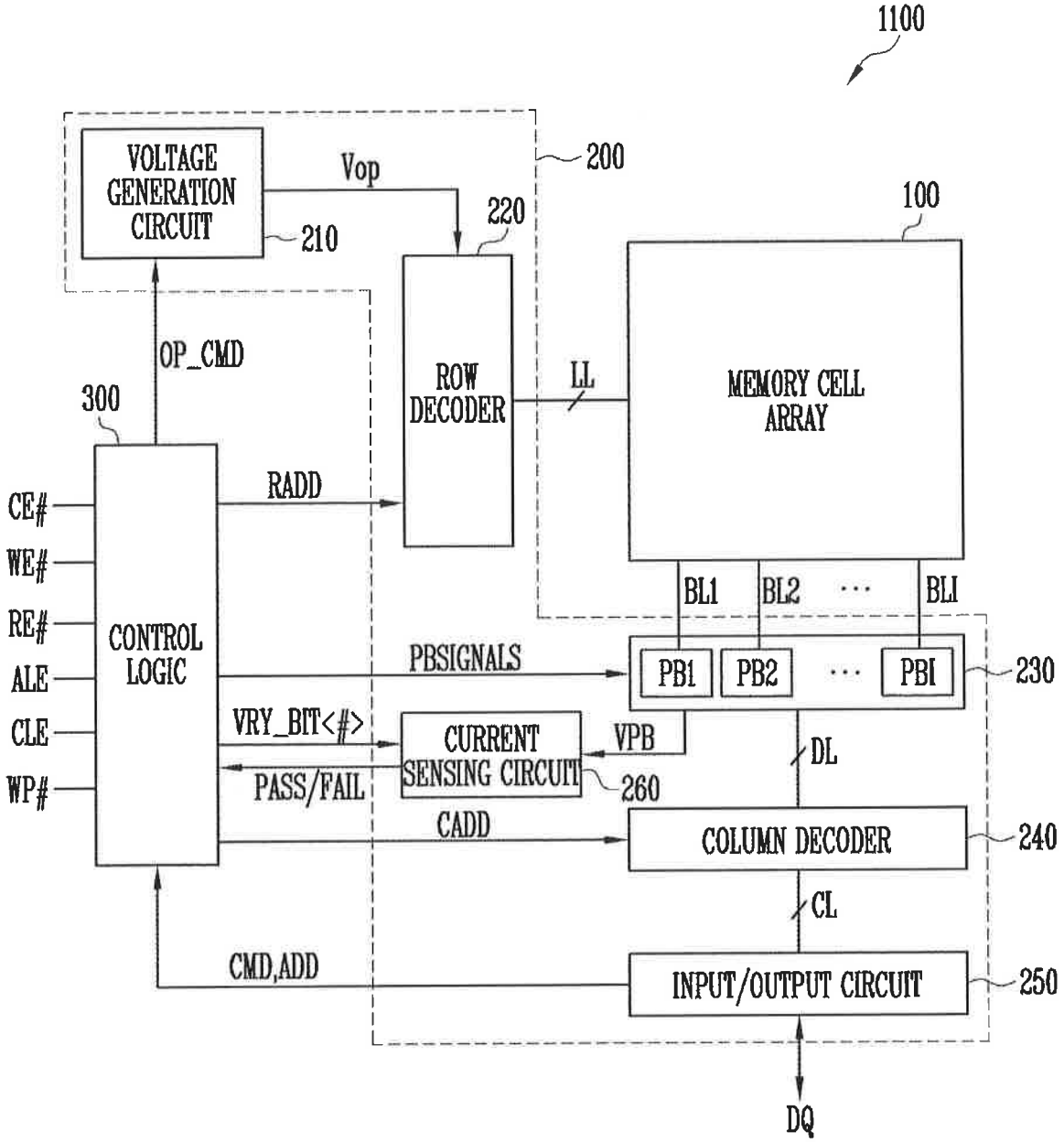

1100
200
VOLTAGE GENERATION CIRCUIT
210
Vop
220
100
OP_CMD
300
ROW DECODER
LL
MEMORY CELL ARRAY
CE#
WE#
RE#
ALE
CLE
WP#
CONTROL LOGIC
RADD
BL1
BL2
BLI
PBSIGNALS
PB1
PB2
PBI
230
VRY_BIT<#>
CURRENT SENSING CIRCUIT
VPB
DL
PASS/FAIL
260
CADD
COLUMN DECODER
240
CL
CMD,ADD
INPUT/OUTPUT CIRCUIT
250
DQ

FIG. 3

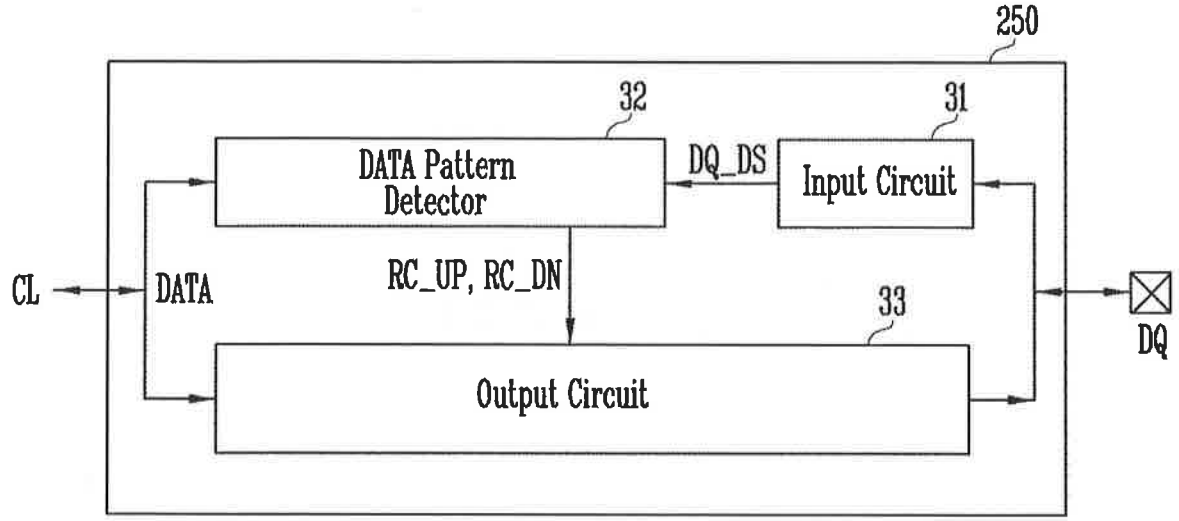

250
32
31
DATA Pattern Detector
DQ_DS
Input Circuit
CL
DATA
RC_UP, RC_DN
33
DQ
Output Circuit

FIG. 4

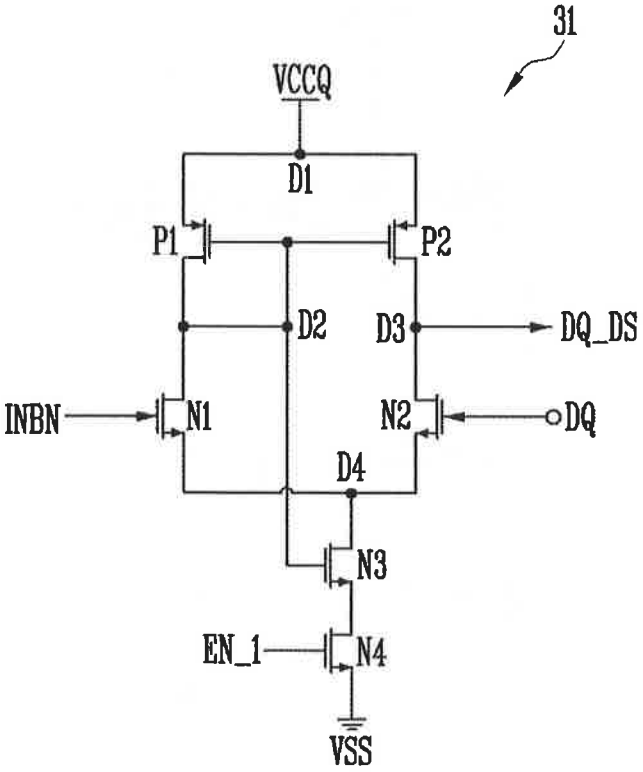

31
VCCQ
D1
P1
P2
D2
D3
DQ_DS
INBN
N1
N2
DQ
D4
N3
EN_1
N4
VSS

FIG. 5

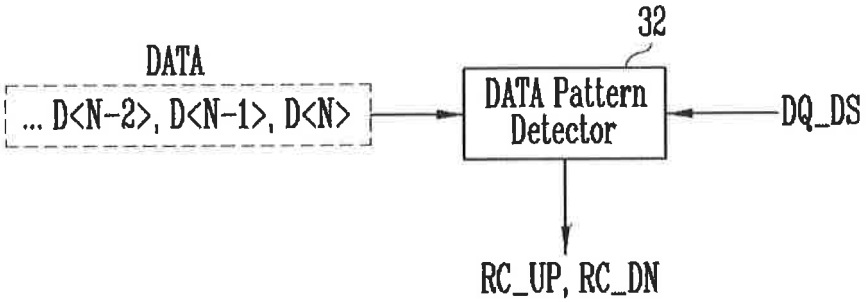

32
DATA
... D<N-2>, D<N-1>, D<N>
DATA Pattern Detector
DQ_DS
RC_UP, RC_DN

FIG. 6

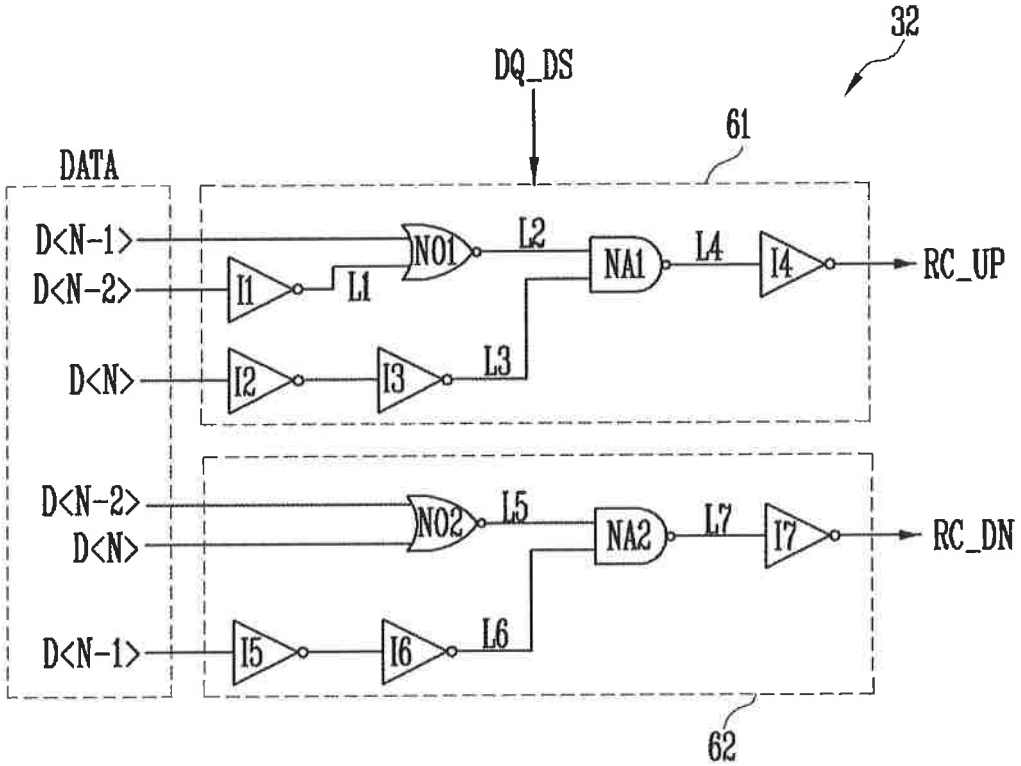

32
DQ_DS
61
DATA
D<N-1>
D<N-2>
D<N>
I1
L1
NO1
L2
NA1
L4
I4
RC_UP
I2
I3
L3
D<N-2>
D<N>
D<N-1>
NO2
L5
NA2
L7
I7
RC_DN
I5
I6
L6
62

FIG. 7

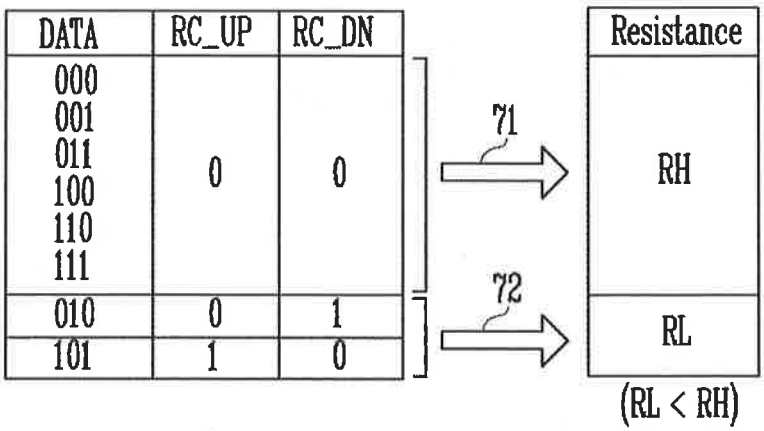

DATA
RC_UP
RC_DN
000
001
011
100
110
111
0
0
010
0
1
101
1
0
71
72
Resistance
RH
RL
(RL < RH)

FIG. 8

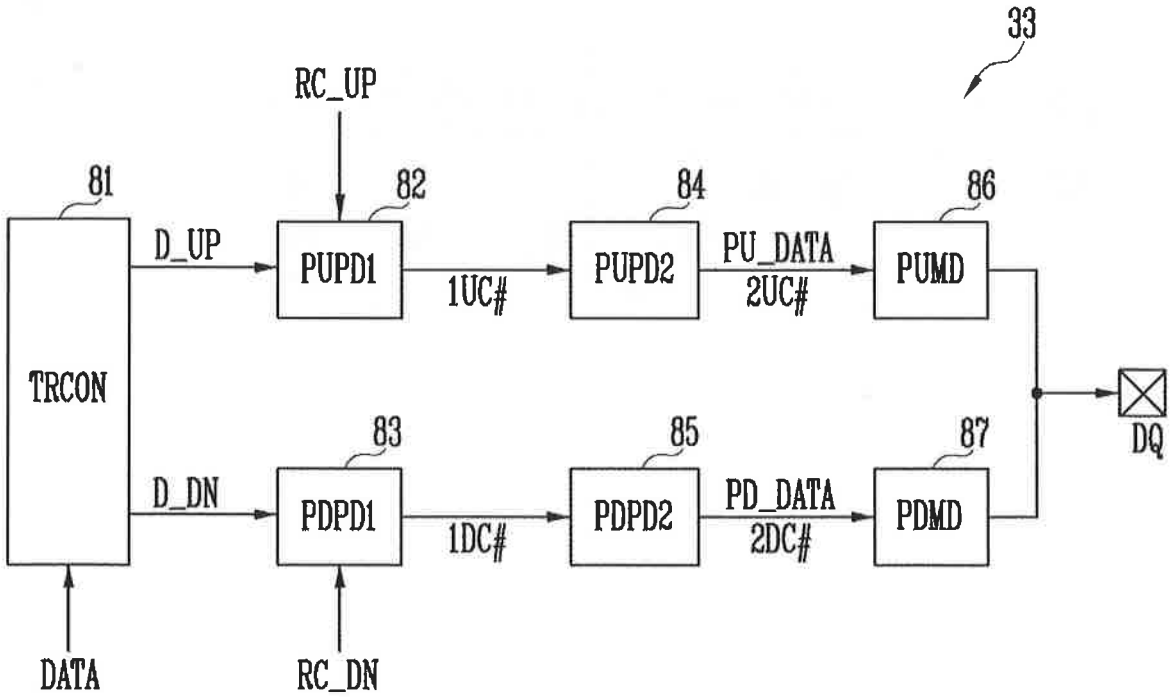

33
RC_UP
81
82
84
86
TRCON
D_UP
PUPD1
1UC#
PUPD2
PU_DATA
2UC#
PUMD
DQ
83
85
87
D_DN
PDPD1
1DC#
PDPD2
PD_DATA
2DC#
PDMD
DATA
RC_DN

FIG. 9

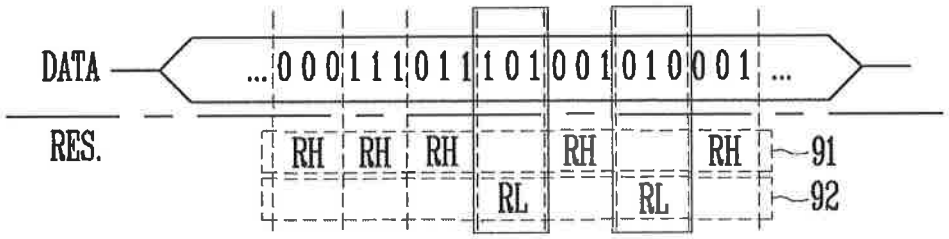

DATA
...0 0 0 1 1 1 0 1 1 1 0 1 0 0 1 0 1 0 0 1 ...
RES.
RH RH RH RH RH
RL RL
91
92

FIG. 10

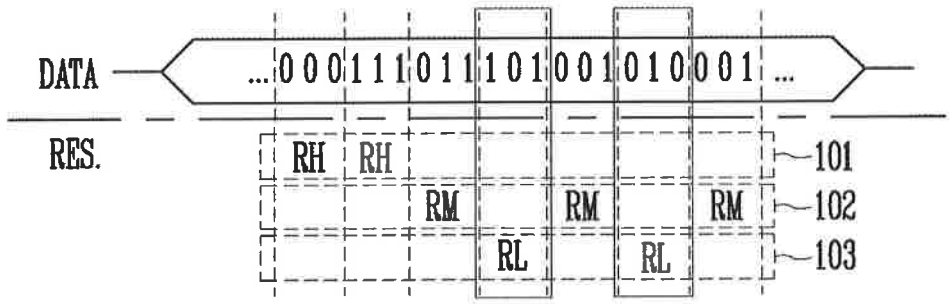

DATA
...0 0 0 1 1 1 0 1 1 1 0 1 0 0 1 0 1 0 0 1 ...
RES.
RH RH
RM RM RM
RL RL
101
102
103

FIG. 11

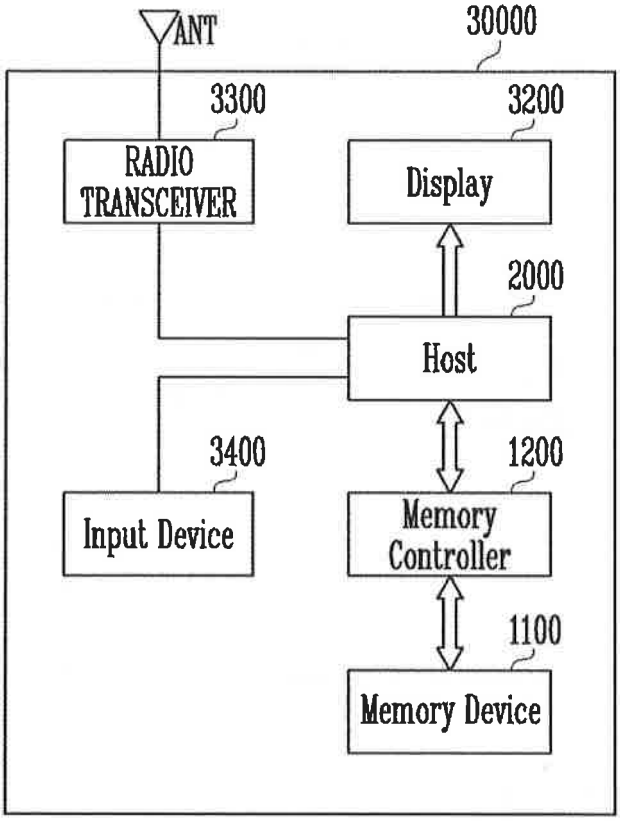

ANT
30000
3300
3200
RADIO TRANSCEIVER
Display
2000
Host
3400
1200
Input Device
Memory Controller
1100
Memory Device

FIG. 12

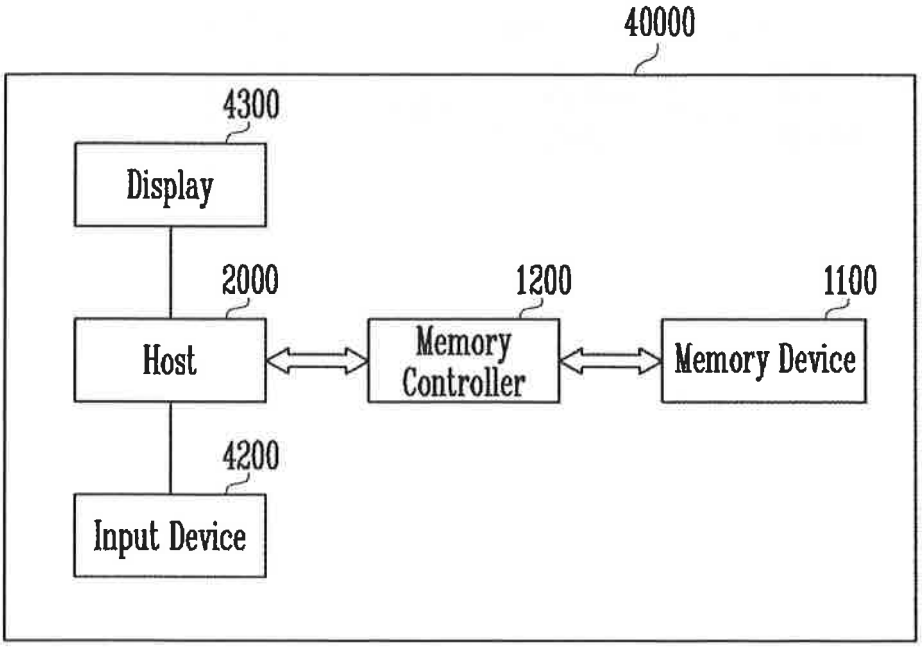

40000
4300
Display
2000
1200
1100
Host
Memory Controller
Memory Device
4200
Input Device

FIG. 13

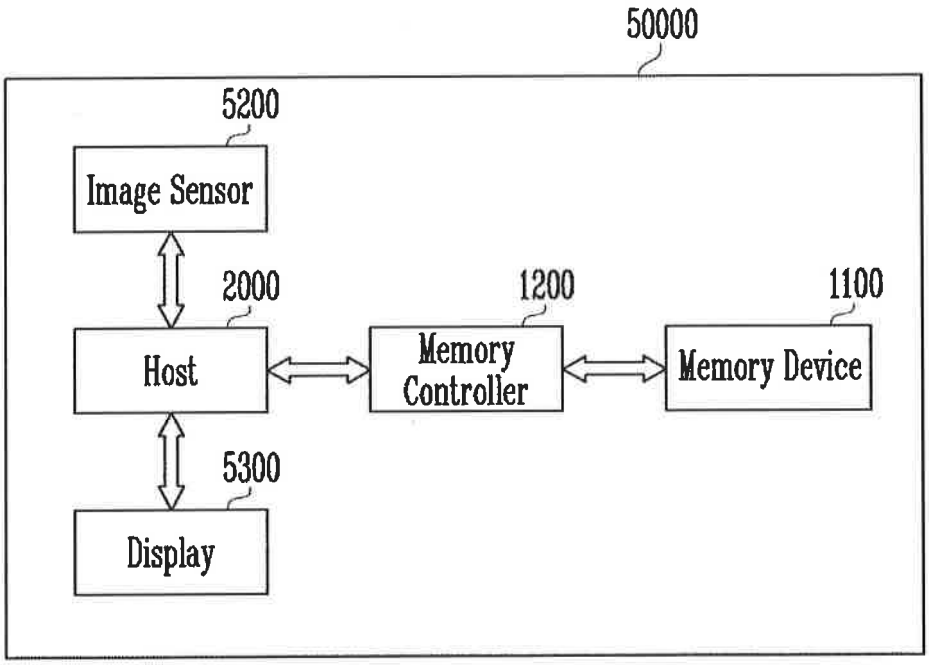
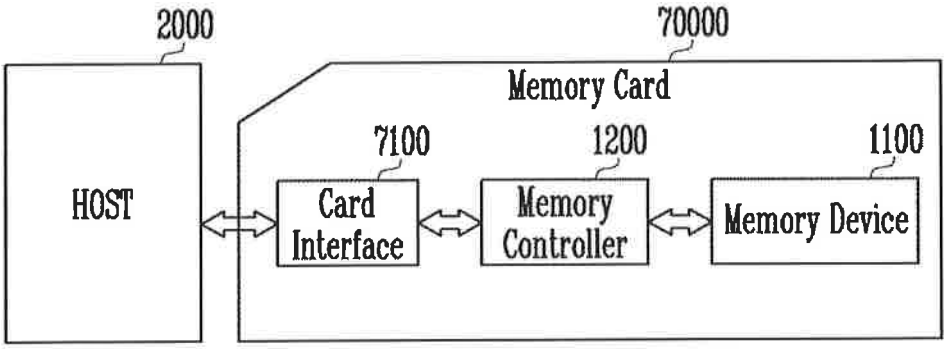

50000
5200
Image Sensor
2000
Host
1200
Memory Controller
1100
Memory Device
5300
Display

FIG. 14


2000
HOST
70000
Memory Card
7100
Card Interface
1200
Memory Controller
1100
Memory Device