Data processing system having plural adapters connecting plural peripheral devices.

ABSTRACT

A register distributed across multiple single port adapters allows the system to operate the single port adapters identically to a single multi-port adapter. Each adapter has its own priority logic identical to the logic used on a multi-port adapter to select an individual port. The priority logic on the adapter allows the system to deselect one adapter and select another adapter in one operation. Each adapter has switch settings to allow selective control of individual bits on the system bus, which allows multiple adapters to respond to the processor simultaneously for different ports in the same manner as a multi-port adapter. By replying simultaneously, the system can use the same software to control two different hardware adapter types: single port, or multi-port.

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