What is Claimed is:

1. An integrated circuit device comprising:

a conductive pattern extending on a substrate in a horizontal direction that is parallel to a surface of the substrate;

an insulating layer extending on the substrate in the horizontal direction, adjacent to and in parallel to the conductive pattern;

a channel layer extending in a channel hole penetrating the conductive pattern and the insulating layer, in a vertical direction that is perpendicular to the surface of the substrate;

a charge storage pattern inside the channel hole between the conductive pattern and the channel layer; and

a dummy charge storage pattern inside the channel hole between the insulating layer and the channel layer, the dummy charge storage pattern being separated from the charge storage pattern,

wherein the charge storage pattern and the dummy charge storage pattern extend along a straight line.

2. The integrated circuit device of claim 1, further comprising:

a first blocking dielectric pattern between the conductive pattern and the charge storage pattern; and

a second blocking dielectric pattern having a first portion between the conductive pattern and the insulating layer, a second portion between the first blocking dielectric pattern and the insulating layer, and a third portion between the charge storage pattern and the dummy charge storage pattern,

wherein the first portion, the second portion and the third portion are integrally connected.

3. The integrated circuit device of claim 2, wherein

the third portion of the second blocking dielectric pattern has an air gap between the charge storage pattern and the dummy charge storage pattern.

4. The integrated circuit device of claim 1, further comprising:

a blocking dielectric pattern spaced apart from the channel layer with the charge storage pattern therebetween, wherein

a side wall of the charge storage pattern that faces the conductive pattern, is closer to the channel layer than a side wall of the dummy charge storage pattern that faces the insulating layer, and

the blocking dielectric pattern has a side wall protruding further toward the channel layer than the insulating layer.

5. The integrated circuit device of claim 1, further comprising

a blocking dielectric pattern spaced apart from the channel layer with the charge storage pattern therebetween,

wherein the blocking dielectric pattern has a concave side wall contacting a side wall of the charge storage pattern that faces the conductive pattern.

6. The integrated circuit device of claim 1, further comprising:

a first blocking dielectric pattern between the conductive pattern and the charge storage pattern;

a second blocking dielectric pattern having a first portion between the conductive pattern and the insulating layer, a second portion between the first blocking dielectric pattern and the insulating layer, and a third portion between the charge storage pattern and the dummy charge storage pattern; and

a third blocking dielectric pattern spaced apart from the first blocking dielectric pattern and the insulating layer with the second blocking dielectric pattern therebetween, the third blocking dielectric pattern surrounding a portion of the conductive pattern,

wherein the first blocking dielectric pattern comprises a silicon oxide layer, and

each of the second blocking dielectric pattern and the third blocking dielectric pattern comprises a silicon oxide layer, a high-k dielectric layer, or a combination of the silicon oxide layer and the high-k dielectric layer.

7. The integrated circuit device of claim 1, further comprising

a blocking dielectric pattern comprising a first pattern portion contacting a side wall of the charge storage pattern that faces the conductive pattern, and a second pattern portion contacting the charge storage pattern and the dummy charge storage pattern in a space between the charge storage pattern and the dummy charge storage pattern, the second pattern portion surrounding a portion of the conductive pattern,

wherein the first pattern portion and the second pattern portion of the blocking dielectric pattern are connected to each other without a visible interface therebetween.

8. The integrated circuit device of claim 1, further comprising

a blocking dielectric pattern contacting the charge storage pattern and the dummy charge storage pattern and surrounding a portion of the conductive pattern,

wherein the blocking dielectric pattern comprises:

a first blocking dielectric pattern contacting the charge storage pattern and being spaced apart from the conductive pattern and the dummy charge storage pattern; and

a second blocking dielectric pattern comprising a portion contacting the charge storage pattern and the dummy charge storage pattern and a portion interposed between the first blocking dielectric pattern and the conductive pattern.

9. The integrated circuit device of any one of claims 1 to 8, further comprising

a tunneling dielectric layer between the charge storage pattern and the channel layer and between the dummy charge storage pattern and the channel layer, the tunneling dielectric layer extending in a direction in which the channel layer extends.

10. The integrated circuit device of any one of claims 1 to 9, wherein

a width of the charge storage pattern in the horizontal direction is different from a width of the dummy charge storage pattern in the horizontal direction.

11. The integrated circuit device of any one of claims 1 to 9, wherein

a width of the charge storage pattern in the horizontal direction is the same as a width of the dummy charge storage pattern in the horizontal direction, and a minimum horizontal distance between the charge storage pattern and the channel layer is smaller than a minimum horizontal distance between the dummy charge storage pattern and the channel layer.

12. An integrated circuit device comprising:

a plurality of conductive patterns extending on a substrate in a horizontal direction that is parallel to a surface of the substrate, the plurality of conductive patterns overlapping each other in a vertical direction that is perpendicular to the surface;

a plurality of insulating layers respectively arranged between adjacent ones of the plurality of conductive patterns, the plurality of insulating layers extending in the horizontal direction;

a channel layer extending in the vertical direction within a channel hole penetrating the plurality of conductive patterns and the plurality of insulating layers;

a plurality of charge trap patterns spaced apart from each other inside the channel hole and interposed between the plurality of conductive patterns and the channel layer;

a plurality of dummy charge trap patterns spaced apart from each other inside the channel hole and spaced apart from the plurality of charge trap patterns, the plurality of dummy charge trap patterns interposed between the plurality of insulating layers and the channel layer; and

a plurality of blocking dielectric patterns comprising a plurality of first pattern portions respectively arranged between adjacent ones of the plurality of insulating layers and interposed between the plurality of conductive patterns and the plurality of charge trap patterns, and a plurality of second pattern portions surrounding respective portions of the plurality of conductive patterns and filling respective spaces between the plurality of charge trap patterns and the plurality of dummy charge trap patterns,

wherein the plurality of charge trap patterns and the plurality of dummy charge trap patterns are arranged inside the channel hole along a straight line.

13. The integrated circuit device of claim 12, wherein

the plurality of charge trap patterns and the plurality of dummy charge trap patterns are respectively alternately arranged inside the channel hole along the straight line extending in a direction away from the substrate.

14. The integrated circuit device of claim 12 or claim 13, wherein

the plurality of charge trap patterns and the plurality of dummy charge trap patterns have a same width in the horizontal direction.

15. The integrated circuit device of any one of claims 12 to 14, wherein

the first pattern portion and the second pattern portion of each of the plurality of blocking dielectric patterns are connected to each other without a visible interface between the first pattern portion and the second pattern portion.

16. The integrated circuit device of any one of claims 12 to 15, wherein

the first pattern portion of each of the plurality of blocking dielectric patterns contacts one charge trap pattern among the plurality of charge trap patterns, and the second pattern portion of each of the plurality of blocking dielectric patterns contacts the one charge trap pattern and one dummy charge trap pattern among the plurality of dummy charge trap patterns, and

a length of each of the plurality of charge trap patterns in the vertical direction is equal to or less than a length of each of the plurality of conductive patterns in the vertical direction and equal to or greater than half of the length of each of the plurality of conductive patterns in the vertical direction.

17. The integrated circuit device of any one of claims 12 to 16, wherein

the plurality of second pattern portions comprise air gaps in the respective spaces between the plurality of charge trap patterns and the plurality of dummy charge trap patterns.

18. The integrated circuit device of any one of claims 12 to 17, wherein

one or more of the plurality of first pattern portions have concave side walls concave toward the channel layer, and

one or more of the plurality of charge trap patterns have convex side walls facing the concave side walls, wherein the concave side walls contact the convex side walls.

19. An integrated circuit device comprising:

a lower conductive line and an upper conductive line extending in a horizontal direction in parallel to each other on a substrate;

an insulating layer extending in the horizontal direction between the lower conductive line and the upper conductive line;

a channel layer in a channel hole extending in a vertical direction by penetrating the lower conductive line, the upper conductive line, and the insulating layer;

a lower charge trap pattern in the channel hole, the lower charge trap pattern interposed between the lower conductive line and the channel layer;

an upper charge trap pattern in the channel hole, the upper charge trap pattern interposed between the upper conductive line and the channel layer and being spaced apart from the lower charge trap pattern in the vertical direction; and

a dummy charge trap pattern between the insulating layer and the channel layer, the dummy charge trap pattern being spaced apart from the lower charge trap pattern by a lower separating space and from the upper charge trap pattern by an upper separating space;

a lower first blocking dielectric pattern between the lower conductive line and the channel layer;

an upper first blocking dielectric pattern between the upper conductive line and the channel layer;

a lower second blocking dielectric pattern between the lower conductive line and the lower first blocking dielectric pattern, the lower second blocking dielectric pattern filling the lower separating space; and

an upper second blocking dielectric pattern between the upper conductive line and the upper first blocking dielectric pattern, the upper second blocking dielectric pattern filling the upper separating space,

wherein the lower charge trap pattern, the upper charge trap pattern and the dummy charge trap pattern extend along a straight line.