

A RAIL - TO - RAIL LOW VOLTAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to amplifiers, and more particularly to a rail-to-rail low voltage linear operational transconductance amplifier.

Brief Description of the Prior Art

State of the art IC design requires operation at low power supply voltages because of the trend toward miniaturization, and a need for portable equipment powered by conventional batteries. The relatively low voltages supplied by conventional batteries cause performance difficulties. A lower supply voltage results in lower signal dynamic range and an increased signal to noise ratio. In order to improve performance, recent designs have attempted to maximize the dynamic range by incorporating rail-to-rail input/output capability. Rail-to-rail performance by definition exists in a transconductance amplifier when the output current is directly proportional to i.e. linear with variation of the input voltage over the full range of voltage available from the power supply. There have been several reports on the design of rail-to-rail low voltage Operational Amplifiers, as noted by Sakurai and Ismail "Low Voltage CMOS Operational Amplifiers", Kluwer Academic Publishers, Boston, 1995. A disadvantage of the amplifiers reported in this publication is that none of them have linear differential mode input voltage to output current over the full range of supply voltage. In other words, they are not capable of true linear rail-to-rail operation. Therefore, they cannot be used in g_m -C active filter synthesis.

The problem with the prior art devices is that CMOS operational transconductance amplifiers constructed from a simple differential pair exhibit a linear transconductance behavior only over a very limited differential input voltage range of a few hundred millivolts. This is discussed by Kardontchik, "Introduction to the Design of Transconductance-Capacitor Filters", Kluwer Academic Publications, Boston, 1992. The improved designs, also discussed in Kardontchik's book, have extended the linear input voltage range to a few volts, but the range does not include the power supply rails, and therefore they do not provide true rail-to-rail performance. U.S. Pat. No. 5,208,552 by Ryat discloses a device referred to as a rail-to-rail OTA. However, this circuit only has a rail-to-rail common mode input range. The differential input linear range is only a few hundred millivolts, and therefore is seriously limited in filter applications. The circuit of Ryat is actually a rail-to-rail input stage of an Operational Amplifier, as described by Sakurai and Ismail, rather than a rail-to-rail input linear OTA. U.S. Pat. No. 4,656,436 by Saari describes a CMOS transconductance circuit with triode mode input. However, there are two serious limitations of the circuit reported by Saari. First, a simple cascode circuit configuration is used so that the input MOS transistor drain to source voltage changes with the input signal, and as a result the linearity of the transconductance would be poor. Second, the linear input range is not rail-to-rail, and therefore not suitable for low voltage applications.

In view of the prior art described, there is a clear need for a transconductance amplifier with a linear rail-to-rail input voltage specification, that can be widely used in low voltage analog and mixed signal integrated circuits and systems, particularly in low voltage g_m -C active filters with improved performance.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an improved rail-to-rail operational transconductance amplifier.

It is a further object of the present invention to provide a single ended rail-to-rail operational transconductance amplifier.

It is a still further object of the present invention to provide a differential input rail-to-rail operational transconductance amplifier.

It is another object of the present invention to provide a transconductance bias voltage supply circuit for a rail-to-rail operational transconductance amplifier.

Briefly, a preferred embodiment of the present invention includes a CMOS operational transconductance amplifier (OTA) having an input voltage vs output current relationship that is linear for an input voltage range extending from one power supply rail to another power supply rail. The input transconducting CMOS transistors operate in the non-saturation region with a feedback loop for precisely holding the drain to source voltage constant. A pair of complementary circuits, each having an OTA designated OTAN having n-MOS input transistors, and an OTA designated OTAP having p-MOS input transistors, in conjunction with n-MOS transistor and p-MOS transistor current mirrors, are connected in parallel to implement a single ended OTA having rail-to-rail voltage input and push-pull current output. Two of these pairs, with complementary input transistors, are used with their outputs paralleled to provide a differential input rail-to-rail OTA. The basic OTA circuit provided is capable of operating at a supply voltage larger than two times the MOS transistor threshold voltage V_T . When the supply voltage is 2V and the MOS transistor threshold voltage is 0.7V, the output current deviation from perfect linearity is less than 0.2% over the rail-to-rail input voltage range.

IN THE DRAWING

Fig. 1 is a block diagram of an OTA;

Fig.2 is a more detailed block diagram of the OTA of Fig. 1;

Fig.3 is a diagram of an OTAN;

Fig.4 shows further detail of the OTAN of Fig. 3;

Fig.5 is a detailed schematic of an OTAP;

Fig.6 is a diagram of a bias circuit;

Fig. 7 illustrates the use of the bias circuit of Fig. 6 to bias a plurality of OTAs; and

Fig. 8 shows a differential input OTA.

Description of the Preferred Embodiment

Referring now to Fig. 1 of the drawing, an operational transconductance amplifier 10 is shown for the purpose of introducing the basic operation of the present invention. The amplifier 10 has inputs 12 and 14, and an output 16. There is a supply voltage input 18, and return connection 20. Transconductance control inputs 22 and 24 are used to input voltages for control of the level of amplification/transconductance.

In operation, control voltages VCP and VCN are applied to inputs 22 and 24, a supply voltage V_{DD} on input 18, and a ground connection to terminal 20. Input 14 has a fixed voltage $V_{DD}/2$ applied. The amplifier 10 provides an output current I_o at 16 in response to a voltage V_{in} at input 12 according to equations (1) and (2).

$$I_o = I_{on} = - (M_n \cdot K_n \cdot VDSN) (V_{in} - V_{DD}/2) \text{ when } V_{in} > \text{ or } = V_{DD}/2 \quad (1)$$

$$I_o = I_{op} = - (M_p \cdot K_p \cdot VDSP) (V_{in} - V_{DD}/2) \text{ when } V_{in} < \text{ or } = V_{DD}/2 \quad (2)$$

The terms $(M_n \cdot K_n \cdot VDSN)$ and $(M_p \cdot K_p \cdot VDSP)$ are constants, the factors of which will be defined in the following specification. The constants VDSN and VDSP depend on the control voltages VCN and VCP respectively. The circuitry internal to amplifier 10 accomplishing the rail-to-rail performance indicated by equations (1) and (2) will be fully described in reference to the following figures of the drawing.

The OTA of Fig. 1 is shown in further detail in Fig. 2, and includes an OTA 26, designated as OTAP, and an OTA 28 designated as OTAN. The OTAN has two inputs 30 and 32 for receiving input voltages V_{G1} and V_{G2} , and an output 34 for output of a current I_{on} . Input 36 is connected to 18 for application of voltage V_{DD} , and terminal 38 is connected to ground terminal 20. Terminal 24 receives the control voltage V_{CN} . The output I_{on} is related to the input voltage V_{G1} and V_{G2} according to equation (3).

$$\begin{aligned} I_{on} &= - (M_n \cdot K_n \cdot V_{DSN}) (V_{G2} - V_{G1}) \text{ when } V_{G1} > V_{G2} \\ &= 0 \text{ when } V_{G1} < V_{G2} \end{aligned} \quad (3)$$

OTAP 26 is similar to OTAN 28 except that the transistors used in OTAN 28 are opposite in type to those in OTAP 26. For example, a transistor at a particular place in the circuit of OTAP 26 that is n-type will be a p-type in the corresponding place in the OTAN 28. The "P" and "N" letters in OTAN and OTAP are used to indicate that the input transistors of the OTAP are p-type, and the input transistors of the OTAN are n-type.

The two inputs 40, 42 are for receiving voltages V_{29} and V_{39} respectively. Input 44 is connected to input 18 for voltage V_{DD} . Input 46 is connected to ground terminal 20. Output 48 sinks current I_{op} according to equation (4).

$$\begin{aligned} I_{op} &= - (M_p \cdot K_p \cdot V_{DSP}) (V_{G39} - V_{G29}) \text{ when } V_{G29} < V_{G39} \\ &= 0 \text{ when } V_{G39} > V_{G29} \end{aligned} \quad (4)$$

The basic building block pertaining to the present invention is the structure of the OTAs 26 and 28. This structure is more fully described in Fig. 3, illustrating the OTAN 28. The structure of OTAP 26 would be obtained by simply changing all n-MOS transistors to p-MOS, and all p-MOS transistors to n-MOS. The inputs 30 and 32 to the gates of n-type input transistors M₁ and M₂ are for application of

input voltages V_{G1} and V_{G2} . The drain-source voltages V_{DS1} and V_{DS2} of transistors M_1 and M_2 are held constant through use of feedback networks 50 and 52. A voltage source VDSN 54 provides the necessary voltage reference for the networks 50, 52. A first current mirror 56 receives the voltage VDD through input 36, and according to principles well known to those skilled in the art, provides a current I_{D2} at output 58 when a current I_{D1} is present at the input 60. The current mirror input 60 is connected to network 50 and passes a current I_{D1} substantially equal to and identified as the drain current of transistor M_1 . The output 58 of mirror 56 is connected to network 52 which draws a current I_{D2} substantially equal to the drain current of transistor M_2 . Output 62 passes the difference between the two drain currents, $I_{D1} - I_{D2}$ to the second current mirror 64, which provides an output current I_{on} equal to $I_{D1} - I_{D2}$ times a constant multiplicative factor M_N at output 34. This is expressed by equation (5).

$$I_{on} = M_N (I_{D1} - I_{D2}) \quad (5)$$

Feedback networks 50, 52 contain amplifiers 66, 68 and transistors M_3 , M_4 respectively. The amplifiers 66, 68 receive the reference voltage VDSN, and maintain the drain-source voltage V_{DS1} of M_1 equal to V_{DS2} of M_2 equal to the value VDSN. The basic principle of operation of the OTAN is explained as follows.

The MOS input transistors M_1 and M_2 are operated in the non-saturation region with a fixed drain to source voltage and serve as transconducting elements suitable for low voltage operation. The I-V equation of an n-MOS transistor in its non-saturation region is expressed by

$$I_D = K_n (V_{GS} - V_{TN}) V_{DS} - (1/2) K_n \cdot V_{DS}^2 \quad (6)$$

I_D is the drain current, V_{GS} is the gate to source voltage, V_{DS} is the drain to source voltage, V_{TN} is the threshold voltage of the n-MOS transistor, and

$$K_n = (\mu_n \varepsilon / t_{ox}) (W/L) \quad (7)$$

where μ_n is the electron mobility, and ε and t_{ox} are the permittivity and thickness of the gate oxide, respectively. W and L are the channel width and channel length of the MOS transistor, respectively. The non-saturation condition of the N-MOS transistor is

$$V_{DS} < (V_{GS} - V_{TN}) \quad (8)$$

The drain currents of transistors M_1 and M_2 are expressed by equations (9) and (10)

$$I_{D1} = K_n (V_{GS1} - V_{TN}) V_{DS1} - (1/2) K_n \cdot V_{DS1}^2 \quad (9)$$

$$I_{D2} = K_n (V_{GS2} - V_{TN}) V_{DS2} - (1/2) K_n \cdot V_{DS2}^2 \quad (10)$$

The feedback networks 50, 52 hold $V_{DS1} = V_{DS2} = V_{DSN}$, if the gain of the amplifier A_1 (A_2) is large enough. The current output $I_{D1} - I_{D2}$ provided by OTAN, as explained above, is then expressed by equation (11).

$$I_{D1} - I_{D2} = (K_n \cdot V_{DSN}) (V_{G1} - V_{G2}) \quad (11)$$

V_{G1} , and V_{G2} are the gate voltages of input transistors M_1 and M_2 respectively. The source voltages of M_1 and M_2 are the same. It can be seen from equation (11) that $I_{D1} - I_{D2}$ is linear with respect to $(V_{G1} - V_{G2})$ when V_{DSN} is a constant. From equation (8), it can be easily shown that equations (12) and (13) must hold to ensure the validity of equation (11):

$$V_{G1} > V_{TN} + V_{DSN} \quad (12)$$

$$V_{G2} > V_{TN} + V_{DSN} \quad (13)$$

In order for $I_{D1} - I_{D2}$ to be positive, and allow output 34 to sink current, V_{G1} must be greater than V_{G2} i.e. $V_{G1} > V_{G2}$. I_{on} will therefore be equal to

$$\begin{aligned} I_{on} &= M_N (I_{D1} - I_{D2}) \text{ when } V_{G1} > V_{G2} \\ I_{on} &= 0 \text{ when } V_{G1} < V_{G2} \end{aligned} \quad (14)$$

This can be expressed in terms of voltages V_{G1} and V_{G2} using equation (11) with equation (14).

$$\begin{aligned} I_{on} &= M_N K_N V_{DSN} (V_{G1} - V_{G2}) \text{ when } V_{G1} > V_{G2} \\ I_{on} &= 0 \text{ when } V_{G1} < V_{G2} \end{aligned} \quad (14)$$

Owing to the bounds imposed by equations (12) and (13), a single OTAN does not show rail to rail input performance. In order to extend the input range to cover the full rail-to-rail supply voltage, a complementary OTAP circuit is used in conjunction with the OTAN circuit, as was shown in Fig. 2. The OTAP circuit is derived from the OTAN circuit by replacing all n-type transistors with p-type transistors, and all p-type transistors with n-type transistors, and by swapping the polarities of the supply rails. The resulting network was described in general terms in reference to Figs. 1 and 2. The voltage and current quantities of OTAP satisfy the following equations:

$$\begin{aligned} I_{op} &= (M_p \cdot K_p \cdot V_{DSP}) (V_{G39} - V_{G29}) \text{ when } V_{G29} < V_{G39} \\ &= 0 \text{ when } V_{G29} > V_{G39} \end{aligned} \quad (15)$$

$$V_{G29} < V_{DD} - |V_{TP}| - V_{DSP} \quad (16)$$

$$V_{G39} < V_{DD} - |V_{TP}| - V_{DSP} \quad (17)$$

$$K_p = (\mu_n \varepsilon / t_{ox}) (W/L) \quad (18)$$

V_{G29} and V_{G39} are the gate voltages of the two input p-MOS transistors M29, M39. V_{TP} is the threshold voltage of the p-MOS transistors. μ_p is the hole mobility. The drain to source voltage of the input transistors M₂₉ and M₃₉, held to VDSP by the feedback networks.

The output current I_o of the OTA of Fig. 2 can then be expressed by :

$$I_o = I_{ON} = - (M_N \cdot K_n \cdot V_{DSN}) (V_{in} - V_{DD}/2) \text{ when } V_{in} > \text{ or } = V_{DD}/2$$

$$I_o = I_{OP} = - (M_p \cdot K_p \cdot V_{DSP}) (V_{in} - V_{DD}/2) \text{ when } V_{in} < \text{ or } = V_{DD}/2 \quad (19)$$

The bounds imposed by equations (12) (16) (13) (17) can now be replaced by a unified bound of power supply voltage:

$$V_{DD} > V_{TN} + V_{TP} + V_{DSN} + V_{DSP} \quad (20)$$

In principle, the magnitudes of VDSN and VDSP may be arbitrarily close to zero. Their values are determined by the transconductance values depicted in equation (19). This can be clearly understood by inspection of the more detailed Figs. 4 and 5.

It can be seen from equation (19) that in order to ensure linearity over the entire range of V_{in} , the transconductances of OTAN and OTAP must be equal. Denoting this transconductance as GM, it can be seen from equation (19) that,

$$M_N \cdot K_n \cdot V_{DSN} = M_p \cdot K_p \cdot V_{DSP} = GM \quad (21)$$

Equation (19) can now be rewritten as equation (22) for the entire rail-to-rail input voltage range,

$$I_o = - GM (V_{in} - V_{DD}/2) \quad (22)$$

Figs. 4 and 5 show further details of the construction of the OTAP 26 and OTAN 28 circuits. In the OTAN 28 circuit of Fig. 4, the amplifiers A1 (66) and A2 (68), included in feedback networks 50 and 52, are shown to be constructed from transistors M7 - M11 and M12 - M16, respectively, as well as transistors M3 and M4. Transistor M20 and current source IRN and the associated circuitry provide biasing for M₁₁ and M₁₆. The drain to source voltage V_{DSN} of input transistors M1 and M2 is determined by the resistor RN and the gate voltage V_{CN} of M17. The current mirror 64 includes M18 - M19 and has two functions. First, the current mirror 64 only allows the OTAN output to sink current when $V_{G1} > V_{G2}$. When V_{G1} is less than or equal to V_{G2} , the output current is zero, since M₁₉ is unable to source current. This is a desired characteristic of the OTAN, as will be explained later. Second, the current mirror M18 - M19 provides current multiplication. The amount of multiplication is determined by the factor M_N which may be larger than unity. M_N is the ratio of the channel widths of M19 to M18 for the same channel length. A large M_N value improves the efficiency of the power consumption of the circuit and the output voltage range. The current mirror 56 discussed in the context of Fig. 3 includes the transistors M5 and M6 shown in Fig. 4. The inputs 30, 32 and outputs 62 and 34 were discussed in reference to Fig. 3, and are all noted in Fig. 4 for reference.

The OTAP circuit 26, as explained above, functions in a similar manner to the OTAN circuit 28, except for the differences due to the different transistor type and voltage. Fig.5. shows the two input transistors M29 and M39 and input voltages V_{G29} and V_{G39} . V_{DSP} is the source to drain voltage of the input transistors M29 and M39, and is controlled by the voltage V_{CP}. The OTAP can only source current when $V_{G29} < V_{G39}$. The complete rail-to-rail OTA is shown in Fig. 2 with the OTAN and OTAP circuits connected in parallel. V_{G2} in the OTAN and V_{G39} in the OTAP are connected together to the common voltage $V_{DD}/2$. V_{G1} in the OTAN and V_{G29} in OTAP are connected together to receive the input voltage V_{in} of the OTA. The output current of the OTA is equal to the sum of the currents from the OTAN and the OTAP. When V_{in} is higher than $V_{DD}/2$, the OTAN

output sinks current and the OTAP output current is zero. When V_{in} is lower than $V_{DD}/2$, the output current is sourced by the OTAP and the OTAN output current is zero. In other words, the output is a push-pull circuit.

The biasing voltages VDSN (Fig. 4) and VDSP (Fig. 5) cannot be selected independently if equation (21) is to be satisfied. Fig. 6 shows a circuit which will produce a VDSN satisfying equation (21) with a given VDSP. Referring back to Figs. 4 and 5, it is apparent that the voltages VDSN and VDSP are determined by the values of the control voltages VCN and VCP respectively. These relationships were also discussed above in reference to the figures of the drawing. The novel biasing circuit of Fig. 6 uses an OTAP and an OTAN to determine the proper voltage VCN with a given VCP. Since OTAPs and OTANs are also the subjects to be biased, the proper voltage VCN is derived with a high degree of accuracy. Accuracy is further enhanced when the various OTAPs and OTANs are all fabricated on the same chip, since they will then be as identical as possible, not being subject to wafer-to-wafer variations. The present invention, however, is not limited to any particular construction method.

The operation of the circuit of Fig. 6, is explained as follows: A voltage VCP is applied at 70 to an OTAP 72. Note that OTAN 74 input is connected to V_{DD} while OTAP 72 input is connected to ground. The function of the circuit 76 is to provide a VCN, for a given VCP, that will cause the output current and therefore transconductance of an OTAN to be equal to the output current of the OTAP. In circuit 76, the OTAP responds to the input $V_{DD}/2$ and VCP by outputting I_{op} . $I_{op} = G_m V_{DD}/2$, where G_m is the transconductance of the OTAP equal to $(M_p \cdot K_p \cdot VDSP)$. The voltage across resistor RS1 is $V_p = RS1 \cdot G_m V_{DD}/2$.

The OTAN outputs current I_{on} which is dependent on VCN. I_{on} is reflected by current mirror 80 to a current I_{on} passing through RS2. If $V_n > V_p$, the output of op-amp 78 (i.e. VCN) will be high. VCN is feedback to OTAN 74. As a result, I_{on} 34 (see Fig.4) will decrease. The decrease in I_{on} will be mirrored by current mirror

80 to cause V_n to decrease. similarly, if $V_n < V_p$, feedback net work 82 and current mirror 80 will cause V_n to increase. The equilibrium point is thus $V_n = V_p$. Referring again to Fig. 6 and equation (19), $I_{op} = (M_p \cdot K_p \cdot VDSP) V_{DD}/2$ and the voltage across the resistor R_{S1} is $V_p = R_{S1} (M_p \cdot K_p \cdot VDSP) V_{DD}/2$. The voltage across the resistor R_{S2} is $V_N = R_{S2} (M_N \cdot K_N \cdot VDSN) V_{DD}/2$. For $R_{S1} = R_{S2}$, we have $M_p \cdot K_p \cdot VDSP = M_N \cdot K_N \cdot VDSN$ satisfying equation (21).

Since in an analog or mixed signal VLSI system, many identical OTAs are needed. The circuit in Fig. 6 can now be used as a master bias VCN generator. Fig 7 shows a complete application of several OTAs biased by a single master bias. Voltage VCP adjusts the transconductance value of all the OTAs simultaneously. It can be used for tuning the time constant for a filter application.

The OTA so far described has only a single ended input, however it can be extended to a differential input operational transconductance amplifier DOTA, as shown in Fig. 8. In Fig. 8, two operational transconductance amplifiers, OTA and OTA' are used. The OTA of Fig. 8 is the same as the OTA of Fig. 2. OTA' is identical to the OTA in Fig. 2 except that OTAN is replaced by OTAN' and OTAP is replaced by OTAP' . The OTAN' is identical to the OTAN in Fig. 4 except that the output current mirror (the N-MOS transistors M18 - M19) is replaced by a current mirror consisting of two P-MOS transistors M18P-MI9P with sources connected to V_{DD} . Therefore, OTAN' only sources output current when $V_{G2} > V_{G1}$ and the output current equals zero when $V_{G2} < V_{G1}$. Correspondingly, OTAP' is identical to OTAP in Fig. 5 except the output current mirror (the p-MOS transistors $M_{37} - M_{38}$.) is replaced by a current mirror consisting of two n -MOS transistors $M_{37N} - M_{38N}$ with sources connected to the ground terminal. Therefore OTAP' only sinks output current when $V_{G29} > V_{G39}$, and the output current equals zero when $V_{G29} < V_{G39}$. OTAN' and OTAP' are connected in parallel as in Fig. 2 to form an OTA', with the - input connected to $V_{DD}/2$ and the + input connected to V_{in} . The output current of the DOTA of Fig. 8 is therefore:

$$I_o = G_M (V_+ - V_-) \quad (14)$$

The OTA or DOTA circuit has been simulated by SPICE, using SPICE level 2 with 3 micron CMOS technology device parameters. When V_{DD} is 2V and the MOS transistor threshold voltage $V_T = 0.7V$, the peak error from perfect linearity is less than 0.2% for a rail-to-rail input voltage range.

The design of a rail-to-rail low voltage single ended input OTA and a rail-to-rail low voltage differential input DOTA have been described. The transconductance characteristic with respect to input voltage is linear from rail-to-rail, and the circuit is capable of operating at a low supply voltage V_{DD} provided that V_{DD} is larger than two times the threshold voltage of the MOS transistors. Simulation results show that its peak deviation from perfect linearity is less than 0.2% for rail-to-rail input voltage with $V_{DD} = 2V$.

Although the above disclosure has presented the preferred embodiment of the invention, variations will be apparent to those skilled in the art. For example, other feedback circuitry can be substituted for the circuits 50, 52, and other types of transistors can be used. Such variations that will be apparent to those skilled in the art are also included in the spirit of the present invention.

In the claims:



CLAIMS

1. A single ended rail-to-rail operational transconductance amplifier comprising:

(a) an OTAN including

(i) a first plurality of transistors and a second plurality of transistors wherein said first plurality of transistors are of n type, and said second plurality of transistors are of p type, and wherein said first plurality of transistors include input transistors,

(ii) first feedback means for maintaining a constant drain to source voltage of said input transistors;

(iii) an OTAN output;

(b) an OTAP complementary to said OTAN wherein said first plurality of transistors are of p type and said second plurality of transistors are of n type, and said OTAP having an OTAP output; wherein said OTAN and said OTAP are connected in parallel providing said single ended rail-to-rail OTA having a single ended input.

2. A rail-to-rail OTA as recited in claim 1 wherein

(a) said OTAN further includes first OTAN current mirror means providing a first current indicative of the difference between a drain current of a first OTAN said input transistor and a drain current of a second OTAN said input transistor; and

(b) said OTAP further includes first OTAP current mirror means complementary to said first OTAN current mirror means, and said OTAP having a first OTAP input transistor and a second OTAP input transistor.

3. A rail-to-rail OTA as recited in claim 2 wherein

(a) said OTAN further includes second OTAN current mirror means responsive to said first current for sinking current when a gate voltage of said first



OTAN input transistor is greater than a gate voltage of said second OTAN input transistor; and

(b) said OTAP further includes second OTAP current mirror means complimentary to said second OTAN current mirror means, for sourcing current when a first gate voltage to said first OTAP input transistor is greater than a second gate voltage to said second OTAP input transistor.

4. A rail-to-rail OTA as recited in claim 1 further comprising means for setting the value of said drain to source voltage of said input transistor to be maintained constant by said feedback means.

5. A rail-to-rail OTA as recited in claim 1 wherein said OTAN sinks current from said OTAN output when said OTAP sources zero current to said OTAP output, and said OTAN sinks zero current from said OTAN output when said OTAP sources current to said OTAP output.

6. An operational transconductance amplifier comprising

(a) first and second input transistors

(b) feedback means for maintaining a constant drain to source voltage of said first and second input transistors;

(c) first current mirror means providing a first current indicative of the difference between a drain current of said first input transistor and a drain current of said second input transistor; and

(d) second current mirror means responsive to said first current for providing an output current proportional to said first current.

7. An operational transconductance amplifier as recited in claim 6 wherein said output current is current sinking.

8. An operational transconductance amplifier as recited in claim 6 wherein said output current is current sourcing.



9. A differential input operational transconductance amplifier comprising:

(a) a first rail-to-rail single ended operational transconductance amplifier including

(i) a first OTAN providing operational transconductance amplification having

(a) first and second input transistors of a first type;

(b) feedback means for maintaining a constant drain to source voltage of said input transistors;

(c) means for sinking current;

(ii) a first OTAP providing operational transconductance amplification having

(a) first and second input transistors of a second type;

(b) feedback means for maintaining a constant drain to source voltage of said input transistors;

(c) means for sourcing current; and wherein said first OTAN and first OTAP are connected in parallel to provide said first rail-to-rail single ended operational transconductance amplifier, and said first operational transconductance amplifier having a first rail-to-rail single ended operational transconductance amplifier input and a first operational transconductance amplifier output; and

(b) a second rail-to-rail single ended operational transconductance amplifier including

(i) a first OTAN' providing operational transconductance amplification having

(a) first and second input transistors of a first type;

(b) feedback means for maintaining a constant drain to source voltage of said input transistors;

(c) means for sourcing current;

(ii) a first OTAP' providing operational transconductance amplification having



- (a) first and second input transistors of a second type;
- (b) feedback means for maintaining a constant drain to source voltage of said input transistors;
- (c) means for sinking current; and wherein said first OTAN' and said first OTAP' are connected in parallel to provide said second rail-to-rail single ended operational transconductance amplifier, said second operational transconductance amplifier having a second rail-to-rail single ended operational transconductance amplifier input and a second operational transconductance amplifier output; and wherein said first rail-to-rail single ended operational transconductance amplifier input and said second rail-to-rail single ended operational transconductance amplifier input provide a differential input for said differential operational transconductance amplifier, and wherein said first operational transconductance amplifier output is connected with said second operational transconductance amplifier output to provide a differential operational transconductance amplifier output.

10. An operational transconductance amplifier as recited in claim 1 further comprising a biasing circuit responsive to a first control voltage to output a second control voltage, said first control voltage for biasing said OTAP to source a first current and said second control voltage for biasing said OTAN to sink a second current equal to said first current.

11. An operation transconductance amplifier as recited in claim 10 wherein said biasing circuit includes

- (a) a bias circuit OTAN having an input voltage equal to $V_{DD}/2$;
- (b) a bias circuit OTAP having an input voltage equal to $V_{DD}/2$;
- (c) a VCP input to said bias circuit OTAP for receiving said first control voltage; and
- (d) a biasing circuit feedback network for adjusting said second control voltage to cause said second current to equal said first current.