

What is claimed is:

1. A manufacturing method for an integrated circuit, comprising: a sub-process of profile modification in a shallow trench isolate layer (STI) gap-fill using a high aspect ratio process (HARP), wherein the sub-process of profile modification in a shallow trench isolate layer (STI) gap-fill using a high aspect ratio process (HARP), comprising: first, the HARP is performed to deposit STI HARP deposits with a certain thickness using CVD process, then a method for removing silicon dioxide from a wafer is employed to perform an etching operation on the STI to enlarge its opening, and the HARP and the etching operation are repeatedly performed until the manufacturing method ends; or

a manufacturing method for an integrated circuit, comprising: a sub-process for removing a SiO_2 natural oxide layer on a hard mask layer of a STI gap fill using HARP, wherein the hard mask layer of the STI is made of Si_3N_4 , and the sub-process for removing a SiO_2 natural oxide layer on a hard mask layer of the STI, comprising: in the sub-process, the SiO_2 natural oxide layer on a surface of the hard mask layer of the STI is etched using a method for removing silicon dioxide from a wafer, and an etch selectivity ratio of the SiO_2 natural oxide layer relative to the STI HARP deposits is controlled, such that the SiO_2 natural oxide layer is removed rapidly, and excessive etching of the STI HARP deposits is prevented; or

a manufacturing method for an integrated circuit, comprising: a sub-process for removing a pad oxide layer, wherein the pad oxide layer is a SiO_2 layer formed by oxidizing a surface of a substrate by means of heating, and is a buffer layer for a hard mask layer made of Si_3N_4 of a STI gap fill using HARP; and the sub-process for removing a pad oxide layer, comprising: in the sub-process, the pad oxide layer is etched using a method for removing silicon dioxide from a wafer, and an etch selectivity ratio of the pad oxide layer relative to the STI HARP deposits is controlled, such that the pad oxide layer is removed rapidly, and excessive etching of the STI HARP deposits is prevented; or

a manufacturing method for an integrated circuit, comprising: a STI recess

sub-process in a manufacturing method of a 2D NAND memory; wherein the NAND memory comprises: a floating gate and graphically intensive area STI HARP deposits located in a graphically intensive area; and a control switch gate and graphically sparse area STI HARP deposits located in a graphically sparse area, the floating gate and the control switch gate are made of polycrystalline silicon, and the graphically intensive area STI HARP deposits and the graphically sparse area STI HARP deposits are made of silicon dioxide, and in the STI recess sub-process, the graphically intensive area STI HARP deposits and the graphically sparse area STI HARP deposits are etched using a method for removing silicon dioxide from a wafer, and an etch selectivity ratio of the STI HARP deposits relative to the floating gate or relative to the control switch gate is controlled, such that the STI HARP deposits is removed rapidly, and excessive damage to the floating gate and the control switch gate is prevented;

wherein the method for removing silicon dioxide from a wafer, comprising:

introducing dehydrated hydrogen fluoride gas and dehydrated alcohol gas into a process chamber;

mixing the dehydrated hydrogen fluoride gas and the dehydrated alcohol gas to generate a gaseous etchant;

causing the etchant to react with a wafer in the process chamber, and maintaining a pressure in a range of 30Torr to 300Torr in the process chamber to increase an etch selectivity ratio; and

extracting a reaction product from the process chamber.

2. The manufacturing method for an integrated circuit according to claim 1, wherein the pressure in the process chamber is 200Torr.

3. The manufacturing method for an integrated circuit according to claim 1, wherein a temperature in the process chamber is in a range of 20°C to 80°C.

4. The manufacturing method for an integrated circuit according to claim 3, wherein the temperature in the process chamber is 40°C.

5. The manufacturing method for an integrated circuit according to claim 1, wherein a flow rate of the hydrogen fluoride gas is in a range of 100sccm to 500sccm, and a flow rate of the alcohol gas is in a range of 100sccm to 1000sccm.

6. The manufacturing method for an integrated circuit according to claim 5, wherein the flow rate of the hydrogen fluoride gas is in a range of 150sccm to 225sccm, and the flow rate of the alcohol gas is in a range of 200sccm to 450sccm.

7. The manufacturing method for an integrated circuit according to claim 1, wherein a ratio of a flow rate of the hydrogen fluoride gas to a flow rate of the alcohol gas is 0.8:1 to 1.2:1.

8. The manufacturing method for an integrated circuit according to claim 5, wherein a ratio of the flow rate of the hydrogen fluoride gas to the flow rate of the alcohol gas is 1:1.

9. The manufacturing method for an integrated circuit according to claim 1, wherein the alcohol gas is at least one of C₁ to C₈ monohydric alcohol gas.

10. The manufacturing method for an integrated circuit according to claim 9, wherein the alcohol gas is at least one of methanol, ethanol, and isopropyl alcohol.