

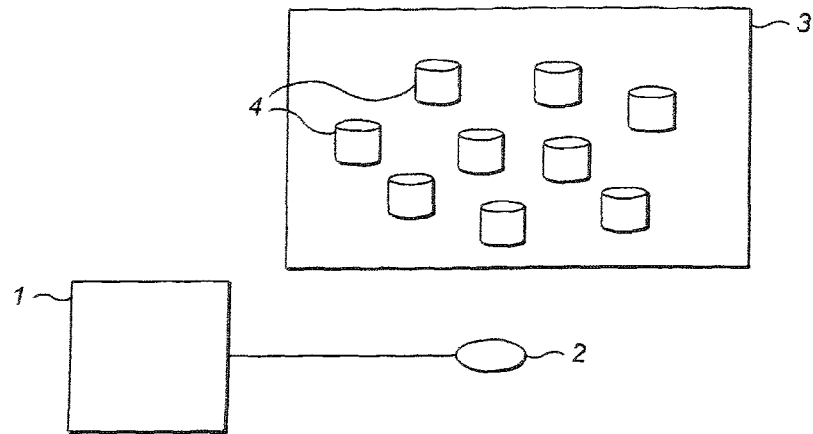


FIG. 1

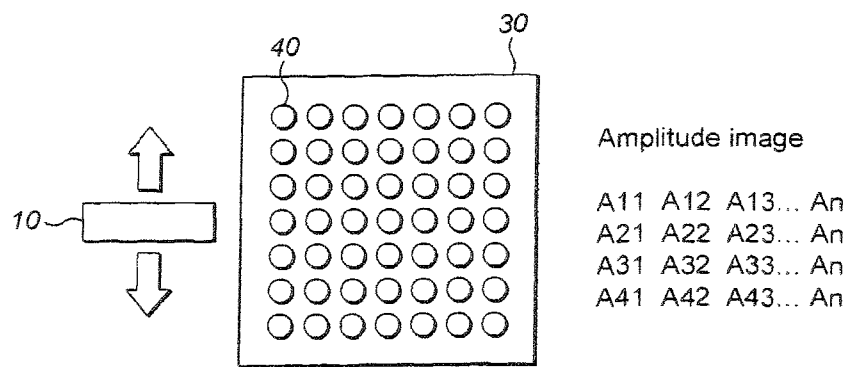


FIG. 2

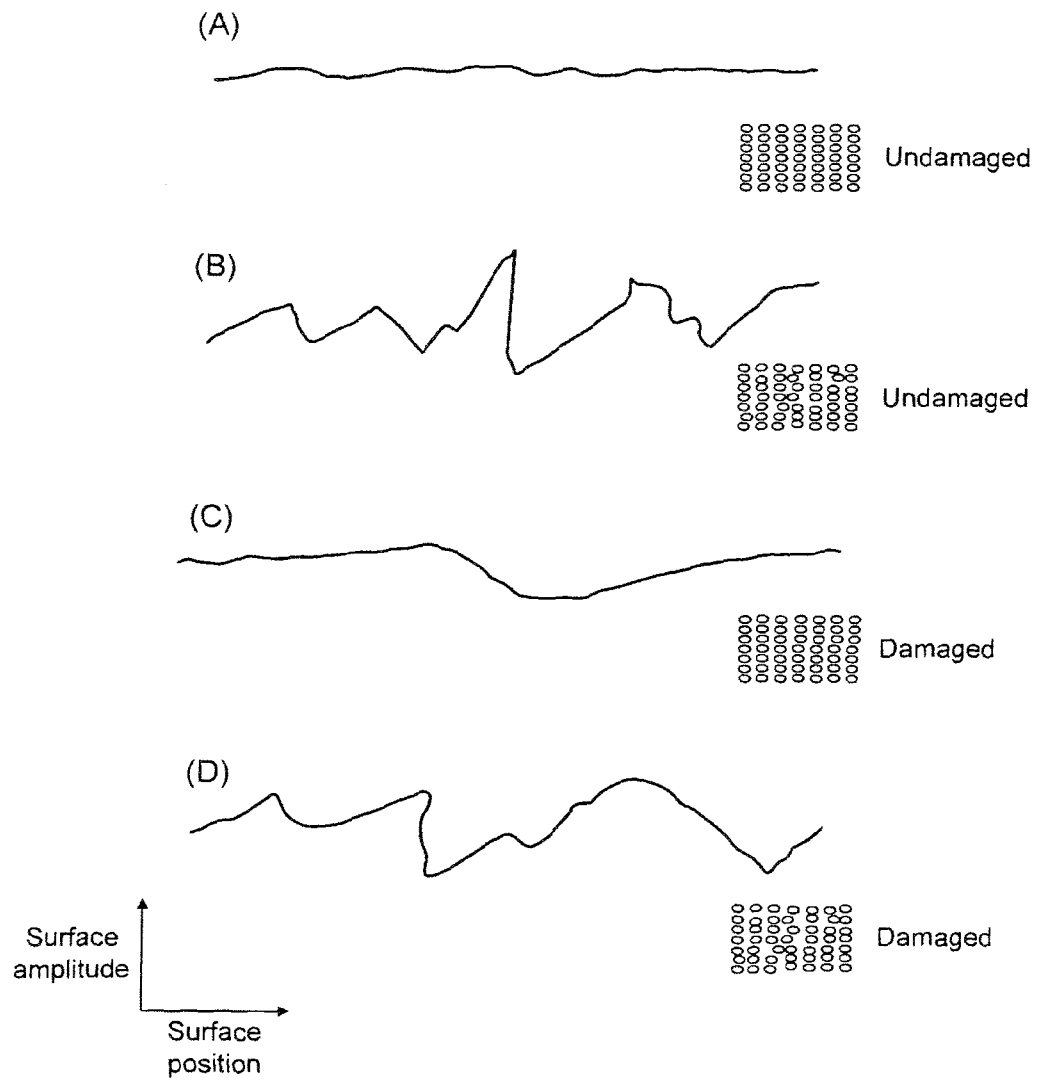


FIG. 3

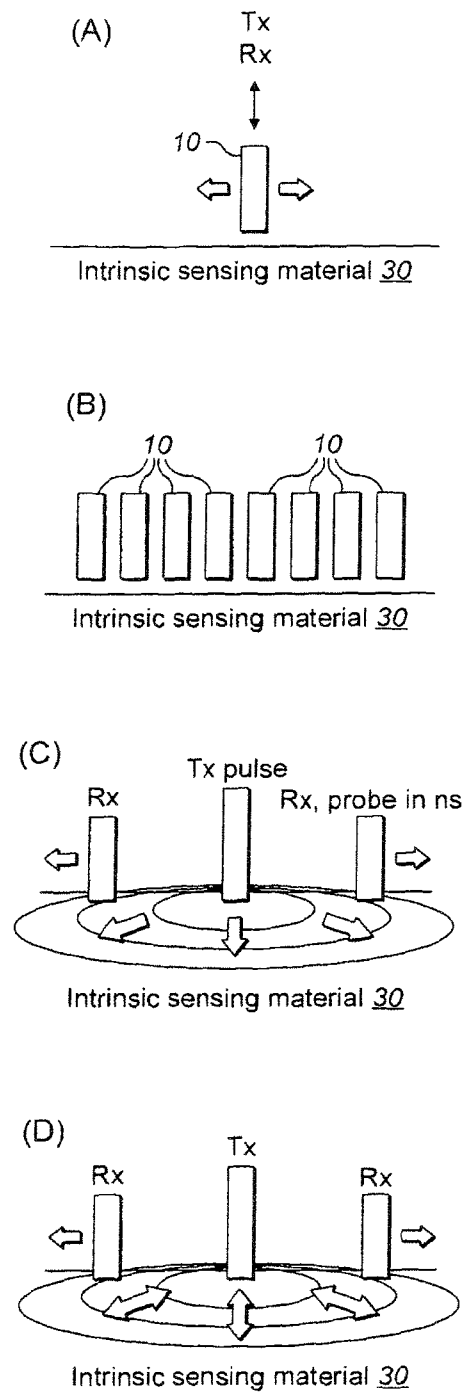


FIG. 4

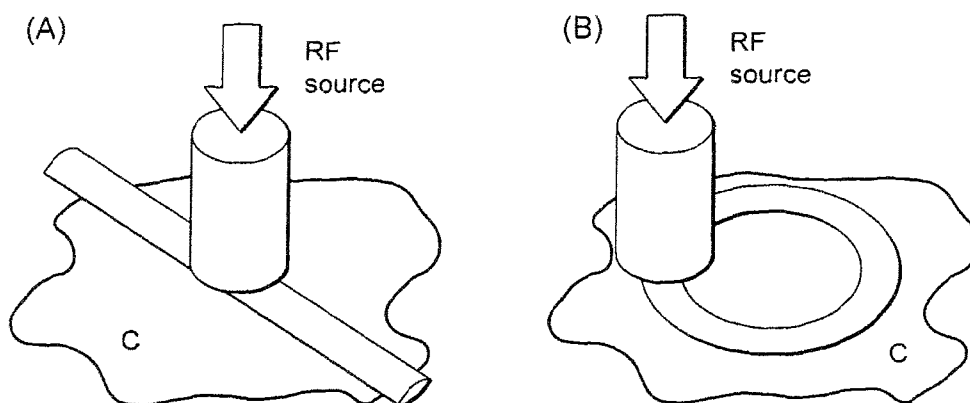


FIG. 5

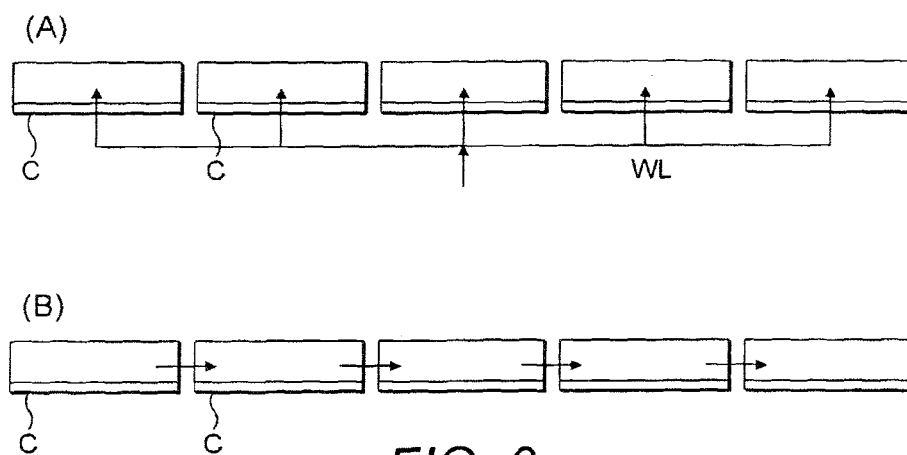
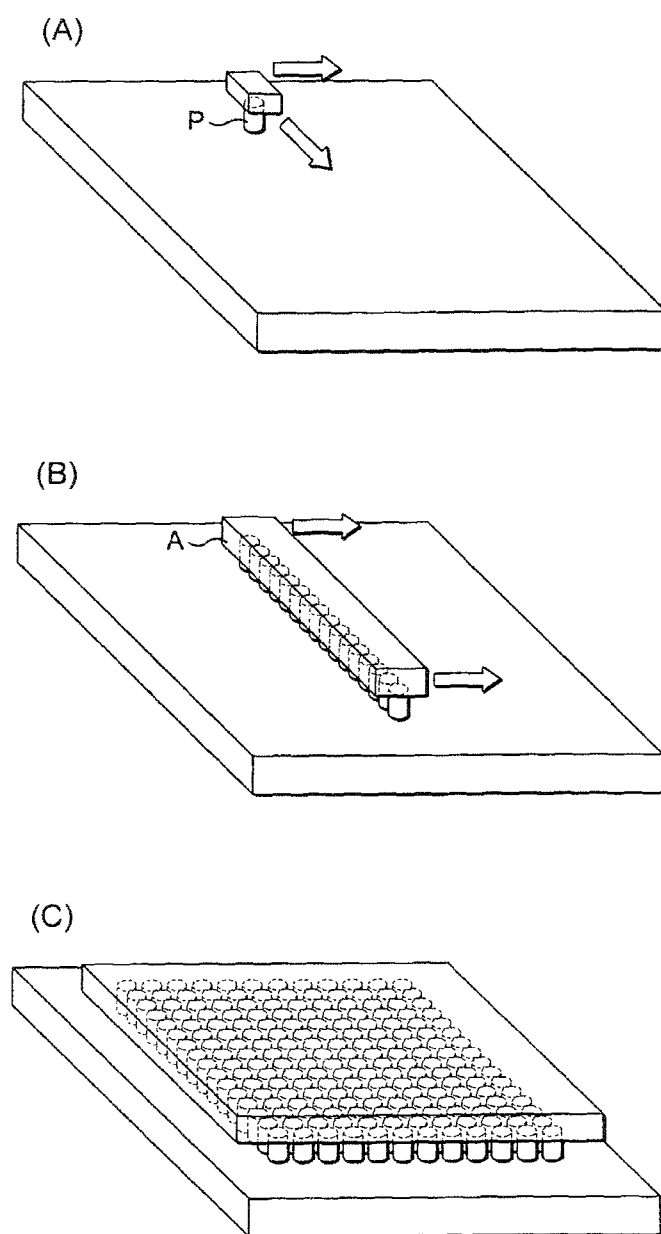


FIG. 6



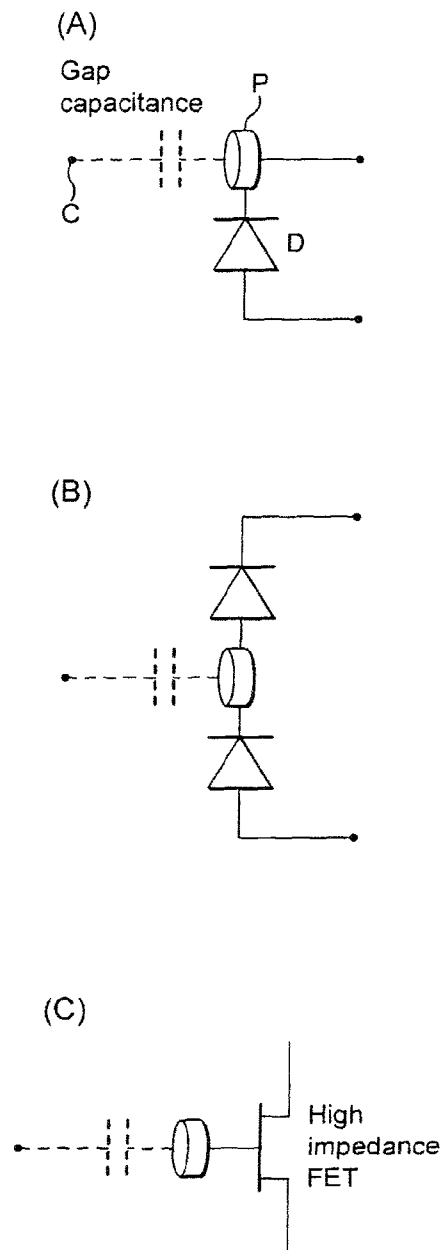
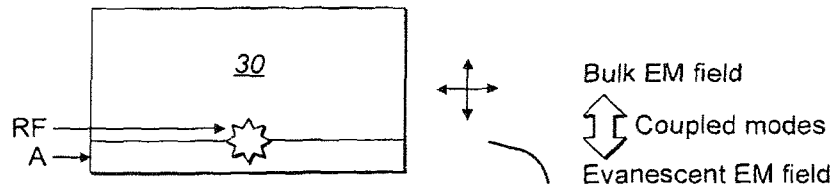
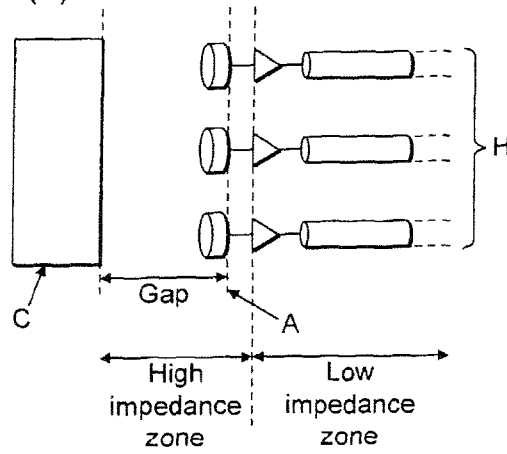


FIG. 8

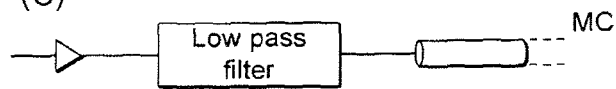
(A)



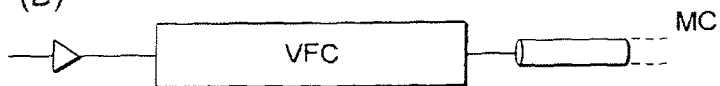
(B)



(C)



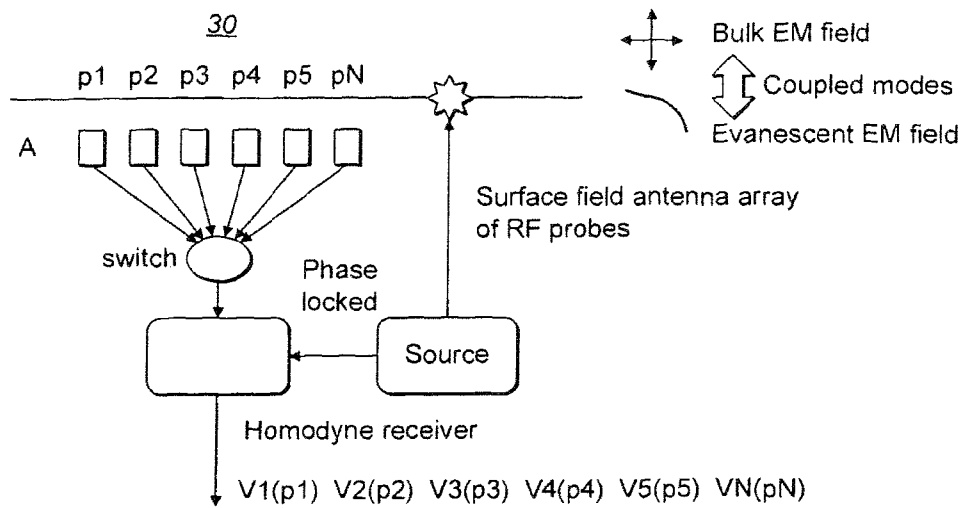
(D)



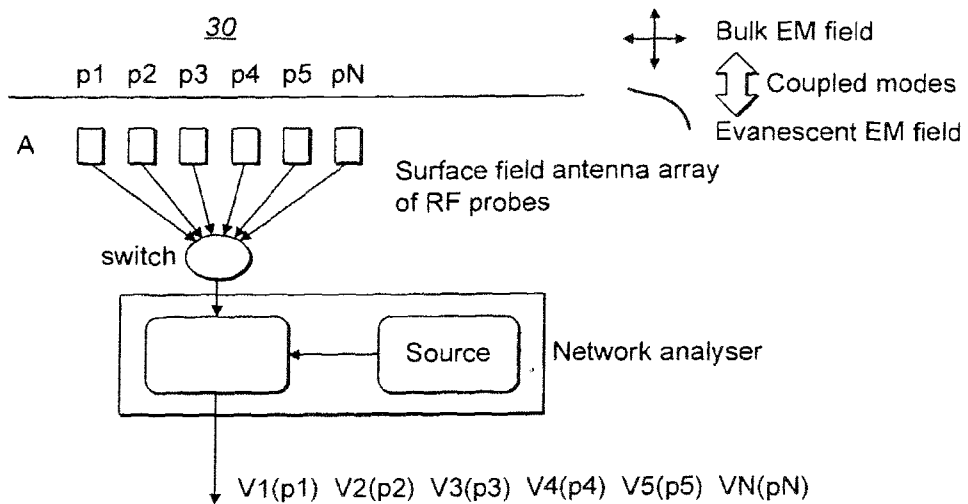
(E)



FIG. 9



Output voltage array to memory:

FIG. 10

Output voltage array to memory:

FIG. 11

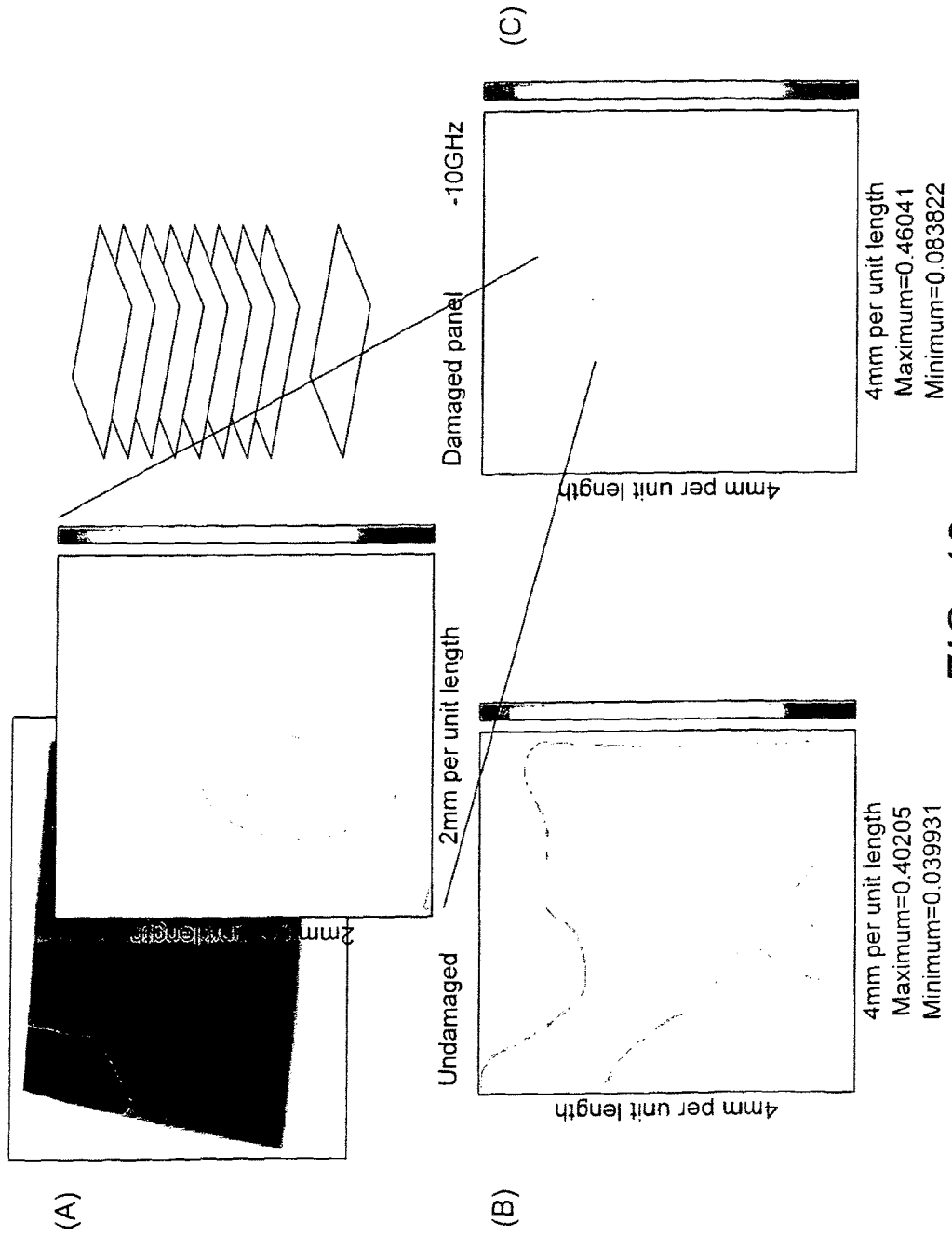
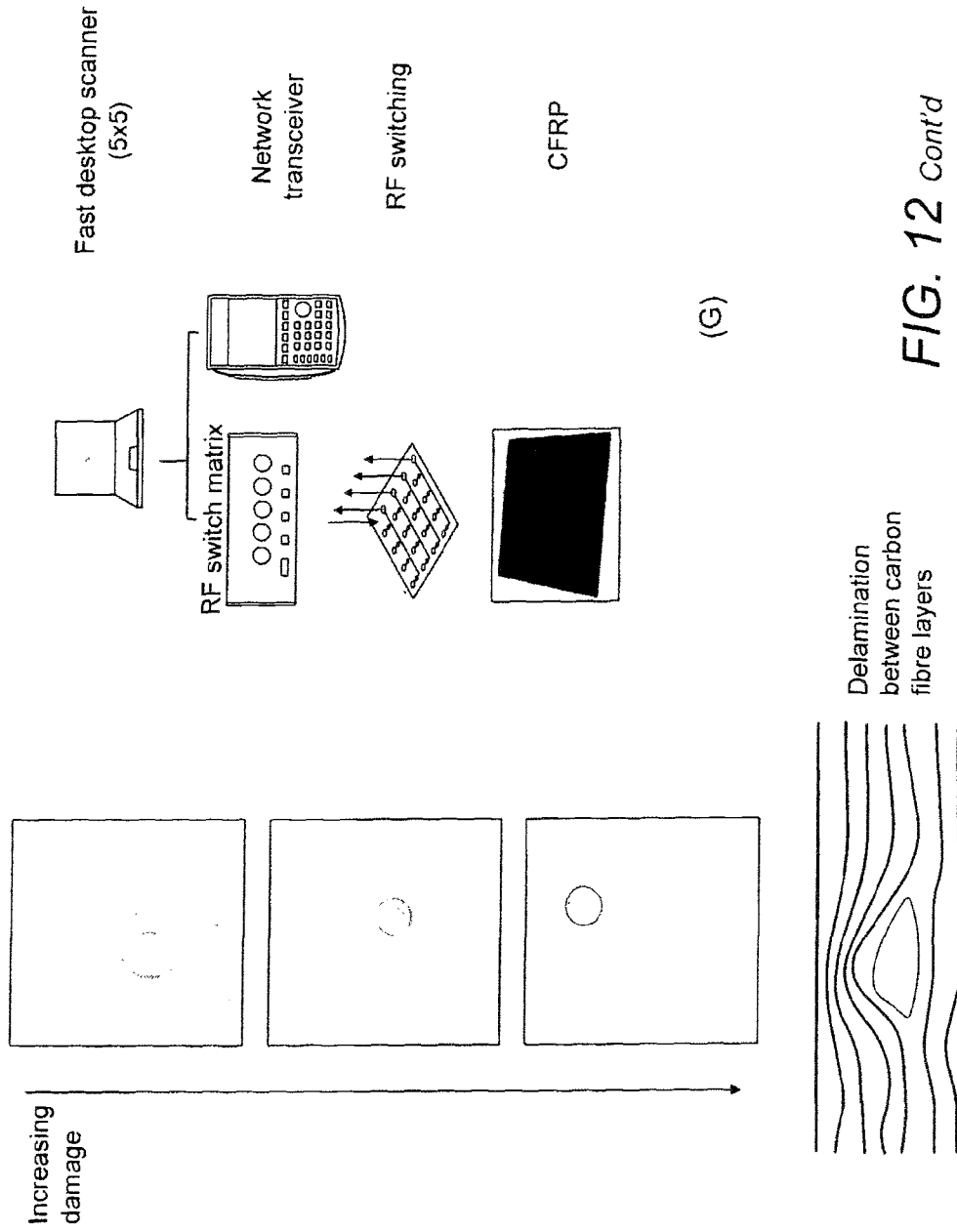


FIG. 12



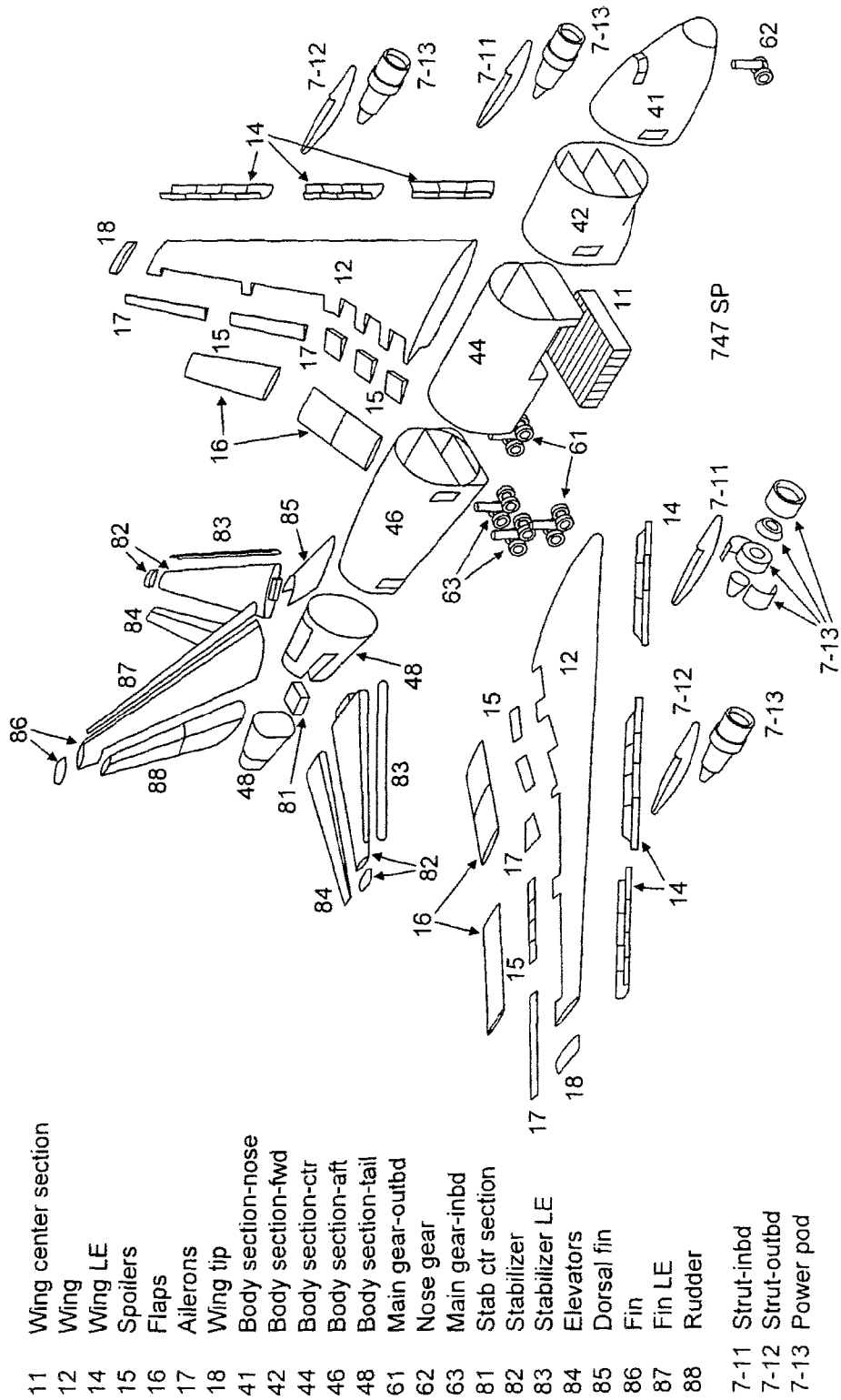
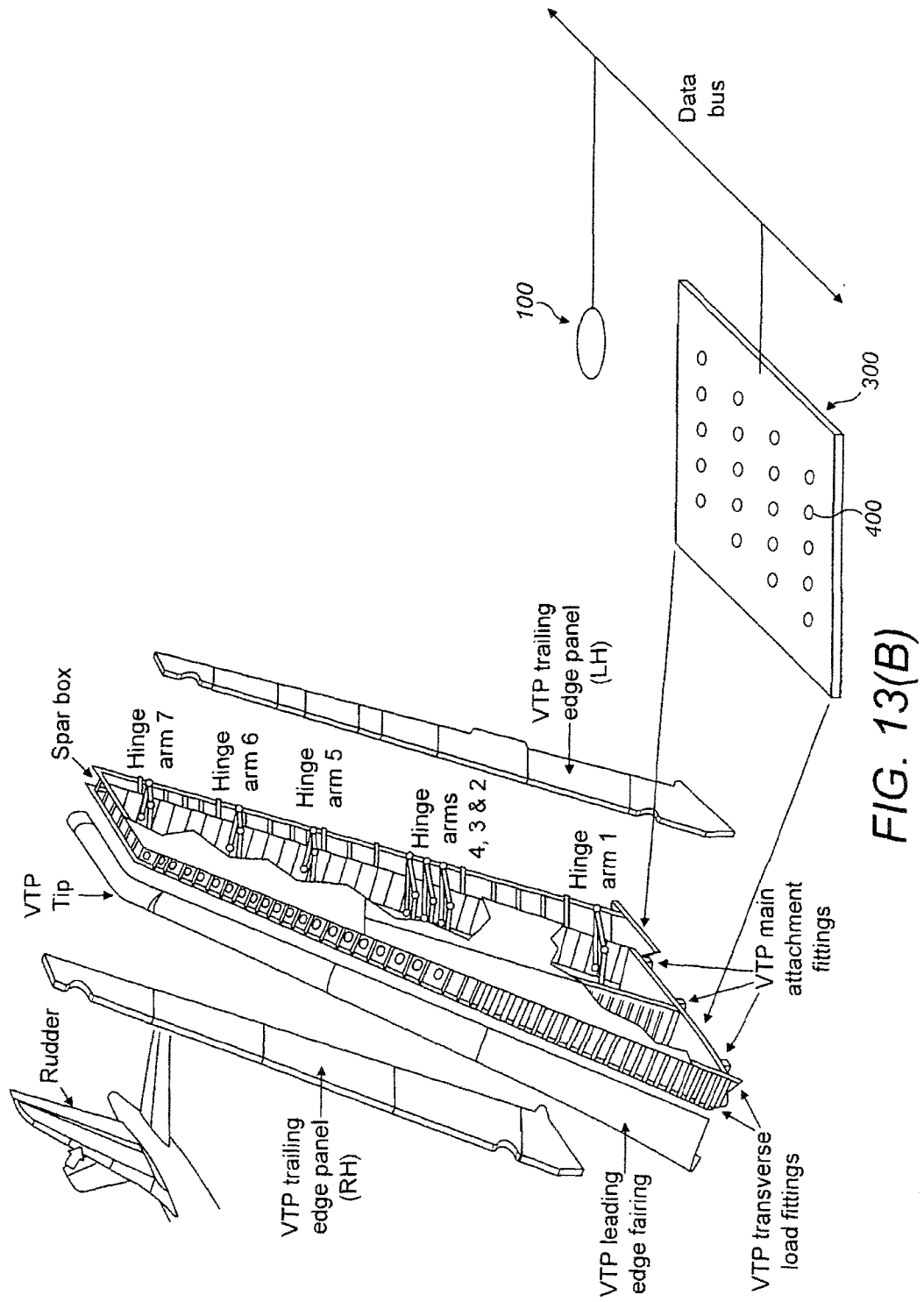


FIG. 13(A)



SA



P

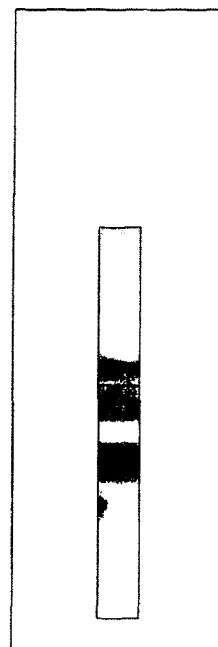
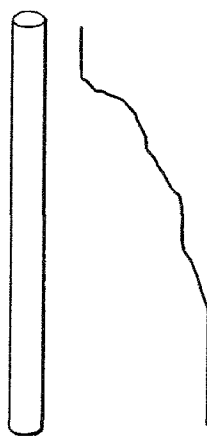


FIG. 14

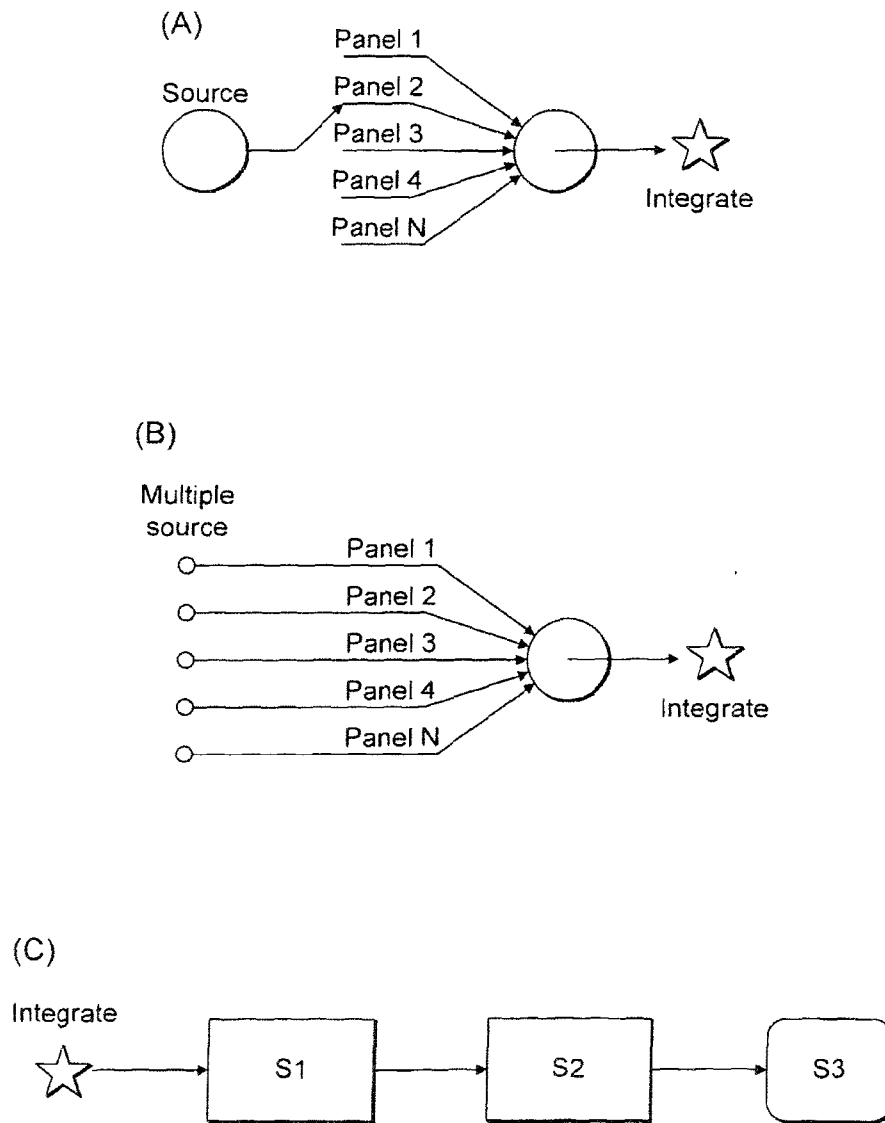


FIG. 15

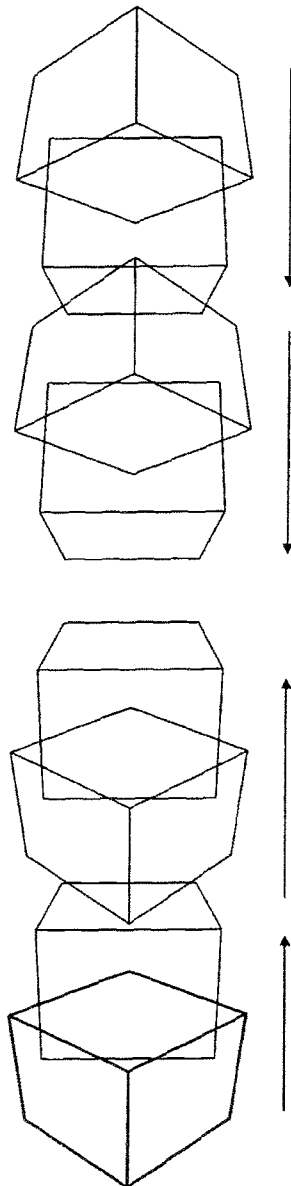


FIG. 16

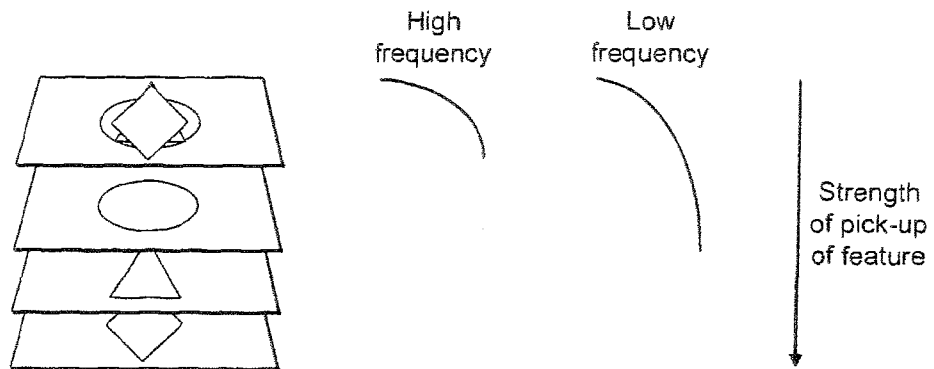


FIG. 17

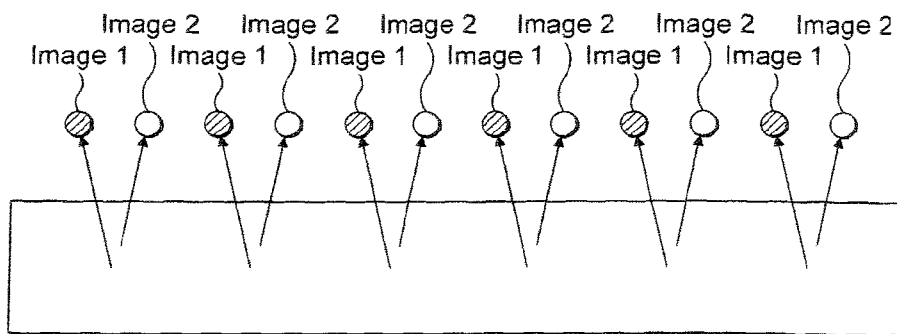


FIG. 18