

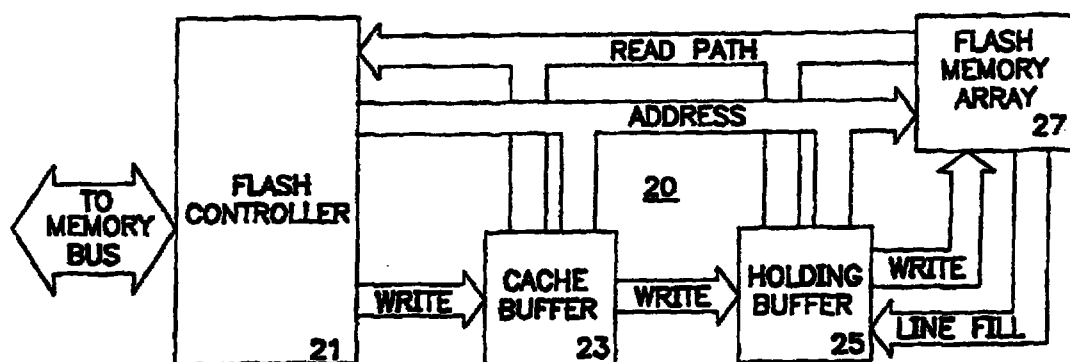
PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : G06F 12/06, 12/00		A1	(11) International Publication Number: WO 97/13204
			(43) International Publication Date: 10 April 1997 (10.04.97)
(21) International Application Number: PCT/US96/15970		(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, (SG) SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).	
(22) International Filing Date: 3 October 1996 (03.10.96)			
(30) Priority Data: 08/538,261 3 October 1995 (03.10.95) US			
(71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).			
(72) Inventors; and (75) Inventors/Applicants (for US only): HASBUN, Robert, N. [US/US]; 4544 Fawn Street, Shingle Springs, CA 95682 (US) FAIZI, Asad [PK/US]; 404 Canyon Terrace Lane, Folsom, CA 95630 (US) LAM, Joann [US/US]; 2170 41st Avenue, San Francisco, CA 94116 (US) RUSCITO, Peter, J. [US/US]; 182 Bayline Circle, Folsom, CA 95630 (US).		Published With international search report.	
(74) Agents: KING, Stephen, L. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).			

(54) Title: FLASH EEPROM MAIN MEMORY IN A COMPUTER SYSTEM



(57) Abstract

A flash EEPROM memory array (27) including a cache buffer (23) for storing lines of data being written to all addresses in main memory (13); a plurality of holding buffers (25) for storing lines of data from the cache buffer (23) addressed to a particular block of addresses in main memory (13); a plurality of blocks of flash EEPROM main memory (27) for storing lines of data from a holding buffer (25) directed to a particular block of addresses in main memory (13); and control circuitry for writing lines of data addressed to a particular block of addresses in main memory (13) from the cache buffer (23) to a holding buffer (25) when the cache buffer (23) fills or a holding buffer (25) limit is reached whichever occurs first, writing valid data from an addressed block of flash memory to lines of the holding buffer not holding valid data written from the cache buffer, erasing the addressed block of flash memory, and writing all of the lines in the holding buffer to the addressed block of flash memory.