

SEMICONDUCTOR APPARATUS AND METHOD FOR FABRICATING THEREOF

FIELD OF THE INVENTION

5 The disclosures made herein relate generally to a semiconductor apparatus, and more particularly to relates to a method for manufacturing a semiconductor apparatus (e.g., gate formation of gate Gallium nitride high-electron-mobility transistor (GaN HEMT) device or the like).

10 BACKGROUND OF THE INVENTION

 Ascribed to the capability of carrying large current and supporting high voltages, Gallium nitride (GaN) semiconductor devices are recognized as the next generation of semiconductor devices suitable for power applications. In order to realize the advantage of the GaN semiconductor device, one of the key factor is
15 device fabrication cost. An Si CMOS fully compatible GaN device fabrication process can enable fast adoption of existing Si CMOS fabrication (Fab), which can bring down the fabrication cost significantly.

Figure 1 illustrates a cross-sectional view of a conventional Gallium Nitride (GaN) Metal-Insulator-Semiconductor High Electron Mobility Transistor
20 (MISHEMT) device (1000a), in accordance with prior art.

Figure 2a to **Figure 2c** illustrate an example fabrication process of a conventional GaN MISHEMT device (1000b), in accordance with prior art.

 Referring to the **Figure 1**, the conventional GaN MISHEMT (1000a) operates based on a conductive two dimensional electron gas (2DEG) layer (106),

which can be modulated by a gate metal contact (114). The 2DEG layer (106) is formed between two epitaxy grown nitride layers (e.g., GaN layer and AlGaN layer) (102 and 104), which have different bandgaps. These two consecutively grown nitride layers (102 and 104) introduce polarization at the interface, which
5 contributes to the formation of the 2DEG layer (106) near the interface of the two layers (102 and 104), specifically in the layer with the narrower band gap.

Further, an external voltage applied on a gate will modulate the band gap bent between two different nitride layers (102 and 104), hence modulating on/off of the 2DEG layer (106), so as to control HEMT transistor turn on or turn off.

10 In the conventional GaN MISHEMT transistor (1000a or 100b), a gate (116) is formed by various metal material as shown in the figure 1. Normally, a metal film re-forms or changes the property when undergo a high temperature (> 600C) thermal process, hence typical GaN MISHEMT process forms an ohmic contact (112) first before forming the transistor gate (116). This will limit the
15 selection of the gate insulator film (110), due to ohmic contact cannot undergo high temperature insulator film deposition.

Referring to Figure 2a to Figure 2c, a conventional GaN MISHEMT fabrication sequence is illustrated. After an isolation region (108) is formed, a gate insulator film (110) have to be deposited first, followed by a formation of the
20 ohmic contact metal (112). Then, a dielectric film (114) is deposited to isolate the ohmic contact metal (112) and subsequent gate metal (116), after that, a high selectivity etching (between the gate insulator film (110) and the dielectric film (114)) process is needed to etch away the gate metal (114) and stop on gate insulator film (110). Subsequently, proper cleaning is needed to minimize etch

damage to the gate insulator film (110) before depositing the gate metal material (114).

SUMMARY OF THE INVENTION

5 The present invention relates to a semiconductor apparatus. The semiconductor apparatus comprises a Gallium nitride (GaN) buffer and an Aluminium gallium nitride (AlGaN) barrier. A two-dimensional electron gas (2DEG) is formed between the GaN buffer and the AlGaN barrier. An isolation region is formed on at least one side portion of the 2DEG, the GaN buffer and the

10 AlGaN barrier. A dielectric film is deposited on a portion of the isolation region and a portion of the AlGaN barrier. A gate insulation film is deposited on the dielectric film. A heavy doped poly silicon (Si) film is deposited on the gate insulation film. The dielectric film is deposited again on the gate insulation film and the heavy doped poly Si film followed by an ohmic contact opening to etch

15 away the dielectric film and the gate insulation film to expose an ohmic contact area. At least one ohmic contact metal is deposited and patterned on a portion of the AlGaN barrier. The at least one ohmic contact metal is deposited and patterned on at least one of a portion of the dielectric film and a portion of the gate insulation film.

20 In an embodiment, the heavy doped Poly Si film enables gate formation in the semiconductor apparatus before an ohmic contact formation process.

 In an embodiment, the gate insulator film and the heavy doped Poly Si film are deposited after the dielectric film is etched away in a gate region of the semiconductor apparatus.

In an embodiment, the gate insulator film and the highly doped Poly Si layer are deposited consecutively, so as to ensure a good interface quality between the gate insulator film and the highly doped poly Si layer.

In an embodiment, the semiconductor apparatus comprises a Gallium
5 nitride high-electron-mobility transistor (GaN HEMT) device and a Gallium Nitride (GaN) Metal-Insulator-Semiconductor High Electron Mobility Transistor (MISHEMT) device.

In an embodiment, the semiconductor apparatus is compatible with an Si CMOS process.

10 The present invention relates to a method for fabricating a semiconductor apparatus. The method includes providing the GaN buffer and an AlGaIn barrier. Further, the method includes forming a 2DEG between the GaN buffer and the AlGaIn barrier. Further, the method includes forming an isolation region on at least one side portion of the 2DEG, the GaN buffer and the AlGaIn barrier.
15 Further, the method includes depositing a dielectric film on a portion of the isolation region and a portion of the AlGaIn barrier. Further, the method includes depositing a gate insulation film on the dielectric film. Further, the method includes depositing a heavy doped poly Si film deposited on the gate insulation film. The dielectric film is deposited again on the gate insulation film and the
20 heavy doped poly Si film followed by an ohmic contact opening to etch away the dielectric film and the gate insulation film to expose an ohmic contact area. Further, the method includes depositing at least one ohmic contact metal and patterning on a portion of the AlGaIn barrier. The at least one ohmic contact metal

is deposited and patterned on at least one of a portion of the dielectric film and a portion of the gate insulation film.

BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

5 The present invention will be fully understood from the detailed description given herein below and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, wherein:

Figure 1 illustrates a cross-sectional view of a conventional GaN
10 MISHEMT device, in accordance with prior art.

Figure 2a to Figure 2c illustrate an example fabrication process of a conventional GaN MISHEMT device, in accordance with prior art.

Figure 3a to Figure 3d illustrate an example fabrication process of a GaN MISHEMT device, in accordance with one embodiment of the present invention.

15 **Figure 4** is an example flow chart illustrating a method for fabricating a GaN MISHEMT device, according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

20 Detailed description of preferred embodiments of the present invention is disclosed herein. It should be understood, however, that the embodiments are merely exemplary of the present invention, which may be embodied in various forms. Therefore, the details disclosed herein are not to be interpreted as limiting, but merely as the basis for the claims and for teaching one skilled in the art of the
25 invention. The numerical data or ranges used in the specification are not to be

construed as limiting. The following detailed description of the preferred embodiments will now be described in accordance with the attached drawings, either individually or in combination.

Accordingly, the embodiment herein is to provide a semiconductor
5 apparatus comprising a GaN buffer and an AlGaN barrier. A 2DEG is formed between the GaN buffer and the AlGaN barrier. An isolation region is formed on at least one side portion of the 2DEG, the GaN buffer and the AlGaN barrier. A dielectric film is deposited on a portion of the isolation region and a portion of the AlGaN barrier. A gate insulation film is deposited on the dielectric film. A heavy
10 doped poly silicon (Si) film is deposited on the gate insulation film. The dielectric film is deposited again on the gate insulation film and the heavy doped poly Si film followed by an ohmic contact opening to etch away the dielectric film and the gate insulation film to expose an ohmic contact area. At least one ohmic contact metal is deposited and patterned on a portion of the AlGaN barrier. The
15 at least one ohmic contact metal is deposited and patterned on at least one of a portion of the dielectric film and a portion of the gate insulation film.

In the conventional methods, a metal film is used to form a transistor gate in a Gallium Nitride (GaN) Metal-Insulator-Semiconductor High Electron Mobility Transistor (MISHEMT). A gate metal is normally formed after
20 source/drain ohmic contact formation due to the concern of high temperature anneal process for ohmic contact formation. In order to do a gate metal-first process, a special gate metal material is needed, which may not be Si CMOS fab compatible. An Si CMOS Fab proven material – Poly Si can be used for GaN MISHEMT gate formation, the Poly Si can be heavily doped to low sheet

resistance, which has similar work function as a metal material. Hence, the proposed method will make GaN MISHEMT process fully compatible with the Si CMOS process.

Based on the proposed method, the gate formation of the semiconductor apparatus can be easily enabled, which helps to minimize high selectivity etch process requirement, improves gate leakage performance and enhances device reliability. The proposed method process is fully compatible with the standard Si CMOS process.

Referring now to the drawings and more particularly to **Figure 3a** through **Figure 4**, where similar reference characters denote corresponding features consistently throughout the figures, there are shown preferred embodiments.

Figure 3a to **Figure 3d** illustrate an example fabrication process of a semiconductor apparatus (3000), in accordance with one embodiment of the present invention. The semiconductor apparatus (3000) can be a Gallium nitride high-electron-mobility transistor (GaN HEMT) device and a GaN MISHEMT device.

Referring to **Figure 3a** to **Figure 3d**, the semiconductor apparatus (3000) includes a 2DEG (106) formed between the GaN buffer (102) and the AlGaN barrier (104). An isolation region (108) is formed on at least one side portion of the 2DEG (106), the GaN buffer (102) and the AlGaN barrier (104). A dielectric film (114) is deposited on a portion of the isolation region (108) and a portion of the AlGaN barrier (104). A gate insulation film (110) is deposited on the dielectric film (114). A heavy doped poly silicon (Si) film (118) is deposited on the gate insulation film (110). The dielectric film (114) is deposited again on the gate

insulation film (110) and the heavy doped poly Si film (118) followed by an ohmic contact opening to etch away the dielectric film (114) and the gate insulation film (110) to expose an ohmic contact area. In an embodiment, the heavy doped Poly Si film (118) enables gate formation in the semiconductor apparatus (3000) before
5 an ohmic contact formation process. The gate insulator film (110) and the heavy doped Poly Si film (118) are deposited after the dielectric film (114) is etched away in a gate region of the semiconductor apparatus (3000).

At least one ohmic contact metal (112) is deposited and patterned on a portion of the AlGa_N barrier (104). The at least one ohmic contact metal (112) is
10 deposited and patterned on at least one of a portion of the dielectric film (114) and a portion of the gate insulation film (110). The gate insulator film (110) and the highly doped Poly Si layer (118) are deposited consecutively, so as to ensure a good interface quality between the gate insulator film (110) and the highly doped poly Si layer (118).

15 The fabrication of the semiconductor apparatus (3000) is compatible with an Si CMOS process. Based on the proposed method, the gate formation of the semiconductor apparatus (3000) can be easily enabled, which helps to minimize high selectivity etch process requirement, improves gate leakage performance and enhances device reliability. The proposed method can be used to eliminate a high
20 selectivity (between the gate insulator film (110) and the dielectric film (114)) etch challenge and potential plasma etch damage to the gate insulator film (110), which improves gate leakage performance and device reliability.

Figure 4 is an example flow chart (S4000) illustrating a method for fabricating the GaN MISHEMT device, according to one embodiment of the

present invention. At S402, the method includes providing the GaN buffer (102) and the AlGaN barrier (104). At S404, the method includes forming the 2DEG (106) between the GaN buffer (102) and the AlGaN barrier (104). At S406, the method includes forming the isolation region (108) on at least one side portion of the 2DEG (106), the GaN buffer (102) and the AlGaN barrier (104). At S408, the method includes depositing the dielectric film (114) on the portion of the isolation region (108) and the portion of the AlGaN barrier (104).

At S410, the method includes depositing the gate insulation film (110) on the dielectric film (114). At S412, the method includes depositing the heavy doped poly Si film (118) deposited on the gate insulation film (110). The dielectric film (114) is deposited again on the gate insulation film (110) and the heavy doped poly Si film (118) followed by an ohmic contact opening to etch away the dielectric film (114) and the gate insulation film (110) to expose an ohmic contact area. At S412, the method includes depositing at least one ohmic contact metal (112) and patterning on a portion of the AlGaN barrier (104). The at least one ohmic contact metal (112) is deposited and patterned on at least one of a portion of the dielectric film (114) and a portion of the gate insulation film (110).

In the conventional methods, a metal film is used to form a transistor gate in a Gallium Nitride (GaN) Metal-Insulator-Semiconductor High Electron Mobility Transistor (MISHEMT). A gate metal is normally formed after source/drain ohmic contact formation due to the concern of high temperature anneal process for ohmic contact formation. In order to do a gate metal-first process, a special gate metal material is needed, which may not be Si CMOS fab compatible. An Si CMOS Fab proven material – Poly Si can be used for GaN

MISHEMT gate formation, the Poly Si can be heavily doped to low sheet resistance, which has similar work function as a metal material. Hence, the proposed method will make the GaN MISHEMT process fully compatible with the Si CMOS process.

- 5 Based on the proposed method, the gate formation of the semiconductor apparatus can be easily enabled, which helps to minimize high selectivity etch process requirement, improves gate leakage performance and enhances device reliability.

10 The proposed method can be used to eliminate a high selectivity (between the gate insulator film (110) and the dielectric film (114)) etch challenge and potential plasma etch damage to gate insulator film (110), which will improve gate leakage performance and device reliability.

15 The terminology used herein is for the purpose of describing particular example embodiments only and is not intended to be limiting. As used herein, the singular forms "a", "an" and "the" may be intended to include the plural forms as well, unless the context clearly indicates otherwise. The terms "comprises", "comprising", "including" and "having" are inclusive and therefore specify the presence of stated features, integers, steps, operations, elements and/or components, but do not preclude the presence or addition of one or more other
20 features, integers, steps, operations, elements, components and/or groups thereof. The method steps, processes and operations described herein are not to be construed as necessarily requiring their performance in the particular order discussed or illustrated, unless specifically identified as an order of performance. It is also to be understood that additional or alternative steps may be employed.

The use of the expression “at least” or “at least one” suggests the use of one or more elements, as the use may be in one of the embodiments to achieve one or more of the desired objects or results.

CLAIMS

We claim:

1. A semiconductor apparatus (3000), comprises:
 - i. a Gallium nitride (GaN) buffer (102);
 - 5 ii. an Aluminum gallium nitride (AlGaN) barrier (104);
 - iii. a two-dimensional electron gas (2DEG) (106) formed between the GaN buffer (102) and the AlGaN barrier (104);
 - iv. an isolation region (108) formed on at least one side portion of the 2DEG (106), the GaN buffer (102) and the AlGaN barrier (104);
 - 10 characterized in that:
 - v. a dielectric film (114) deposited on a portion of the isolation region (108) and a portion of the AlGaN barrier (104);
 - vi. a gate insulation film (110) deposited on the dielectric film (114);
 - vii. a heavy doped poly silicon (Si) film (118) deposited on the gate insulation film (110), wherein the dielectric film (114) is deposited
15 again on the gate insulation film (110) and the heavy doped poly Si film (118) followed by an ohmic contact opening to etch away the dielectric film (114) and the gate insulation film (110) to expose an ohmic contact area; and
 - 20 viii. at least one ohmic contact metal (112) deposited and patterned on a portion of the AlGaN barrier (104), wherein at least one ohmic contact metal (112) is deposited and patterned on at least one of a portion of the dielectric film (114) and a portion of the gate insulation film (110).

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2. The semiconductor apparatus (3000) as claimed in claim 1, wherein the heavy doped Poly Si film (118) enables gate formation in the semiconductor apparatus (3000) before an ohmic contact formation process.
- 5 3. The semiconductor apparatus (3000) as claimed in claim 1, wherein the gate insulator film (110) and the heavy doped Poly Si film (118) are deposited after the dielectric film (114) is etched away in a gate region of the semiconductor apparatus (3000).
- 10 4. The semiconductor apparatus (3000) as claimed in claim 1, wherein the gate insulator film (110) and the highly doped Poly Si layer (118) are deposited consecutively.
- 15 5. The semiconductor apparatus (3000) as claimed in claim 1, wherein semiconductor apparatus (3000) comprises a Gallium nitride high-electron-mobility transistor (GaN HEMT) device and a Gallium Nitride (GaN) Metal-Insulator-Semiconductor High Electron Mobility Transistor (MISHEMT) device.
- 20 6. The semiconductor apparatus (3000) as claimed in claim 1, wherein the fabrication of the semiconductor apparatus (3000) is compatible with a Si CMOS process.
7. A method for fabricating a semiconductor apparatus (3000), comprises:

- i. providing a Gallium nitride (GaN) buffer (102) and an Aluminum gallium nitride (AlGaN) barrier (104);
 - ii. forming a two-dimensional electron gas (2DEG) (106) between the GaN buffer (102) and the AlGaN barrier (104);
 - 5 iii. forming an isolation region (108) on at least one side portion of the 2DEG (106), the GaN buffer (102) and the AlGaN barrier (104);
- characterized in that:
- iv. depositing a dielectric film (114) on a portion of the isolation region
10 (108) and a portion of the AlGaN barrier (104);
 - v. depositing a gate insulation film (110) on the dielectric film (114);
 - vi. a heavy doped poly silicon (Si) film (118) deposited on the gate insulation film (110), wherein the dielectric film (114) is deposited again on the gate insulation film (110) and the heavy doped poly
15 Si film (118) followed by an ohmic contact opening to etch away the dielectric film (114) and the gate insulation film (110) to expose an ohmic contact area; and
 - vii. depositing at least one ohmic contact metal (112) and patterning on a portion of the AlGaN barrier (104), wherein at least one ohmic
20 contact metal (112) is deposited and patterned on at least one of a portion of the dielectric film (114) and a portion of the gate insulation film (110).

8. The method as claimed in claim 7, wherein the heavy doped Poly Si film (118) enables gate formation in the semiconductor apparatus (3000) before an ohmic contact formation process.
- 5 9. The method as claimed in claim 7, wherein the gate insulator film (110) and the heavy doped Poly Si film (118) are deposited after the dielectric film (114) is etched away in a gate region of the semiconductor apparatus (3000).
- 10 10. The method as claimed in claim 7, wherein the gate insulator film (110) and the highly doped Poly Si layer (118) are deposited consecutively.
- 15 11. The method as claimed in claim 7, wherein semiconductor apparatus (3000) comprises a Gallium nitride high-electron-mobility transistor (GaN HEMT) device and a Gallium Nitride (GaN) Metal-Insulator-Semiconductor High Electron Mobility Transistor (MISHEMT) device.
12. The method as claimed in claim 7, wherein the fabrication of the semiconductor apparatus (3000) is compatible with an Si CMOS process.