

A RECTIFIER

Background of the Invention

The present invention relates to a rectifier for use in a communications device, and in particular to a
5 rectifier suitable for use in wireless communications devices such as RFID tags.

Description of the Prior Art

Wireless communication using devices such as transponders or RFID (Radio Frequency Identifier) tags (hereinafter referred to generally as "tags"), is achieved by having the tag receive a carrier
10 signal from a device generally known as an interrogator. The modulation of the signal by the interrogator allows data to be transferred from the interrogator to the tag. In addition to this, the tag often has the ability to further modulate the signal received from the interrogator, thereby allowing data to be transferred back from the tag to the interrogator.

15 This allows the tags to be used for example as identifier tags for products or the like. In this case, the tag is programmed with information regarding the product, such as the nature of the product, date of creation, or the like. The interrogator can then read this information from the tag at a later time, allowing the product to be uniquely identified. This is particularly useful, as the interrogator need not be directly adjacent to the tag, allowing the interrogator to determine the nature of products
20 from a distance.

In applications of this form, the tags are usually adapted to be both portable and as small as possible, thereby allowing the tags to be fixed to the outside of packaging, or the like. Accordingly, it is important to ensure that the power consumption of the tags is minimised as much as possible.
25 This helps prevent failure of the wireless communication due to exhausted batteries, or the like.

In order to save power, it is known to produce tags in which only portion of the tags internal circuitry is driven by batteries. In this case, the remaining circuitry, such as the RF circuitry, obtains its power from the carrier signal generated by the interrogator. Devices of this form are
30 known as semi-passive devices. Similarly, it is also possible to produce passive devices in which all the circuitry is powered by the carrier signal, thereby overcoming the need for any additional power source.

Passive and semi-passive devices of this form can be miniaturised to a large degree, allowing tags to
35 be created that are equivalent in size to a button or coin, allowing the tags to be attached to objects as described above.

An example of a passive transceiver is shown in Figure 1.

As shown, the passive transceiver is formed from an antenna 11 coupled to a power supply rectifier 13 via a matching network 12. The matching network 12 is also coupled to a
5 modulator/demodulator 14 formed from a second rectifier, which is in turn coupled to a pulse shaping circuit 16. In addition to this, the power supply rectifier 13, the modulator/demodulator 14 and the pulse shaping unit 16 are coupled to an MCU (Micro Control Unit) 15 as shown.

In use the tag operates in two different modes, namely interrogator-transmission, when the
10 interrogator transfers data to the tag, and in tag-transmission, when the tag transfers data to the interrogator.

In tag-transmission mode, the transceiver is adapted to receive a carrier signal from an interrogator via the antenna 11. The carrier signal is then modulated by the tag to allow data to be transferred to
15 the interrogator. In contrast in the interrogator-transmission mode, the interrogator modulates the carrier signal with a modulating signal, such that the tag receives a modulated signal, the modulation representing the data to be transferred to the tag.

In interrogator-transmission mode the modulated signal is received by the tag and transferred to the
20 power supply rectifier 13 and the modulator/demodulator 14 via the matching network 12, which operates to match the impedance of the antenna with that of the power supply rectifier 13 and the modulator/demodulator 14. The power supply rectifier 13 rectifies the received modulated signal to generate a power to supply Vcc, which is transferred to the MCU 15, whilst the modulator/demodulator 14 rectifies the received modulated signal to recover the modulating signal.

25 The pulse shaping circuit 16 reshapes the modulating signal and transfers the reshaped signal to the MCU 15. This allows the MCU 15 to determine any data transferred to the passive transceiver in the modulated signal.

30 In tag-transmission mode, the MCU 15 can also transfer data to the modulator/demodulator 14 from the data output. The modulator/demodulator 14 then modulates the carrier signal received from the interrogator in accordance with the data. This allows data to be transferred from the passive transceiver to an associated interrogator in a process known as backscatter modulation.

35 It will be appreciated that as the system operates half-duplex communication, is not possible for both the tag and the interrogator to transmit data simultaneously. Accordingly, the tag can only transmit data to the interrogator when the tag receives a carrier signal (i.e. a signal that has not been

modulated by the interrogator).

As the demodulator 14 is similar to power supply rectifier 13, the circuits can be combined. An example of a rectifier incorporating this arrangement is shown in Figure 2.

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As shown in this example, the matching network 12 is coupled to a single rectification circuit 19. The rectification circuit 19 is then coupled to the MCU 15 via a pulse shaping circuit 16, a voltage regulator 22 and a modulator 20. Operation of the circuit is substantially similar to the circuit described above with respect to Figure 1 and will therefore not be described in further detail.

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In comparison with traditional receivers that use low noise amplifiers to increase sensitivity, a passive receiver has rather poor sensitivity. This is primarily because the circuitry is made very basic to reduce power consumption and cost. Furthermore, in passive transceivers, the transceiver has to generate additional power to supply digital circuits as well as the RF circuits.

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The power available to a receiver is governed by the equations:

$$P_r = P_t \times G_t \times G_r \times \left(\frac{\lambda}{4\pi D} \right)^2 \times \frac{1}{L}$$

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$$D = \sqrt{\frac{P_t \times G_t \times G_r}{P_r}} \times \frac{\lambda}{4\pi} \times \sqrt{\frac{1}{L}}$$

Where:

P_r = receiver power

D = operating range

P_t = transmission power

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G_t = transmitter antenna gain

P_r = receiving power

G_r = receiver antenna gain

λ = wavelength

L = signal losses (including polarity loss, matching loss, antenna directivity loss)

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The available power for the receiver P_r is proportional to transmission power P_t and the receiver antenna gain G_r . Similarly the power is inversely proportional to D^2 . The available power therefore decreases rapidly as the distance increase.

Accordingly, the field strength of the signal received at the antenna has to be sufficient to allow the received signal to be processed, as well as to allow data to be transmitted back to the interrogator restored and subsequently processed. As a result, a given strength of carrier signal will result in a given operating range for the receiver.

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In the case of the circuit of Figure 1 operating to receiver data from an interrogator, the antenna generates a signal modulated as shown in Figure 3. The waveform of the rectified signal generated by the modulator/demodulator 14 is shown in Figure 4. Figure 5 shows the waveform of the signal generated by the power supply rectifier.

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In this case, in order to generate data having an amplitude of V_{cc} , the amplitude of the received signal at 33, 35 will have to be at least V_p , where $V_p > V_{cc}/2$. In this case, the rectified signal must power the MCU and allow the RF signal to be demodulated.

15 In the case of the circuit operating to the transmit data to the interrogator, additional power is required to send data back to the interrogator. Instead of radiating its own RF waves to transmit data, the circuit modulates the incoming carrier wave. The manner in which this is achieved will depend on the particular implementation and the operating frequency of the system.

20 For low frequencies, the circuit switching results in a variation in the load of the antenna, which in turn causes variation of voltage amplitude of signal induced antenna. For instance, a short circuit draws more current and therefore absorbs more power from the antenna, so the voltage is therefore reduced.

25 As for high frequencies variation of load will result in variation of the impedance at input port of matching network, which causes a change of reflection. In comparison to this, at low frequencies, when the impedance of antenna port is 100% conjugated match with that of input port of matching network, there is no reflection taking place, and the entire instant wave will be delivered to circuit.

30 The power reflected increases with impedance miss-matching, with the extreme case occurring when the circuit is the short or open circuit at the port such that all the instant power is reflected. Therefore, in high frequencies, the antenna normally matches the circuit properly. However, when short circuit take place in the rectification circuit the impedance matching at the antenna port will become worse, which result in reflection of the carrier wave.

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The interrogator will sense the reflection allowing the data to be back scattered. During the reflection the power entering the circuit reduces. Furthermore, short circuit will discharge the

current previously stored in capacitor, and thus the circuit requires time to recover after the short circuit is over. To overcome this problem a switch can be made at the matching network by introducing a reactance component such as capacitor or inductor so that the bias condition will not change during reflection time.

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As a result, the tag requires additional power to transmit data to the interrogator, thus further reducing the operating range of the tags.

10 Solutions to this problem include:

- 1) Increase the transmission power of the interrogator
- 2) Increase the antenna gain of the tag
- 3) Reduce the power consumption and operating voltage of the tag
- 4) Increase the sensitivity of interrogators

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The maximum transmission power is limited by regulations that vary from region to region, and these are therefore limited.

It is effective to improve range by increasing the gain of the tag antenna. However, the antenna is typically small, simple and inexpensive, thereby limiting the practical gain that can be obtained. Trade-off has to be made among performance (including gain and bandwidth), size and cost of material,

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Decreasing the power consumption of the tag will increase the range. However, the effect is again limited by the fact that the power consumption is generally very low and can only be limited to a certain degree. This again places an effective limit on the improvements that can be obtained.

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In the case of improving the sensitivity of the interrogator, the magnitude of the modulation need not be as great as the modulation used to transmit data from the interrogator to the tag. An example of this is shown in Figure 6. In this example, the modulation of the signal between the points 37, 38, 39, 40 is lower than the depth of modulation than the signal shown in Figure 3 at 33, 34, 35, 36.

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However, it is usually difficult to improve the sensitivity of a receiver when both the receiver and transmitter have to work simultaneously as in the case of interrogators that communicate with passive transponders. In particular, the transmitter and receiver are generally connected to a single antenna via a coupler. In use, the coupler is adapted to ensure that the isolation between the transmission and reception channels is as high as possible. However, as the transmission power is

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generally a few thousand times higher than the reception power, then if even a small proportion of the transmission channel couples to the reception channel, then this can interfere with or even completely saturate the receiving channel. As complete isolation of the channels by the coupler is impossible, it is therefore necessary to ensure the received signal is stronger than any interference
5 created by the transmission channel.

The techniques outlined above allow the operating range to be improved to a certain degree. However, additional increases in operating range require improved levels of rectified voltage generated in the tag, together with improved levels of backscatter modulation.

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US-A-6,140,924 shows an example of prior one system in which a diode rectifier is provided that also acts as a voltage doubler coupled to a single antenna port. However, doubling the voltage only leads to a certain degree of improvement.

15 However, a major problem with rectifiers of this form is that the response of the rectifier is non-linear. This causes problems in the generation of harmonics within the circuit, as well as causing difficulties in matching the impedance of the rectifier to the antenna. This is highlighted by the fact that in addition to the impedance matching circuit, the system of US-A-6,140,924 also requires the presence of an external capacitor, the value of which must be selected to tune the response of the
20 circuit.

A further proposed solution for two port antennas, is for each port to connect to a respective voltage doubler as described in US-A-6,140,924. The two output voltages of the voltage doublers can be superposed to generate a voltage that is approximately 4 times as high as input peak. However,
25 such an arrangement generally has a number of drawbacks. Firstly, dual port antennas are difficult to design. Secondly, the solution is not applicable to antennae such as patch antennae where each port consists of a terminal and ground pin, in which case the voltage cannot be superposed. Thirdly, the amplitude of the signal at each port is reduced as compared to that of single port antenna. For instance, a loop is cut to have two ports at different places, such that the conductor of the loop is cut
30 into two pieces. The gain for each port is reduces due to effect on current flow through the loop conductor.

Summary of the Present Invention

In a first broad form the present invention provides a rectifier for use in a communications device,
35 the device being adapted to receive a signal from an interrogator device via an antenna, the rectifier including:

- a) First and second input terminals coupled to the antenna for receiving the signal, one of the input terminals forming a voltage reference;
- b) First and second output terminals;
- c) A first clamping circuit coupled to at least one of the input terminals and the voltage reference, the first clamping circuit being adapted to generate a first clamped signal at a first terminal;
- d) A first peak rectifier coupled to the first terminal and at least the first output terminal, the first peak rectifier being adapted to rectify the first clamped signal to generate a first rectified signal at the first output terminal with respect to voltage reference;
- e) A second clamping circuit coupled to at least one of the input terminals and the voltage reference, the second clamping circuit being adapted to generate a second clamped signal at a second terminal; and,
- f) A second peak rectifier coupled to the second terminal and at least the second output terminal, the second peak rectifier being adapted to rectify the second clamped signal to generate a second rectified signal at the second output terminal with respect to voltage reference.

In use, the first and second input terminals of the rectifier are preferably coupled to the antenna via an impedance matching circuit.

The second input terminal may form the voltage reference. In this case, the signal typically has a magnitude V_p , with the first clamping circuit being coupled to the first input terminal such that the first clamped signal has a magnitude substantially equal to $2V_p$.

- The second clamping circuit is typically coupled to the first input terminal such that the second clamped signal has a magnitude substantially equal to $-V_p$.

In this case, the rectifier can be adapted to provide a modulated signal or DC voltage having a magnitude of substantially $3V_p$.

Generally:

- a) The first clamping circuit includes:
 - i) A first capacitor coupled to the first input terminal and the first terminal; and,
 - ii) A first diode having a cathode terminal coupled to the first terminal and an anode terminal coupled to the second input;
- b) The first peak rectifier includes:
 - i) A second capacitor coupled to the first and second output terminals; and,

- ii) A second diode having a cathode terminal coupled to the first output terminal and an anode terminal coupled to the first terminal;
- c) The second clamping circuit includes:
 - i) A third capacitor coupled to the second input terminal and the second terminal; and,
 - 5 ii) A third diode having a cathode terminal coupled to the first input terminal and an anode terminal coupled to the second terminal; and,
- d) The second peak rectifier includes:
 - i) The second capacitor coupled to the first and second output terminals; and,
 - 10 ii) A fourth diode having a cathode terminal coupled to the second terminal and an anode terminal coupled to the second output terminal.

The rectifier can be adapted to further modulate the received carrier signal, the rectifier including a switching circuit connected in parallel with the second capacitor, the switching circuit being adapted to control the modulation of the received signal in accordance with a modulating signal
15 received from a controller. In this case, the controller may be an MCU, or other appropriate digital circuit, adapted to provide data for modulating the received signal.

The rectifier may also include third and fourth input terminals.

- 20 In this case, the third and fourth input terminals are coupled to the antenna via a respective impedance matching circuit.

The third input terminal may be coupled to the second to thereby form the voltage reference, in which case the second clamping circuit may be coupled to the fourth input terminal such that the
25 second clamped signal has a magnitude substantially equal to $-2V_p$.

In this case, the rectifier can be adapted to provide a modulated signal or DC voltage having a magnitude of substantially $4V_p$.

30 Generally:

- a) The first clamping circuit includes:
 - i) A first capacitor coupled to the first input terminal and the first terminal; and,
 - ii) A first diode having a cathode terminal coupled to the first terminal and an anode terminal coupled to the voltage reference;
- 35 b) The first peak rectifier includes:
 - i) A second capacitor coupled to the first output terminal and the voltage reference; and,

- ii) A second diode having a cathode terminal coupled to the first output terminal and an anode terminal coupled to the first terminal;
- c) The second clamping circuit includes:
 - i) A third capacitor coupled to the fourth input terminal and the second terminal; and,
 - 5 ii) A third diode having a cathode terminal coupled to the voltage reference and an anode terminal coupled to the second terminal; and,
- d) The second peak rectifier includes:
 - i) A fourth capacitor coupled to the second output terminal and the voltage reference; and,
 - 10 ii) A fourth diode having a cathode terminal coupled to the second terminal and an anode terminal coupled to the second output terminal.

The rectifier may include a fifth capacitor connected to the output terminals.

15 The fourth input terminal may be coupled to the first input, such that the first, second third and fourth input terminals are coupled to the antenna via a single matching circuit.

The rectifier may further include a switching circuit connected in parallel with either or both of the second and fourth capacitors, the switching circuit being adapted to control the modulation of the received signal in accordance with a modulating signal received from a controller.

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In this case, the controller can be adapted to receive data and modulate the received signal in accordance with received data. The data is typically received from a data store, although other data sources may be used. As mentioned above, the controller may be an MCU, or other appropriate digital circuit, adapted to provide data for modulating the received signal.

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In a second broad form the present invention provides a communications device for use in a wireless communications system, the system including an interrogator adapted to generate a signal, the device being adapted to communicate with the interrogator via the signal, the device including:

- a) An antenna for receiving the signal;
- 30 b) A rectifier coupled to the antenna to receive the signal, the received signal having a magnitude V_p , the rectifier being adapted to perform at least one of:
 - i) Rectify the signal to generate a power supply signal, the power supply signal having a magnitude of at least $3V_p$; and,
 - ii) Demodulate the signal to generate a demodulated signal, the demodulated signal having
- 35 a magnitude of at least $3V_p$.

In this case, the rectifier can be further adapted to modulate the received signal.

The communications device may therefore be a passive or semi passive RFID Tag. Although the communications device may also be another form of communications device.

- 5 The rectifier is preferably a rectifier according to the first broad form of the invention.

The term signal refers to either the carrier signal or the modulated signal depending on whether the communications device is in receiving or transmission mode.

10 **Brief Description of the Drawings**

An example of the present invention will now be described with reference to the accompanying drawings, in which: -

- Figure 1 is a block diagram of a first example of a passive transponder;
- 15 Figure 2 is a block diagram of a second example of a passive transponder;
- Figure 3 is an example of the RF signal induced by the antenna in the circuit of Figure 1;
- Figure 4 is an example of the waveform generated by the modulator/demodulator of Figure 1;
- Figure 5 is an example of the waveform generated by the rectifier power supply of Figure 1;
- Figure 6 is an example of the waveform of backscatter modulated signal;
- 20 Figure 7A is a first example of a rectifier according to the present invention;
- Figure 7B is an example of the equivalent circuit of the circuit of Figure 7A for positive half cycles;
- Figure 7C is an example of the equivalent circuit of the circuit of Figure 7A for negative half cycles;
- Figure 7D is an example of the waveform generated at the first terminal of the rectifier of Figure
- 25 7A;
- Figure 8A is a second example of a rectifier according to the present invention;
- Figure 8B is an example of the waveform of the up-clamped signal in the rectifier of Figure 8A;
- Figure 8C is an example of the waveform of the down-clamped signal in the rectifier of Figure 8A;
- Figure 9A is a third example of a rectifier according to the present invention;
- 30 Figure 9B is an example of the equivalent circuit of the circuit of Figure 9A for positive half cycles;
- and,
- Figure 9C is an example of the equivalent circuit of the circuit of Figure 9A for negative half cycles.

Detailed Description of the Preferred Embodiments

- 35 An example of a rectifier according to the present invention will now be described with reference to Figure 7A.

As shown in Figure 7A, the rectifier shown generally at 100 is coupled to an antenna port 101 via a matching network 102. The rectifier includes first and second input terminals 121, 126 that are coupled to respective output terminals of the matching circuit, as shown. In this configuration, the second input terminal 126 acts as the ground.

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The rectifier also includes first and second output terminals 123, 124, which in use would be coupled to subsequent circuitry depending on the specific use of the rectifier. It will be appreciated from the above, that these outputs are therefore usually coupled to an MCU, or the like.

10 In any event, the rectifier is formed from:

- A first clamping circuit including a first capacitor 111 coupled to the first input terminal 121, and a first terminal 122, and a first diode 113 having a cathode terminal coupled to the first terminal 122 and an anode terminal coupled to the second input terminal 126;
- A first peak rectifier including a second capacitor 117 coupled to the first and second output terminals 123, 124 and a second diode 112 having a cathode terminal coupled to the first output terminal 123 and an anode terminal coupled to the first terminal 122;
- A second clamping circuit including a third capacitor 114 coupled to the second input terminal 126, and a second terminal 125, and a third diode 115 having a cathode terminal coupled to the first input terminal 121 and an anode terminal coupled to the second terminal 125; and,
- 20 • A second peak rectifier including the second capacitor 117 coupled to the first and second output terminals 123, 124 and a fourth diode 116 having a cathode terminal coupled to the second terminal 125 and an anode terminal coupled to the second output terminal 124.

25 In use, the RF signal (formed from the combined carrier and the RF modulating signals) received by the antenna induces an alternating voltage that is applied to the rectifier 100 through the port 101 and the matching network 102. This configuration allows the rectifier to provide power supply or demodulated signals having a voltage or amplitude approximately three times as large as the peak voltage or amplitude of the RF signal induced at the antenna port 101.

30 The manner in which this is achieved will now be described with reference to Figures 7B and 7C. In particular, it will be appreciated that as the signal supplied to the input terminals 121, 126 is a sinusoidal signal, the response of the rectifier will differ between positive and negative half cycles. Accordingly, the response of the rectifier in positive and negative half cycles will be described with reference to the equivalent circuits shown in Figures 7B and 7C respectively.

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As shown in Figure 7B, in positive half cycles, the current flows through a loop formed from the first capacitor 111, the second diode 112, the second capacitor 117, the fourth diode 116 and the

third capacitor 114. In contrast, in negative half cycles, the current flows through two parallel loops formed respectively from the third capacitor 114, and the third diode 115, and the first diode 113 and the first capacitor 111, as shown in Figure 7C.

5 In this example, the signal generated at the input terminals 121, 126 has a magnitude of $\pm V_p$ volts. With the input 126 forming the ground this means that during positive half cycles the input 121 reaches a peak voltage of $+V_p$, with the input reaching a minimum peak voltage of $-V_p$ during negative half cycles.

10 Accordingly, during the negative half cycles, the first clamping circuit clamps the negative peaks to 0V at the terminal 122 (assuming the forward voltage of the first diode 113 is 0V), causing the first capacitor 111 to become charged to $+V_p$ when the input terminal 121 reaches the minimum voltage $-V_p$. In positive half cycles, the voltage at the input terminal 121 increases to V_p , which raises the voltage at the first terminal 122 to $2V_p$.

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As a result, the negative peaks are clamped to zero volts and the positive peaks to $2V_p$ at the first terminal 122. An example of the voltage waveform generated at the first terminal 122 is shown in Figure 7D.

20 In response to this waveform, the first peak rectifier rectifies the waveform generated at the first terminal 122 to generate a voltage of magnitude $2V_p$ (as compared to ground) at the output terminal 123.

The second clamping and peak rectifier circuits operate to further increase the output voltage.

25 During negative half cycles, the second clamping circuit clamps the second terminal 125 to $-V_p$. As a result, the third capacitor 114 becomes charged to V_p (assuming the forward voltage of the third diode 115 is 0V) when the input terminal 121 reaches the negative peak of $-V_p$.

30 As the voltage at the output terminal 124 (which also forms the digital ground V_{ss}) is clamped to the voltage of the terminal 125 by the fourth diode 116, the digital ground V_{ss} at the output terminal 124 is clamped to $-V_p$ compared to the analogue ground at the input 126, during positive half cycles.

35 As a result, the voltage across the second capacitor 117 is $3V_p$, allowing the rectifier to provide a modulated signal or power supply signal to subsequent digital circuits, via the output terminals 123, 124. This is achieved by careful design of a time constant determined by the capacitance of the second capacitor 117, and the load of the subsequent digital circuit. Thus, by selecting a suitable

time constant, this allows the signal generated at the outputs to be used as the demodulated signal (as shown for example in Figure 4). However, if a time constant much greater than the period of the demodulated signal is selected, the output signal can be used as the power supply signal (as shown for example in Figure 5).

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Furthermore, as the output signal has a magnitude of 3Vp, the rectifier effectively triples the voltage of the received signal. Accordingly, the rectifier shown in Figure 7 effectively improves the performance and hence the operating range of a tag incorporating this rectifier instead of a prior art rectifier.

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Furthermore, the rectifier of Figure 7A can be used for any frequency of received carrier signal, with the matching network determine the operating frequencies and their bandwidth characteristics. Accordingly, appropriate design of the matching network can make transceiver circuit well matched to the antenna port over a single or range of frequency bands.

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A further benefit that can be implemented in microwave frequency communications is the use of microwave Schottky diodes that have a low forward voltage and resistance to help reduce wasted power.

20 A second example of a rectifier according to the present invention will now be described with reference to Figure 8A.

As shown the rectifier shown generally at 200 is coupled to an antenna port 201 via two matching networks 202, 203. The rectifier 200 therefore includes two pairs of input terminals, although two
25 of the input terminals are combined at 234 to form a common ground connection. The rectifier therefore effectively includes three input terminals 231, 234, 237 that are coupled to respective outputs of the matching circuits 202, 203, as shown.

The rectifier also includes first and second output terminals 233, 235, which in use would be
30 coupled to subsequent circuitry depending on the specific use of the rectifier. It will be appreciated from the above, that these outputs are therefore usually coupled to an MCU, or the like.

In any event, the rectifier is formed from:

- A first clamping circuit including a first capacitor 211 coupled to the first input terminal 231,
35 and a first terminal 232, and a first diode 213 having a cathode terminal coupled to the first terminal 232 and an anode terminal coupled to the second input terminal 234;

- A first peak rectifier including a second capacitor 214 coupled to the first output terminal 233 and the second input 234 and a second diode 212 having a cathode terminal coupled to the first output terminal 233 and an anode terminal coupled to the first terminal 232;
- A second clamping circuit including a third capacitor 215 coupled to the second input terminal 234, and a second terminal 236, and a third diode 217 having an anode terminal coupled to the second terminal 236 and a cathode terminal coupled to the second input terminal 234; and,
- A second peak rectifier including a fourth capacitor 218 coupled to the second input terminal 234 and the second output terminal 235 and a fourth diode 216 having a cathode terminal coupled to the second terminal 236 and an anode terminal coupled to the second output terminal 235.

In use, the RF signal received by the antenna induces an alternating voltage that is applied to the rectifier 200 through the port 201 and the matching networks 202, 203. In this case, one terminal of the antenna port is used to feed the terminals of the matching networks 202, 203 that form the common ground connection 234, with the other terminal 238 of the port feeding the other inputs of the matching networks, as shown. This configuration allows the rectifier to provide power supply or demodulated signals having a voltage or amplitude approximately four times as large as the peak voltage or amplitude of the RF signal induced at the antenna port 201, as will now be described.

Again, as in the case of the rectifier of Figure 7A, the signal supplied to the input terminals 231, 234, 237 is a sinusoidal signal, and accordingly the response of the rectifier will differ between positive and negative half cycles.

During positive half cycles, the current flows through the loops shown in dotted lines 240. Thus, current flows through a first positive loop formed from the first capacitor 211, the first terminal 232, the second diode 212, the second capacitor 214, and the second input terminal 234. The current also flow through the second positive loop formed from the third capacitor 215, the third diode 217 and the second input terminal 234, as shown.

During negative half cycles, the current flows through the loops shown by the dashed lines 241. The first negative loop includes the first diode 213, the first capacitor 211, and the first input terminal 231. The second negative loop includes the fourth capacitor 218, the fourth diode 216, the third capacitor 215, and the third input terminal 237.

In this example, the signal generated at the input terminals 231, 234, 237 has a magnitude of $\pm V_p$ volts. With the second input terminal 234 forming the ground this means that during positive half

cycles the inputs 231, 237 reach a peak voltage of $+V_p$, with the inputs 231, 237 reaching a minimum peak voltage of $-V_p$ during negative half cycles.

Accordingly, during the negative half cycles, the first clamping circuit clamps the negative peaks to
5 0V at the terminal 232 (assuming the forward voltage of the first diode 213 is 0V), causing the first capacitor 211 to become charged to $+V_p$ when the input 231 reaches the minimum voltage $-V_p$. In positive half cycles, the voltage at the input 121 increases to V_p , which raises the voltage at the first terminal 232 to $2V_p$, taking account the voltage V_p across capacitor 211.

10 As a result, the negative peaks are clamped to 0V and the positive peaks to $2V_p$ at the first terminal 232. An example of the voltage waveform generated at the first terminal 232 is shown in Figure 8B.

In response to this waveform, the first peak rectifier rectifies the waveform generated at the first
15 terminal 232 to generate a voltage of magnitude $2V_p$ (as compared to ground) across the capacitor 214.

The second clamping and peak rectifier circuits operate to further increase the output voltage.

20 During positive half cycles, the second clamping circuit clamps the second terminal 236 to 0V (assuming the forward voltage of the third diode 217 is 0V). As a result, the third capacitor 215 becomes charged to V_p when the third input terminal 237 reaches the peak of $+V_p$. In negative half cycles the voltage at the third input terminal 237 drops to its negative peak $-V_p$, the voltage at the second terminal 236 reaches $-2V_p$ (taking into account the voltage V_p , across the third capacitor
25 215).

As a result, the negative peaks are clamped to 0V and the positive peaks to $-2V_p$ at the second terminal 236. An example of the voltage waveform generated at the first terminal 232 is shown in Figure 8C.

30 In response to this waveform, the second peak rectifier rectifies the waveform generated at the second terminal 236 to generate a voltage of magnitude $-2V_p$ (as compared to ground) across the capacitor 218.

35 Accordingly, the potential at the output terminal 235 is $-2V_p$ when compared to the analogue ground at the second input 234.

As a result, the voltage across the output terminals 233, 235 has a magnitude of 4Vp, allowing the rectifier to provide a modulated signal or power supply signal to subsequent digital circuits, via the outputs 233, 235.

- 5 A fifth capacitor may optionally be included positioned between the output terminals 233, 235, as shown. The fifth capacitor 219 preferably helps define a time constant for the circuit, to help ensure the form of the signal generated at the outputs is correct. Thus, by selecting a suitable time constant, determined by the capacitance of the fifth capacitor 219, and the load of the subsequent digital circuit, this allows the signal generated at the outputs to be used as the demodulated signal.
- 10 However, if a time constant much greater than the period of demodulated signal is selected, the output signal can be used as the power supply signal.

In this case, the output 235 would typically be set to digital ground Vss, thereby allowing a peak voltage of +4Vp to be generated at the output terminal 233.

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Hence, the rectifier of Figure 8A is capable of providing a DC power supply signal, or a demodulated signal of magnitude approximately 4 times as great as the received signal.

- 20 In addition, to this the voltages generated across the second and fourth capacitors 214, 218 can also be used as voltage references for use in subsequent digital circuits.

Furthermore, by connecting a switch (not shown) in paralleled with one of the second, fourth or fifth capacitors 214, 218, 219, or directly between the output terminals 233, 235, this allows the
25 respective capacitor to be selectively shorted. This will effect the response of the rectifier, which in turn effects the load of the antenna. As a result, the oscillating current induced in the antenna allows the incoming carrier signal received by the antenna to be modified.

- In particular, the change in the oscillating current leads to variation in the magnitude of the
30 electromagnetic field and thus causes a change in the RF power radiated back from the antenna. The interrogator that generates the carrier signal received by the antenna can detect this change in the radiated power. Accordingly, selectively opening and closing the switch allows the incoming carrier signal to be modulated in accordance with digital data obtained from a register, a memory, a digital processor or MCU, or the like. This allows data to be transferred back to the interrogator in
35 a "backscatter" process.

Placing the switch across the second or fourth capacitor 214, 218 rather than the fifth capacitor 219

will result in a low depth of modulation similar to that shown in Figure 6, thereby helping to reduce the power consumption of the circuit, thereby helping to further increase the operating range of the device.

5 Accordingly, the output of the second, fourth or fifth capacitors can be used as demodulated data or as modulation switching points. In this case, by providing the second and fourth capacitors 214, 218 with different capacitance values, this allows one of the capacitors 214, 218 to be used as a reference voltage, whilst the other is used to provide the demodulated data.

10 Even if the capacitors 214, 218 have the same values, the different loads for each capacitor lead to different diode bias for the first and second diodes 212 and 213 compared to that of third and fourth diodes 217, 216. Accordingly, in this case, different matching networks are required. The matching networks 202, 203 can be tuned separately to match the individual digital circuits connected to the outputs 233, 235.

15

A third example of a rectifier according to the invention is shown in Figure 9A. This rectifier is similar to the rectifier shown in Figure 8A, and similar reference numerals (increased by 100) are used for similar components.

20 The operation of the circuit will not be described in detail. However, it will be appreciated that in this example, the rectifier inputs 331, 334, 337 are coupled to a single matching circuit, with the inputs 331, 337 being coupled together as shown.

The equivalent circuits showing the operation of the circuit in positive and negative half cycles are shown in Figures 9B and 9C respectively. From this it will be appreciated that during the negative half cycles, the first clamping circuit, formed from the first capacitor 311 and the first diode 313, clamps the negative peaks to 0V at the first terminal 332 (assuming the forward voltage of the first diode 213 is 0V). This causes the first capacitor 311 to become charged to +Vp when the input 331 reaches the minimum voltage -Vp. In positive half cycles, the voltage at the input 321 increases to Vp, which raises the voltage at the first terminal 332 to 2Vp, taking account the voltage Vp across capacitor 311.

30

As a result, the negative peaks are clamped to 0V and the positive peaks to 2Vp at the first terminal 332.

35

Similarly, during positive half cycles, the second clamping circuit, formed from the third capacitor 315 and the third diode 317, clamps the second terminal 336 to 0V (assuming the forward voltage

of the third diode 217 is 0V). As a result, the third capacitor 315 becomes charged to V_p when the third input terminal 337 reaches the peak of $+V_p$. In negative half cycles the voltage at the third input terminal 337 drops to its negative peak $-V_p$, the voltage at the second terminal 336 reaches $-2V_p$ (taking into account the voltage V_p , across the third capacitor 315).

5

As a result, the negative peaks are clamped to 0V and the positive peaks to $-2V_p$ at the second terminal 336.

Accordingly, the signal output for the digital circuit coupled to the output terminals 333, 335 will have a magnitude of $4V_p$ (i.e. four times as large as input signal).

In each of the above example, it will be appreciated that the diodes are non-linear components, whose non-linear characteristics include:

- one-way conductivity; and,
- variations of impedance reflected in the current versus voltage characteristic chart of the diode

The non-linear effects of the diodes make it difficult to match the impedance of the rectifier accurately. In general, when the forward voltage of a diode is small (close to 0V) the impact of any non-linearity is minimal and can be ignored. However, the response of the diode is different when forward biased rather than reversed biased. In particular, for a input voltage $V_i(t)$, and output voltage $V_o(t)$ and a diode forward voltage (voltage across the diode when forward biased) $v_d(t)$, the relationship between the voltages is defined by the equations:

$$V_o(t) = V_i(t) - V_d(t)$$

In use $V_d(t)$ demonstrates a non-linear response to $V_i(t)$, and for positive half cycles, the forward voltage $V_d(t)$ is generally so small that:

$$V_o(t) \approx V_i(t)$$

However, one-way conductivity still exists. Accordingly, it is only when symmetry is introduced into the circuit that one-way conductivity can be eliminated. In practice, the variation in the forward voltage $V_d(t)$ will depend on the voltages in the input terminals 121, 126. Thus theoretically, the impedance of the rectifier input should be impedance matched to the output of the matching circuit. However as the impedance of the rectifier has a linear response, whereas the matching circuit impedance is non-linear, this accurate impedance matching over all voltages is not possible.

Accordingly, in order to overcome this, the matching circuits in the examples described above

match to the average impedance of the rectifier.

A further point is that, in the frequency domain, diodes will tend to generate harmonics for the characteristics of its one way conductivity. Accordingly, most of the energy contained in the
5 harmonic will be wasted if the circuits match at the fundamental frequency.

Furthermore, a proportion of any harmonic components produced will be coupled to antenna, allowing them to be radiated outward as RF signals. However, these signals often fall outside the pre-approved ISM frequencies and would therefore interfere with other licensed devices. As the
10 limits on the emission levels for these frequencies are usually very low, this can make obtain approval of the system difficult.

However, the rectifier of Figure 9A overcomes these problems. In particular, the rectifier shown in Figure 9A is symmetrical so that the equivalent circuits for positive and negative half cycles are
15 identical.

As a result, the rectifier presents the same impedance during both negative and positive half cycles, allowing the matching circuit to be matched accurately to the impedance of the rectifier.

20 Accordingly, the overall response of the rectifier between the input terminals 331/337 and 334 is effectively linear, thereby allowing more accurate impedance matching of the matching network 302. This in turn helps reduce the emission of harmonic frequencies.

Accordingly, the rectifiers described above, increase the rectified voltage or amplitude of a signal
25 received at a single port antenna more than the rectifiers according to the prior art. Furthermore as the current consumption is small, a change in the current drain (or load) placed on the rectifier will not have such a major impact on the operating range of a tag incorporating the rectifier. Accordingly, this allows tags incorporating rectifiers in accordance with the invention to achieve far better operating ranges than tags incorporating prior art rectifiers.

30 Furthermore, the rectifier of Figure 9A has approximately linear response and therefore generates less harmonics, making impedance matching more accurate and effective.

As a result, the single antenna port rectifiers of Figures 7 to 9 have demonstrated a better
35 performance than the prior art rectifiers, even when compared to dual port antenna arrangements. In particular, the one port rectifiers of Figures 8 and 9 for example, provide a voltage approximate 4 times the input peak voltage, which is better in terms of operating range than the two port system

which provides similar overall voltage magnification. This is because the amplitude of RF signals established at each port of the two port antennas $V_{p'}$ is lower than that of single port antenna V_p .

Hence, the maximum voltage that the prior art can provide is:

5
$$V_{cc'} = 2 \times V_{p'} + 2 \times V_{p'} = 4 \times V_{p'}$$

Whereas in the systems of Figures 8 and 9, the rectifier provides a voltage of:

$$V_{cc} = 4 \times V_p$$

10
$$\text{Where: } V_p > V_{p'}$$

The term ground as used in the specification is intended to refer to a connection that acts as an effective ground for the purposes of the above analysis. It will be appreciated that when the rectifiers outlined above are implemented in conjunction with antennae such as loop and dipole
15 antennae, there is strictly no ground connection clamped to 0 volts. However, in this example, at least one of the input terminals will still be clamped to a particular voltage and can therefore act as a voltage reference equivalent to the ground terminal in the above analysis.

Persons skilled in the art will appreciate that numerous variations and modifications will become
20 apparent. All such variations and modifications which become apparent to persons skilled in the art, should be considered to fall within the spirit and scope that the invention broadly appearing before described.

THE CLAIMS:

- 1) A communications device for use in a wireless communications system, the system including an interrogator adapted to generate a signal, the device being adapted to communicate with the interrogator via the signal, the device including:
 - a) An antenna for receiving the signal;
 - b) A matching circuit coupled to the antenna; and
 - c) A rectifier coupled to the matching circuit to receive the signal via the matching circuit, the received signal having a magnitude V_p , the rectifier being adapted to perform at least one of:
 - i) Rectify the signal to generate a power supply signal, the power supply signal having a magnitude of at least $3V_p$; and,
 - ii) Demodulate the signal to generate a demodulated signal, the demodulated signal having a magnitude of at least $3V_p$; and,
 - d) A switching circuit coupled to the rectifier to thereby effect the response of the rectifier so as to control the modulation of the received signal in accordance with a modulating signal received from a controller.
- 2) A communications device according to claim 1, the rectifier including at least one capacitor, and wherein the switching circuit operates to effect the response of the rectifier by shorting the capacitor.
- 3) A communications device according to claim 1 or claim 2, the rectifier being coupled to output terminals having a capacitor positioned therebetween, the capacitor being selected in accordance with the load of a subsequent digital circuit to thereby control the time constant of the rectifier, which in turn causes the rectifier to generate the power supply signal or the demodulated signal.
- 4) A communications device according to any one of the claims 1 to 3, the rectifier having a linear response.
- 5) A communications device according to claim 4, wherein equivalent circuits defined by the rectifier for positive and negative half cycles are identical.
- 6) A communications device according to any one of the claims 1 to 5, the rectifier including:
 - a) First and second input terminals coupled to the antenna for receiving the signal, one of the input terminals forming a voltage reference;
 - b) First and second output terminals;
 - c) A first clamping circuit coupled to at least one of the input terminals and the voltage reference, the first clamping circuit being adapted to generate a first clamped signal at a first terminal;
 - d) A first peak rectifier coupled to the first terminal and at least the first output terminal, the first peak rectifier being adapted to rectify the first clamped signal to generate a first rectified signal at the first output terminal with respect to voltage reference;

- e) A second clamping circuit coupled to at least one of the input terminals and the voltage reference, the second clamping circuit being adapted to generate a second clamped signal at a second terminal; and,
- f) A second peak rectifier coupled to the second terminal and at least the second output terminal, the second peak rectifier being adapted to rectify the second clamped signal to generate a second rectified signal at the second output terminal with respect to voltage reference.
- 7) A communications device according to claim 6, wherein, in use, the first and second input terminals of the rectifier are coupled to the antenna via an impedance matching circuit.
- 8) A communications device according to claim 7, the second input terminal forming the voltage reference, the signal having a magnitude V_p , and the first clamping circuit being coupled to the first input terminal such that the first clamped signal has a magnitude substantially equal to $2V_p$.
- 9) A communications device according to claim 8, the second clamping circuit being coupled to the first input terminal such that the second clamped signal has a magnitude substantially equal to $-V_p$.
- 10) A communications device according to claim 9, the rectifier being adapted to provide a modulated signal or DC voltage having a magnitude of substantially $3V_p$.
- 11) A communications device according to any of claims 6 to 10, wherein:
 - a) The first clamping circuit includes:
 - i) A first capacitor coupled to the first input terminal and the first terminal; and,
 - ii) A first diode having a cathode terminal coupled to the first terminal and an anode terminal coupled to the second input;
 - b) The first peak rectifier includes:
 - i) A second capacitor coupled to the first and second output terminals; and,
 - ii) A second diode having a cathode terminal coupled to the first output terminal and an anode terminal coupled to the first terminal;
 - c) The second clamping circuit includes:
 - i) A third capacitor coupled to the second input terminal and the second terminal; and,
 - ii) A third diode having a cathode terminal coupled to the first input terminal and an anode terminal coupled to the second terminal; and,
 - d) The second peak rectifier includes:
 - i) The second capacitor coupled to the first and second output terminals; and,
 - ii) A fourth diode having a cathode terminal coupled to the second terminal and an anode terminal coupled to the second output terminal.
- 12) A communications device according to claim 11, the rectifier being adapted to further modulate the received carrier signal, the rectifier including a switching circuit connected in parallel with the

- second capacitor, the switching circuit being adapted to control the modulation of the received signal in accordance with a modulating signal received from a controller.
- 13) A communications device according to any one of claims 6 to 12, the rectifier further including third and fourth input terminals.
 - 14) A communications device according to claim 13, wherein, in use, the third and fourth input terminals are coupled to the antenna via a respective impedance matching circuit.
 - 15) A communications device according to claim 13 or claim 14, when dependent on claim 8, the third input terminal being coupled to the second to thereby form the voltage reference, the second clamping circuit being coupled to the fourth input terminal such that the second clamped signal has a magnitude substantially equal to $-2V_p$.
 - 16) A communications device according to claim 15, the rectifier being adapted to provide a modulated signal or DC voltage having a magnitude of substantially $4V_p$.
 - 17) A communications device according to any one of claims 13 to 16, wherein:
 - a) The first clamping circuit includes:
 - i) A first capacitor coupled to the first input terminal and the first terminal; and,
 - ii) A first diode having a cathode terminal coupled to the first terminal and an anode terminal coupled to the voltage reference;
 - b) The first peak rectifier includes:
 - i) A second capacitor coupled to the first output terminal and the voltage reference; and,
 - ii) A second diode having a cathode terminal coupled to the first output terminal and an anode terminal coupled to the first terminal;
 - c) The second clamping circuit includes:
 - i) A third capacitor coupled to the fourth input terminal and the second terminal; and,
 - ii) A third diode having a cathode terminal coupled to the voltage reference and an anode terminal coupled to the second terminal; and,
 - d) The second peak rectifier includes:
 - i) A fourth capacitor coupled to the second output terminal and the ground; and,
 - ii) A fourth diode having a cathode terminal coupled to the second terminal and an anode terminal coupled to the second output terminal.
 - 18) A communications device according to claim 17, the fourth input terminal being coupled to the first input, such that the first, second third and fourth input terminals are coupled to the antenna via a single matching circuit.
 - 19) A communications device according to claim 17 or claim 18, the switching circuit being connected in parallel with either or both of the second and fourth capacitors.

- 20) A communications device according to claim 12 or claim 19, the controller being adapted to receive data and modulate the received signal in accordance with received data.
- 21) A communications device according to claim 20, the rectifier being adapted to receive the data from a data store.
- 22) A communications device according to claim 17 or claim 18, the communications device being passive or semi passive RFID Tag.
- 23) A communications device according to any one of claims 17 to 19, the rectifier being adapted to generate at least one of a power supply signal having a magnitude of at least $4V_p$ and a demodulated signal having a magnitude of at least $4V_p$.
- 24) A communications system including a communications device according to any of claims 1 to 23, and an interrogator adapted to generate the signal.
- 25) A rectifier for use in a communications device, the rectifier being coupled in use to a matching circuit to receive a signal via the matching circuit, the received signal having a magnitude V_p , the rectifier being adapted to perform at least one of:
- a) Rectify the signal to generate a power supply signal, the power supply signal having a magnitude of at least $3V_p$; and,
 - b) Demodulate the signal to generate a demodulated signal, the demodulated signal having a magnitude of at least $3V_p$; and,
- and, wherein in use, the rectifier is coupled to a switching circuit coupled to the rectifier to thereby effect the response of the rectifier so as to control the modulation of the received signal in accordance with a modulating signal received from a controller.
- 26) A rectifier according to claim 26, the rectifier being adapted for use in the communications device of any one of the claims 1 to 23.