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PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Semiconductor Structures and methods of manufacture

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organized according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor structures and methods of manufacturing such structures.

According to the present invention, a method of fabricating a semi-conductor structure includes the steps of embedding a plurality of monocrystalline bodies of semiconductor material in a support substrate composed of glass having a working temperature above about 900°C., the bodies being electrically isolated from each other through the substrate and exposed at one surface only of the substrate. The bodies may all be of the same semiconductor material or bodies of different semiconductor materials may be embedded in the substrate.

In one embodiment the method is carried out by forming a plurality of mesas at one surface of a wafer of monocrystalline semiconductor material. That surface is then coated with high temperature glass to provide the support substrate and wafer material is removed to leave only the mesas embedded in the substrate. In an alternative embodiment, one surface of a wafer of monocrystalline semiconductor material is coated with high temperature glass to form the support substrate. The opposite surface of the wafer is then etched to form discrete spaced bodies of monocrystalline semiconductor material and the bodies are embedded in the support substrate.

Circuit components can be formed in the embedded bodies of semiconductor material using oxide masking and diffusion techniques. Passive components may also be formed by deposition of resistive film material on the substrate itself. A suitable lead pattern can be formed overlying the substrate and the oxide material to interconnect the components in a desired manner.

The invention also comprises an integrated semiconductor network comprising a support substrate composed of glass having a working temperature above about 900°C., at least one semiconductor body embedded in the support substrate and containing an active circuit component, at least one semiconductor body embedded in the support substrate and containing a passive circuit component, the said bodies being electrically isolated through the support substrate and electrically interconnected by conductive means overlying a surface of the support substrate and connected to surfaces of the bodies extending to that surface, the opposite surfaces of the semiconductor bodies being covered by the substrate.

The invention also comprises an integrated semiconductor network comprising a support substrate composed of glass having a working temperature above about 900°C. in which are embedded bodies of semiconductor material, the bodies being formed of two or more of the materials silicon, germanium, and gallium arsenide, the bodies being electrically isolated from each other through the substrate and each body providing a circuit component accessible at a surface of that body extending to a surface of the substrate, the opposite surfaces of the bodies being covered by the substrate.

By way of example, the invention will be described in greater detail with reference to the accompanying drawings in which:

FIGURES 1a—1e are pictorial views in section of a semiconductor wafer and glass substrate illustrating steps of one method of producing a semiconductor structure in accordance with the present invention,

FIGURES 2a—2f are pictorial views in section of a semiconductor wafer and glass substrate illustrating steps in an alternative method of producing a semiconductor structure in accordance with the invention.

FIGURES 3a is a pictorial view in section of an integrated semiconductor network formed by the process illustrated in FIGURES 1a—1e or that illustrated in FIGURES 2a—2f, and

FIGURE 3b is the circuit diagram of the network shown in FIGURE 3a.

In the embodiments of the invention to be described, single crystalline semiconductor circuit components are supported by a glass substrate. The substrate, an insulating material, provides electrical isolation of the circuit components. In one embodiment mesas are formed by etching on one side of a semiconductor wafer. Initially the wafer may have an epitaxial layer of N+ or P+ material depending upon device requirements. After the mesas are formed, the side of the wafer having the mesas is coated with a high temperature glass, a glass with a working temperature above about 900°C, which has a coefficient of thermal expansion substantially matching the coefficient of thermal expansion of the semiconductor material. The layer of glass has sufficient thickness to give mechanical strength to the microminiature circuit subsequently formed thereon. After the glass coating has been applied, the exposed surface of the semiconductor wafer is removed by lapping or etching, for example, leaving only the mesa portions of the wafer embedded in the glass substrate. The desired circuit components can then be formed in the embedded semiconductor material by conventional masking, etching and diffusing techniques. Finally, ohmic leads and contacts are provided to interconnect the components and complete the circuit.

In another embodiment, a glass coating can be applied to a plane surface on one side of a semiconductor wafer. The exposed side of the wafer is then scribed to fracture the crystalline structure of the wafer in a desired pattern. An etchant is applied to this side of the wafer and the semiconductor material is preferentially etched along the scribed areas, thus leaving islands of semiconductor material on the glass substrate. The glass is then heated to its working point and pressure is applied to the remaining semiconductor material to embed the islands of semiconductor material in the glass. The glass surface can be polished, if necessary, to obtain a plane surface for subsequent operations.

In another embodiment, bodies of silicon, germanium, gallium arsenide, or any combinations thereof can be embedded in a single glass substrate. Thus a circuit can be obtained which includes several types of semiconductor components, thereby utilizing the particular electrical and thermal characteristics of each of the semiconductor materials.

A preferred embodiment of the invention will be described with reference to FIGURES 1a—1e. Illustrated are steps of a method for making the logical "NOR" circuit shown in FIGURE 3a and FIGURE 3b. In FIGURE 1a, a portion of a semiconductor wafer 10 is shown. The wafer 10 may be a single crystal or a single crystal with an epitaxial layer, depending on device requirements. In this illustrative embodiment, N-type silicon is used; however, the material could be germanium or gallium arsenide. Conventional photomasking and etching techniques are utilized to form mesas 11 on the wafer 10 as shown in FIGURE 1b. In FIGURE 1c, a high temperature alumina silica glass 12 is coated on the side of the wafer having the mesas. The glass is chosen to have a coefficient of thermal expansion substantially the same as the silicon over the temperature range of 0°C to 1100°C. One convenient technique for applying the glass to the semiconductor wafer is by using a photoresist-glass mixture as described in patent Specification No. 1073758. With this technique, a mixture of glass particles and a photoresist polymer, such as Eastman Kodak KMER, is applied to the wafer surface by a settling or a centrifugal process, taught in the above-identified application. Subsequently, the photoresist polymer is developed to provide a temporary bond for the glass particles. The wafer and glass coating are then fired at a sufficient temperature to melt the glass and burn away the polymer. After the wafer and glass are cooled, the semiconductor wafer 10 is removed by lapping or etching. FIGURE 1d shows the glass substrate 12 rotated through 180° and the wafer 10 removed, leaving only the mesas 11 embedded in the glass substrate 12. The glass must have sufficient thickness to provide mechanical support for the mesas, but should also be readily scribed and broken. A glass thickness of 5 mils is satisfactory. In FIGURE 1e, a silicon oxide layer 13 is formed on the exposed surfaces of the mesas. This is accomplished by oxidizing the semiconductor material, if silicon, or by depositing silicon oxide by using an organometallic compound such as tetraethoxysilane in either an oxidative or pyrolytic process, both processes being well known in the art. Conventional photomasking, etching and diffusing processes are then used to form the base and emitter regions of the transistors T_1 and T_2 and the resistors R_1, R_2 and R_3 for the circuit illustrated in FIGURE 3a. Rather than having diffused resistors, thin film resistors of Nichrome (Registered Trade Mark) for example, can be applied to the surface of the glass substrate. Lastly, ohmic leads and contacts are provided to complete the circuit.

Another illustrative embodiment is shown in

FIGURES 2a—2f. Again steps of a method for making the logical "NOR" circuit of FIGURE 3a are described. FIGURE 2a is a portion of a semiconductor wafer 20, again N-type silicon, for example. In FIGURE 2b a glass layer 21 is applied to a plane surface of the wafer 20. In FIGURE 2c, the wafer is shown rotated through 180° and the exposed surface of the semiconductor wafer 20 has been scribed to fracture the crystalline structure as illustrated by the scribe line 22 and the fracture 23. Next, the surface of the semiconductor wafer 20 may be masked in a pattern which exposes only the scribed portions; however, this step is not necessarily required as an etchant will preferentially attack the scribed and fractured portions of the semiconductor wafer 20. The semiconductor wafer 20 is then etched, preferably by an alkaline etchant such as sodium hydroxide which does not attack the glass. The etchant preferentially etches the damaged areas of the semiconductor wafer, leaving islands 24 of semiconductor material as shown in FIGURE 2d. Next, the glass layer 21 is heated to its working point and the semiconductor islands 24 are pressed into the glass layer 21, as shown in FIGURE 2e. The surface of the glass layer can then be polished, if necessary, to obtain a plane surface for subsequent operations. However, it may be possible to obtain sufficient planarity without polishing if, for example, polished silicon carbide pressure plates are used. In FIGURE 2f, the semiconductor islands 24 are coated with a silicon oxide film 25. Again, this may be accomplished either by oxidizing the surface of the semiconductor, if silicon, or by vapor deposition of silicon oxide. Finally, the desired circuit components are formed in the masked semiconductor islands by employing conventional photomasking, etching, and diffusing techniques. The circuit components are then interconnected to provide a circuit similar to FIGURE 3a.

The process of this invention offers the advantage of having microelectronic circuits with components of more than one semiconductor material. For instance, silicon or germanium transistors, whose electrical characteristics such as leakage current and current gain increase with temperature, can be used in conjunction with gallium arsenide transistors whose electrical characteristics drop off with temperature increase. Thus, temperature compensation can be built into a circuit by proper choice of semiconductor components. The several semiconductor materials can be placed on a suitable glass substrate, an alumina-silica-lead oxide glass for example, and then pressed into the glass substrate in a manner as described with reference to FIGURES 2a—2f.

While the invention has been described with reference to specific methods and embodiments, it is to be understood that this description is not to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as other embodiments of the invention will become apparent to persons skilled in the art without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. A method of fabricating a semiconductor structure, including the steps of embedding a plurality of monocrystalline bodies of semiconductor material in a support substrate composed of glass having a working temperature above about 900°C., the bodies being electrically isolated from each other through the substrate and exposed at one surface only of the support substrate.

2. A method according to Claim 1, in which a plurality of mesas are formed at one surface of a wafer of monocrystalline semiconductor material, the said one surface of the wafer is coated with glass to cover the mesas and to provide the support substrate, and wafer material is removed from the opposite side of the water to leave only the mesas embedded in the substrate.

3. A method according to Claim 1, in which one surface of a wafer of monocrystalline semiconductor material is coated with glass to form the support substrate, the opposite surface of the wafer is etched to form discrete spaced bodies of monocrystalline semiconductor material and the bodies are embedded in the support substrate.

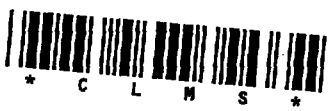
4. A method according to Claim 3, in which the discrete bodies are formed by scribing the said opposite surface of the wafer to fracture selected portions of the crystalline structure of the wafer and an etchant is applied to the scribed surface until the fractured portions of the wafer have been removed leaving the said discrete bodies of semiconductor material.

5. A method according to any one of the preceding claims, the semiconductor material being silicon and the glass being alumina-silica glass having a coefficient of thermal expansion substantially equal to that of the silicon material over the temperature range 0°C to 1100°C.

6. A method according to any one of the preceding claims, including the steps of covering the exposed surfaces of the semiconductor bodies with silicon oxide, selectively diffusing doping impurities into the embedded semiconductor bodies to form circuit components and applying ohmic contacts and leads to the structure to interconnect the components in a desired manner.

7. A method according to Claim 6, including the step of applying resistive film circuit components to the glass substrate, and in which the said ohmic contacts and leads interconnect the diffused and film components.

8. A method according to Claim 1, in which bodies of respectively different semiconductor material are embedded in the substrate.



FIGURES 2a—2f. Again steps of a method for making the logical "NOR" circuit of FIGURE 3a are described. FIGURE 2a is a portion of a semiconductor wafer 20, again N-type silicon, for example. In FIGURE 2b a glass layer 21 is applied to a plane surface of the wafer 20. In FIGURE 2c, the wafer is shown rotated through 180° and the exposed surface of the semiconductor wafer 20 has been scribed to fracture the crystalline structure as illustrated by the scribe line 22 and the fracture 23. Next, the surface of the semiconductor wafer 20 may be masked in a pattern which exposes only the scribed portions; however, this step is not necessarily required as an etchant will preferentially attack the scribed and fractured portions of the semiconductor wafer 20. The semiconductor wafer 20 is then etched, preferably by an alkaline etchant such as sodium hydroxide which does not attack the glass. The etchant preferentially etches the damaged areas of the semiconductor wafer, leaving islands 24 of semiconductor material as shown in FIGURE 2d. Next, the glass layer 21 is heated to its working point and the semiconductor islands 24 are pressed into the glass layer 21, as shown in FIGURE 2e. The surface of the glass layer can then be polished, if necessary, to obtain a plane surface for subsequent operations. However, it may be possible to obtain sufficient planarity without polishing if, for example, polished silicon carbide pressure plates are used. In FIGURE 2f, the semiconductor islands 24 are coated with a silicon oxide film 25. Again, this may be accomplished either by oxidizing the surface of the semiconductor, if silicon, or by vapor deposition of silicon oxide. Finally, the desired circuit components are formed in the masked semiconductor islands by employing conventional photomasking, etching, and diffusing techniques. The circuit components are then interconnected to provide a circuit similar to FIGURE 3a.

The process of this invention offers the advantage of having microelectronic circuits with components of more than one semiconductor material. For instance, silicon or germanium transistors, whose electrical characteristics such as leakage current and current gain increase with temperature, can be used in conjunction with gallium arsenide transistors whose electrical characteristics drop off with temperature increase. Thus, temperature compensation can be built into a circuit by proper choice of semiconductor components. The several semiconductor materials can be placed on a suitable glass substrate, an alumina-silica-lead oxide glass for example, and then pressed into the glass substrate in a manner as described with reference to FIGURES 2a—2f.

While the invention has been described with reference to specific methods and embodiments, it is to be understood that this description is not to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as other embodiments of the invention will become apparent to persons skilled in the art without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. A method of fabricating a semiconductor structure, including the steps of embedding a plurality of monocrystalline bodies of semiconductor material in a support substrate composed of glass having a working temperature above about 900°C., the bodies being electrically isolated from each other through the substrate and exposed at one surface only of the support substrate.

2. A method according to Claim 1, in which a plurality of mesas are formed at one surface of a wafer of monocrystalline semiconductor material, the said one surface of the wafer is coated with glass to cover the mesas and to provide the support substrate, and wafer material is removed from the opposite side of the water to leave only the mesas embedded in the substrate.

3. A method according to Claim 1, in which one surface of a wafer of monocrystalline semiconductor material is coated with glass to form the support substrate, the opposite surface of the wafer is etched to form discrete spaced bodies of monocrystalline semiconductor material and the bodies are embedded in the support substrate.

4. A method according to Claim 3, in which the discrete bodies are formed by scribing the said opposite surface of the wafer to fracture selected portions of the crystalline structure of the wafer and an etchant is applied to the scribed surface until the fractured portions of the wafer have been removed leaving the said discrete bodies of semiconductor material.

5. A method according to any one of the preceding claims, the semiconductor material being silicon and the glass being alumina-silica glass having a coefficient of thermal expansion substantially equal to that of the silicon material over the temperature range 0°C to 1100°C.

6. A method according to any one of the preceding claims, including the steps of covering the exposed surfaces of the semiconductor bodies with silicon oxide, selectively diffusing doping impurities into the embedded semiconductor bodies to form circuit components and applying ohmic contacts and leads to the structure to interconnect the components in a desired manner.

7. A method according to Claim 6, including the step of applying resistive film circuit components to the glass substrate, and in which the said ohmic contacts and leads interconnect the diffused and film components.

8. A method according to Claim 1, in which bodies of respectively different semiconductor material are embedded in the substrate.



9. A method of forming a semiconductor structure substantially as described herein with reference to and as illustrated by FIGURES 1a—1e of the accompanying drawings.

10. A method of forming a semiconductor structure substantially as described herein with reference to and as illustrated by FIGURES 2a—2f of the accompanying drawings.

11. A method according to Claim 9 or Claim 10 substantially as described herein with further reference to and as illustrated by FIGURES 3a and 3b of the accompanying drawings.

12. A semiconductor structure produced by a method according to any one of the preceding claims.

13. An integrated semiconductor network comprising a support substrate composed of glass having a working temperature above about 900°C, at least one semiconductor body embedded in the support substrate and containing an active circuit component, at least one semi-conductor body embedded in the support substrate and containing a passive circuit component, the said bodies being electrically isolated through the support substrate and electrically interconnected by conductive means overlying a surface of the support substrate and connected to surfaces of the bodies extending to that substrate surface, the opposite surfaces of the semiconductor bodies being covered by the substrate.

14. An integrated semiconductor network comprising a support substrate composed of glass having a working temperature above about 900°C in which are embedded bodies of semiconductor material, the bodies being formed of two or more of the materials silicon, germanium and gallium arsenide, the bodies being electrically isolated from each other through the substrate and each body defining a circuit component accessible at a surface of that body extending to a surface of the substrate, the opposite surfaces of the bodies being covered by the substrate.

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