C L A I M S

1. A storage system comprising:

a first memory chip unit including a first pad electrode unit including a first portion and a second portion electrically coupled to each other, and a first memory cell array electrically coupled to the first pad electrode unit; and

a prober that is able to hold the first memory chip unit and executes reading and writing on the first memory cell array of the held first memory chip unit, wherein

the prober includes

a probe card including a first probe electrode that is able to be in contact with the first pad electrode unit of the held first memory chip unit, and a first memory controller that is able to be electrically coupled to the first probe electrode and execute reading and writing on the first memory cell array via the first probe electrode, and

a movement mechanism that moves the probe card or the held first memory chip unit to bring the first pad electrode unit of the held first memory chip unit into contact with the first probe electrode,

the movement mechanism executes a first operation that brings the first probe electrode into contact with the first portion of the first pad electrode unit and does not bring the first probe electrode into contact with the second portion of

the first pad electrode unit, and a second operation that does not bring the first probe electrode into contact with the first portion of the first pad electrode unit and brings the first probe electrode into contact with the second portion of the first pad electrode unit, and

the movement mechanism is configured to

execute the first operation when a first condition is not satisfied, and

execute the second operation when the first condition is satisfied.

2. The storage system according to claim 1, further comprising:

a first wafer including the first memory chip unit, wherein

the prober is able to hold the first wafer, and holds the first memory chip unit by holding the first wafer, and

the movement mechanism moves the first memory chip unit by moving the first wafer.

3. The storage system according to claim 1, wherein

the first condition includes that the number of times of contact between the first probe electrode and the first portion of the first pad electrode unit is equal to or larger than a first threshold.

4. The storage system according to claim 1, wherein

the first condition includes that the first memory controller has failed in error correction processing of data from the first memory chip unit.

5. The storage system according to claim 1, wherein

the first condition includes that the first memory chip unit has failed in error correction processing of data from the first memory controller.

6. The storage system according to claim 1, wherein

the first memory chip unit includes a latch circuit that is commonly coupled to the first portion and the second portion of the first pad electrode unit.

7. The storage system according to claim 3, further comprising:

a first wafer including the first memory chip unit; and

a second wafer, wherein

the prober is able to hold the first wafer, and holds the first memory chip unit by holding the first wafer,

the movement mechanism moves the first memory chip unit by moving the first wafer, and

the movement mechanism is further able to execute a third operation that brings the first probe electrode into contact with the second wafer.

8. The storage system according to claim 7, wherein

the movement mechanism is configured to execute the first operation or the second operation after executing the third operation, when a second condition is satisfied.

9. The storage system according to claim 8, wherein

the second condition includes that the number of times of contact between the first probe electrode and the first wafer is equal to or larger than a second threshold larger than the first threshold.

10. The storage system according to claim 2, wherein

the first wafer further includes a second memory chip unit including a second pad electrode unit including a first portion and a second portion electrically coupled to each other, and a second memory cell array electrically coupled to the second pad electrode unit,

the probe card further includes a second probe electrode electrically coupled to the first memory controller,

the first operation further includes bringing the second probe electrode into contact with the first portion of the second pad electrode unit, and

the second operation further includes bringing the second probe electrode into contact with the second portion of the second pad electrode unit.

11. The storage system according to claim 2, wherein

the first wafer further includes a third memory chip unit including a third pad electrode unit including a first portion and a second portion electrically coupled to each other, and a third memory cell array electrically coupled to the third pad electrode unit,

the probe card further includes a third probe electrode and a second memory controller electrically coupled to the third probe electrode,

the first operation further includes bringing the third probe electrode into contact with the first portion of the third pad electrode unit, and

the second operation further includes bringing the third probe electrode into contact with the second portion of the third pad electrode unit.

12. The storage system according to claim 2, wherein

the first pad electrode unit has a convex shape from the first wafer toward the probe card in a state where the first wafer is placed in the prober, and

a portion of the first probe electrode facing the first wafer placed in the prober has a flat plate shape.