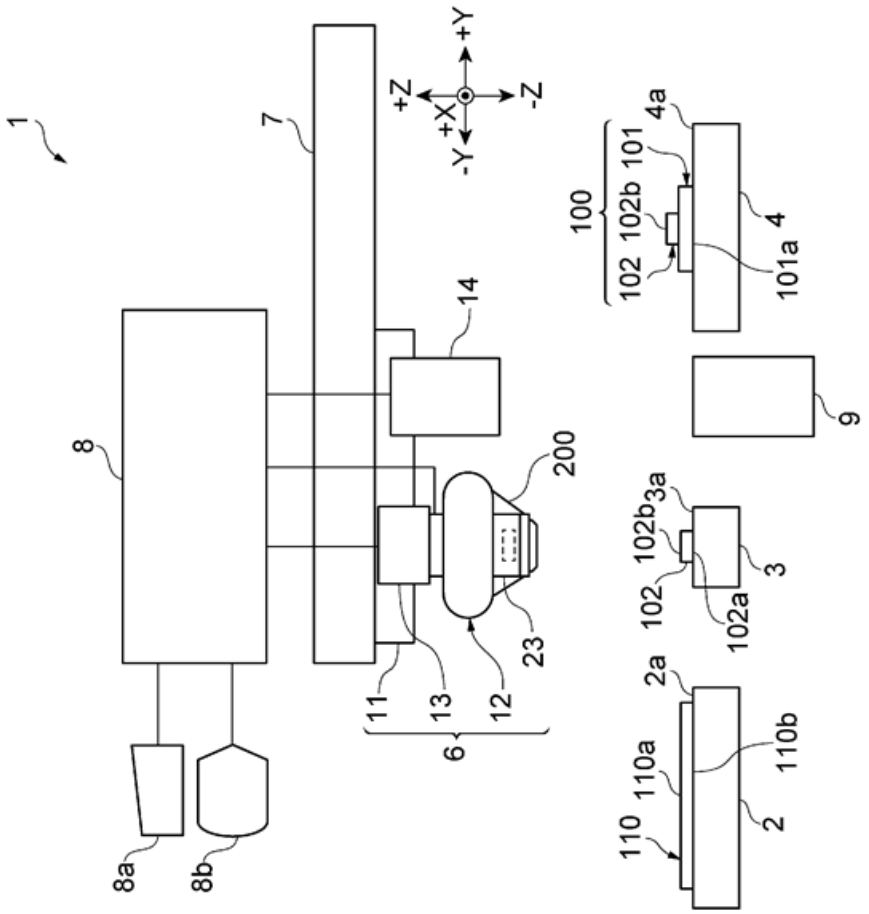
1
7
+Z
+Y
-Z
+X
-Y
14
8
200
23
11
13
12
6
8a
8b
100
102
102b
101
4a
4
101a
9
3a
102b
102
102a
3
2a
110a
110
110b
2

FIG. 1

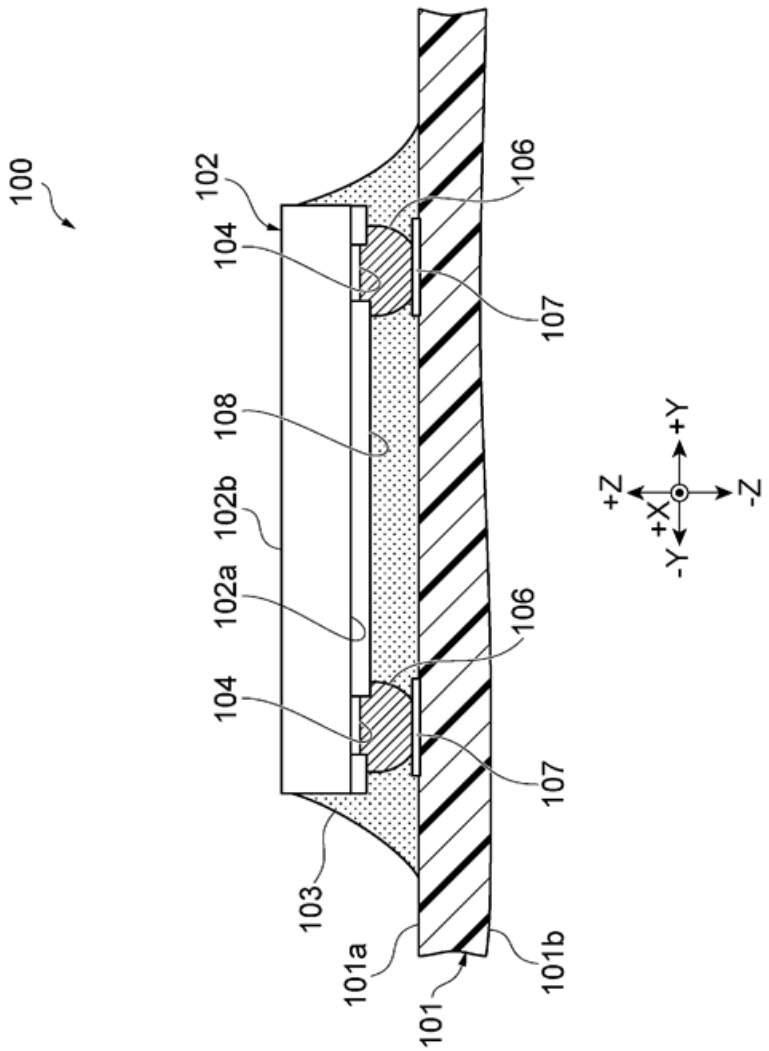
100
102
104
106
107
108
102b
102a
106
104
107
103
101a
101b
101
+Z
+Y
-Z
+X
-Y

FIG. 2

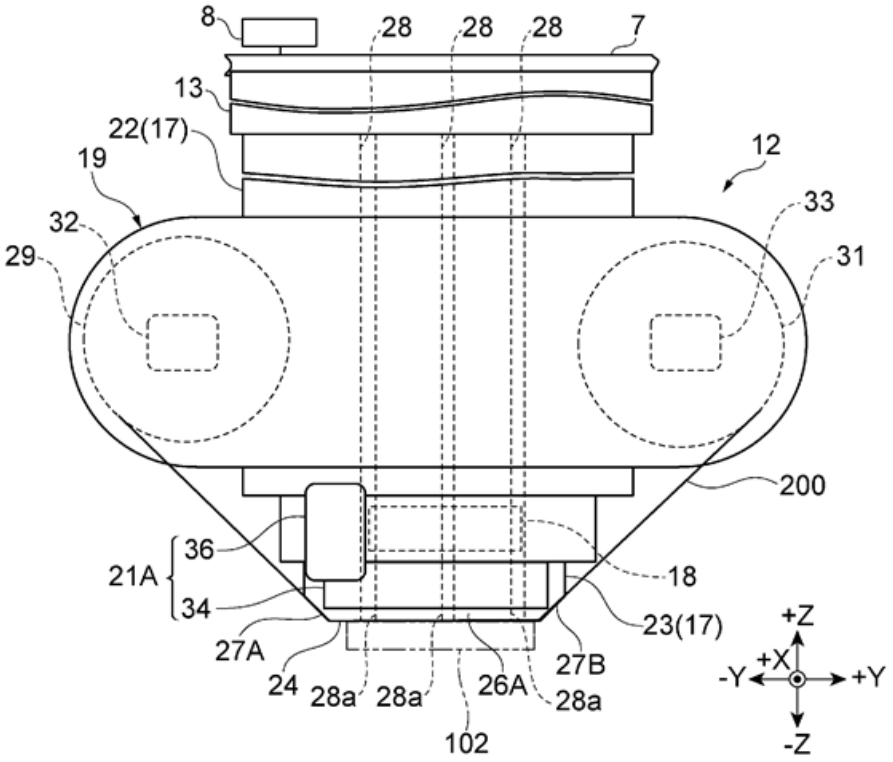
8
28
28
28
7
13
22(17)
19
12
32
33
29
31
200
36
21A
34
18
23(17)
27A
24
28a
28a
26A
27B
28a
102
+Z
+X
-Y
+Y
-Z

FIG. 3

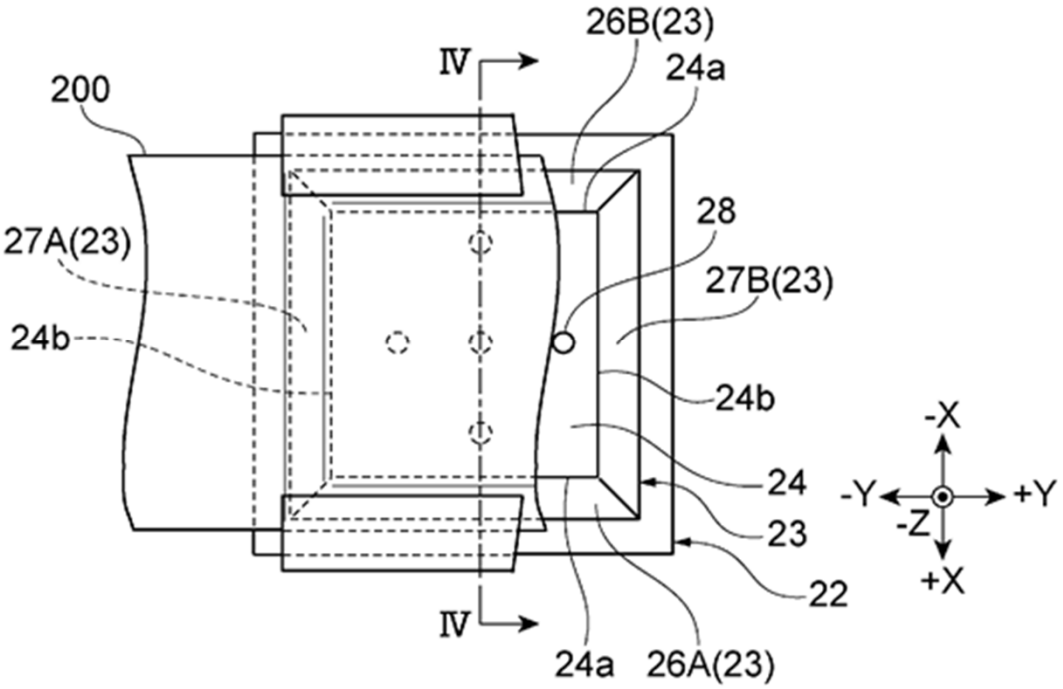
26B(23)
IV
24a
200
28
27A(23)
27B(23)
24b
24b
24
23
22
IV
24a
26A(23)
-X
-Y
+Y
-Z
+X

FIG. 4A

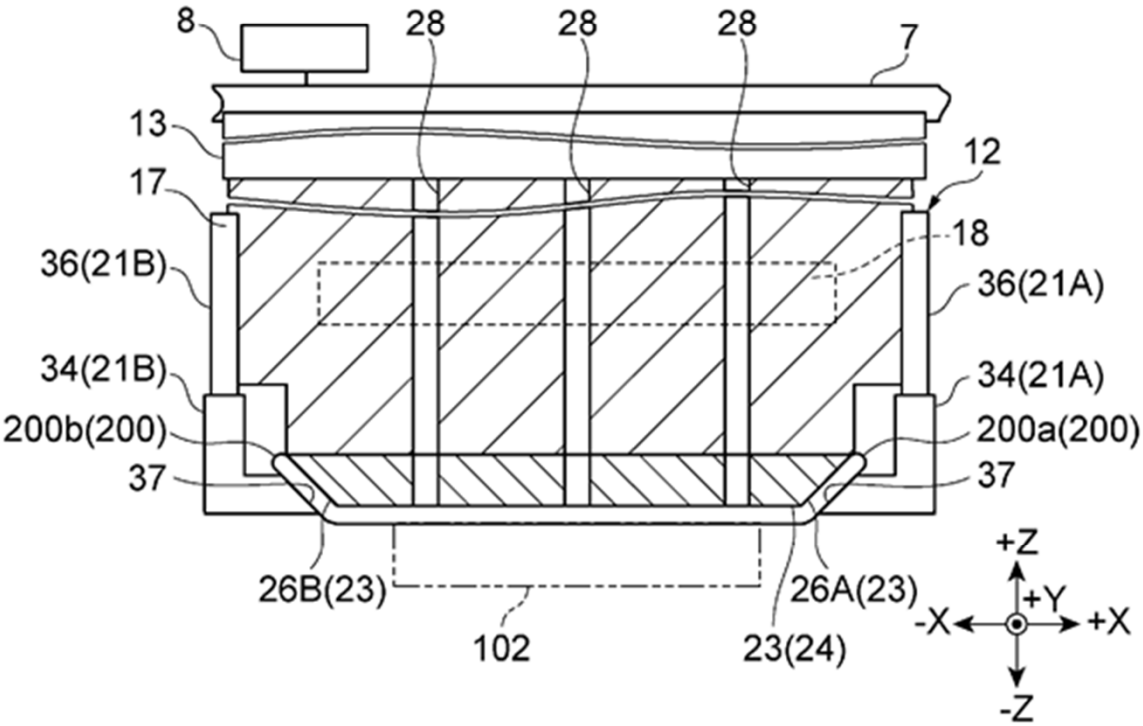
8
28
28
28
7
13
12
17
18
36(21B)
36(21A)
34(21B)
34(21A)
200b(200)
200a(200)
37
37
26B(23)
26A(23)
102
23(24)
+Z
+Y
-X
+X
-Z

FIG. 4B

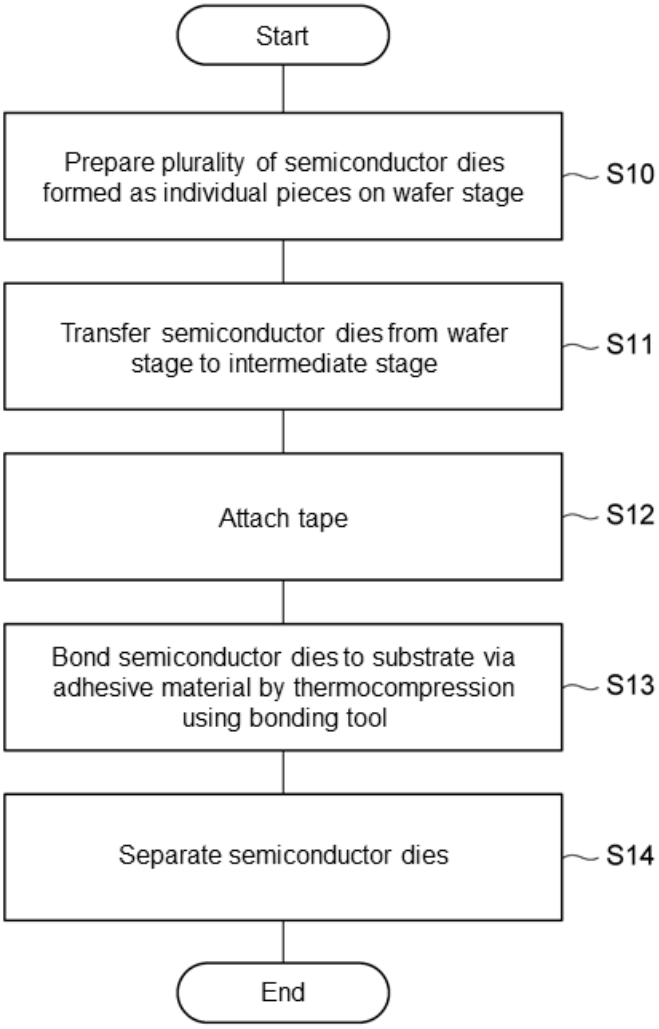
Start
Prepare plurality of semiconductor dies formed as individual pieces on wafer stage
S10
Transfer semiconductor dies from wafer stage to intermediate stage
S11
Attach tape
S12
Bond semiconductor dies to substrate via adhesive material by thermocompression using bonding tool
S13
Separate semiconductor dies
S14
End

FIG. 5

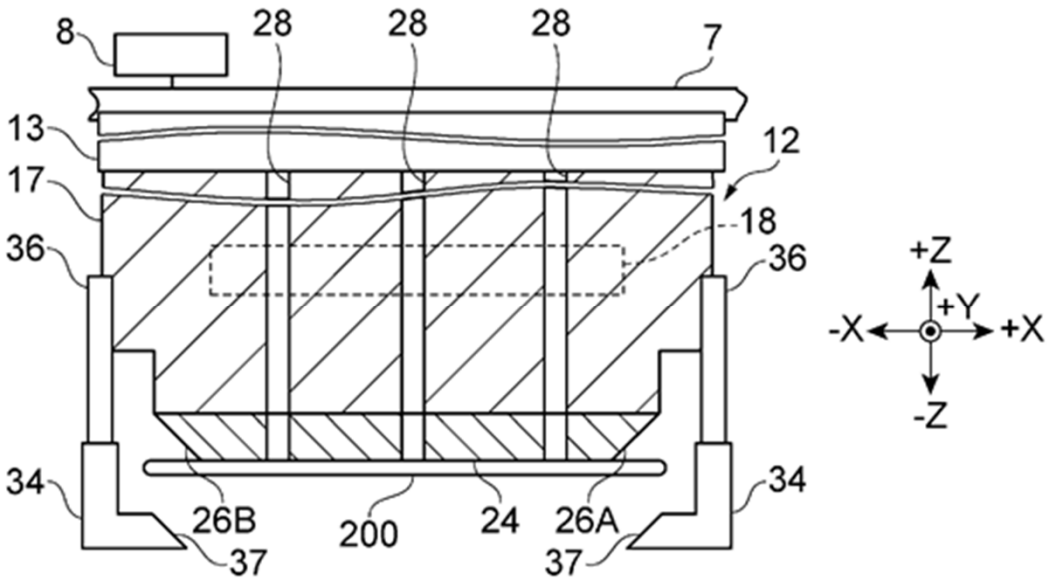
8
28
28
28
7
13
12
17
18
36
36
+Z
+Y
-X
+X
-Z
34
34
26B
200
24
26A
37
37

FIG. 6A

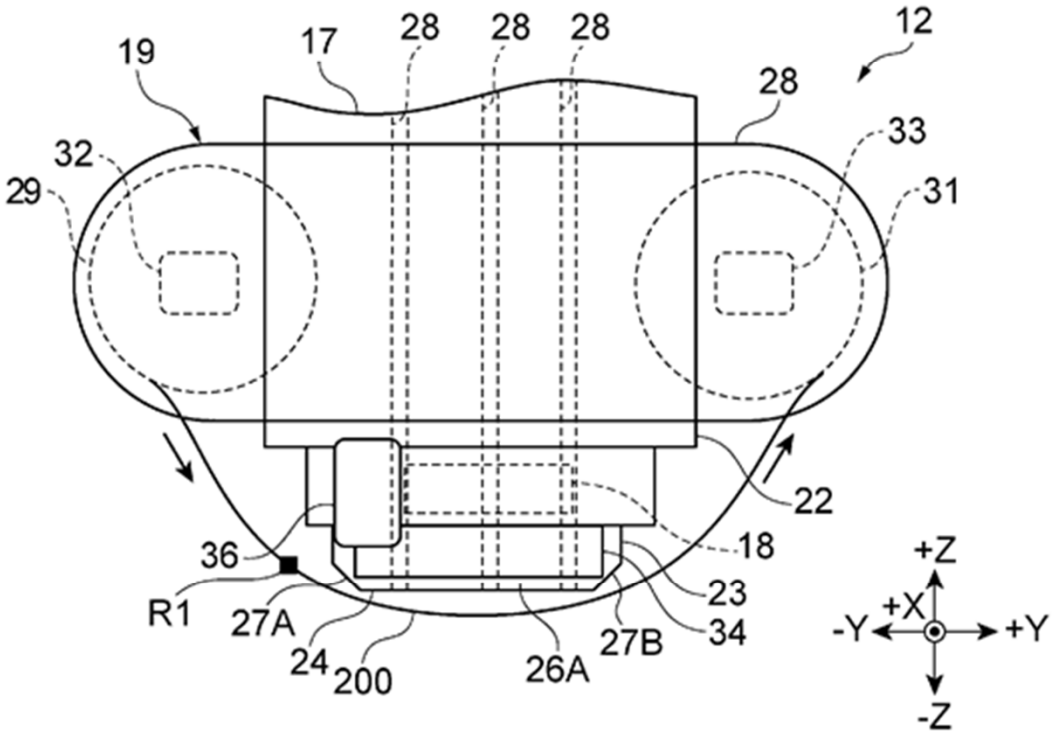
19
17
28
28
28
12
28
32
33
29
31
22
18
36
R1
27A
24
200
26A
27B
23
34
+Z
+X
-Y
+Y
-Z

FIG. 6B

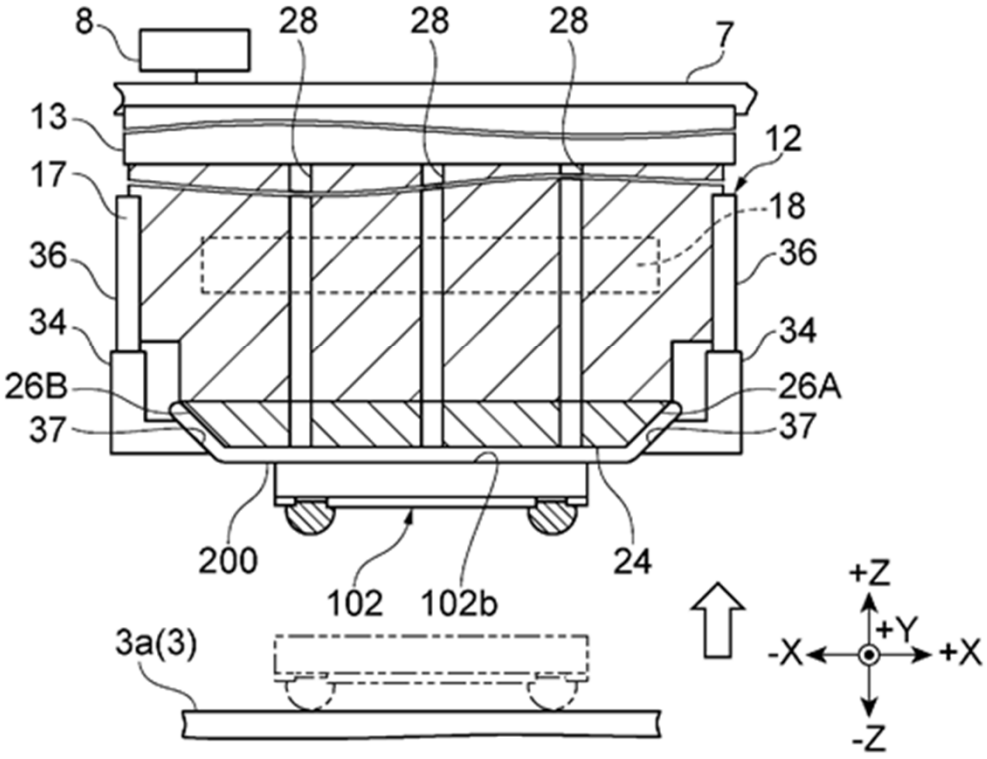
8
28
28
28
7
13
12
17
18
36
36
34
34
26B
26A
37
37
200
102
102b
24
3a(3)
+Z
+Y
-X
+X
-Z

FIG. 7A

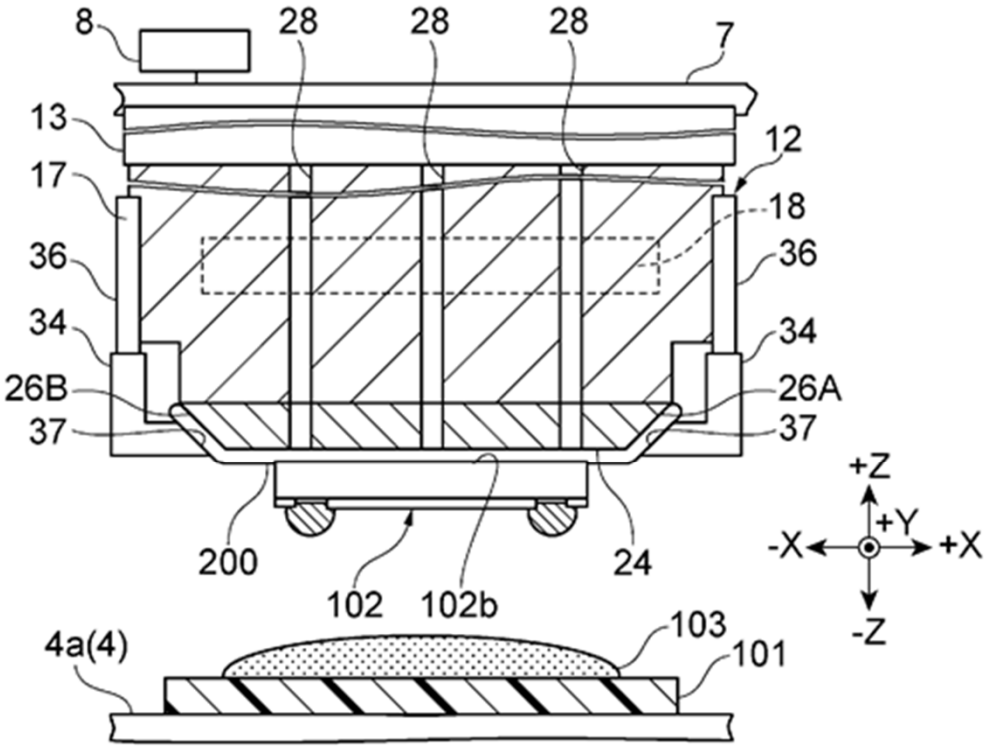
8
28
28
28
7
13
12
17
18
36
36
34
34
26B
26A
37
37
200
102
102b
24
4a(4)
103
101
+Z
+Y
-X
+X
-Z

FIG. 7B

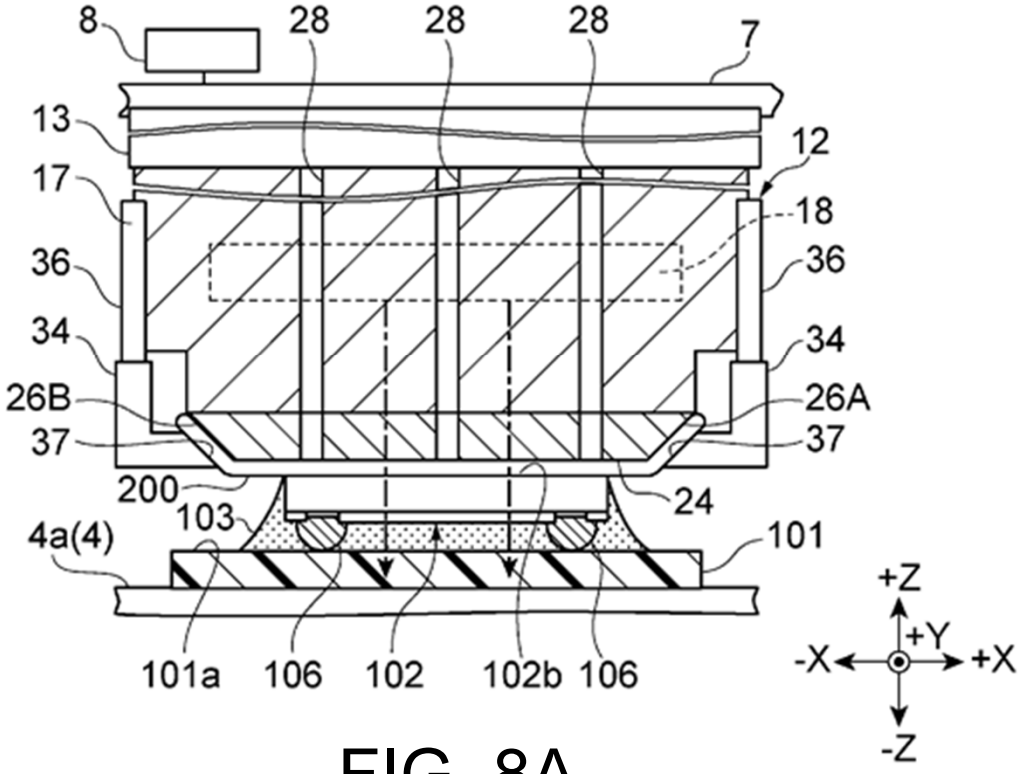
8
28
28
28
7
13
12
17
18
36
36
34
34
26B
26A
37
37
200
24
103
4a(4)
101
101a
106
102
102b
106
+Z
+Y
-X
+X
-Z

FIG. 8A

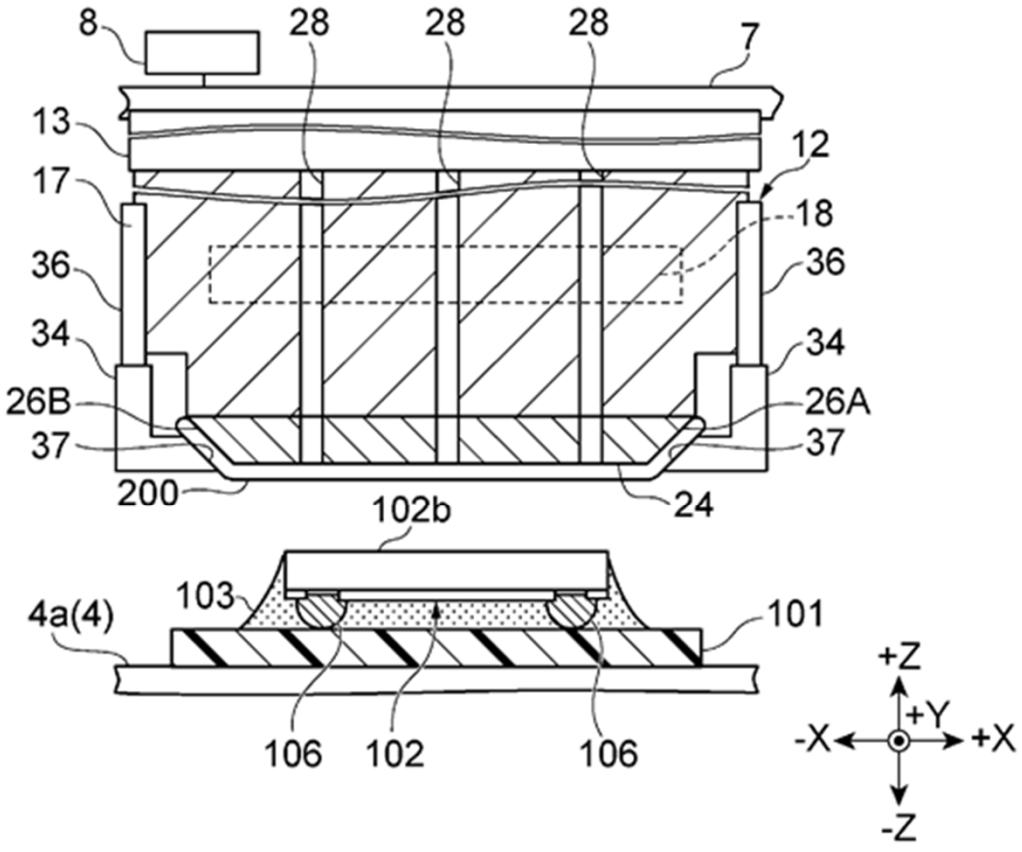
8
28
28
28
7
13
12
17
18
36
36
34
34
26B
26A
37
37
200
24
102b
103
4a(4)
101
106
102
106
+Z
+Y
-X
+X
-Z

FIG. 8B

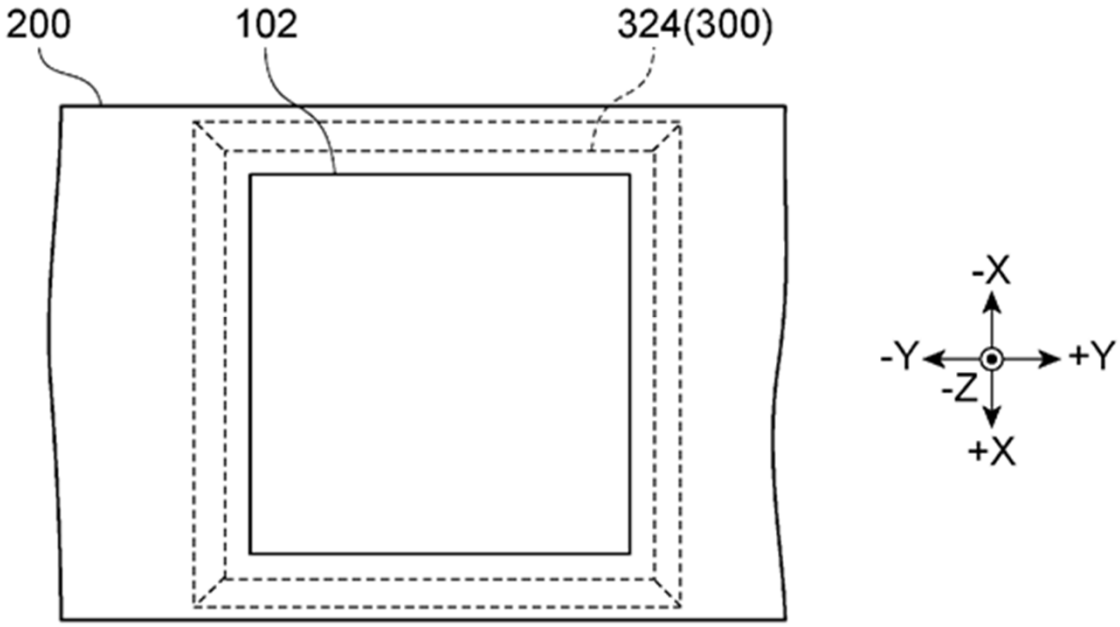

FIG. 9A

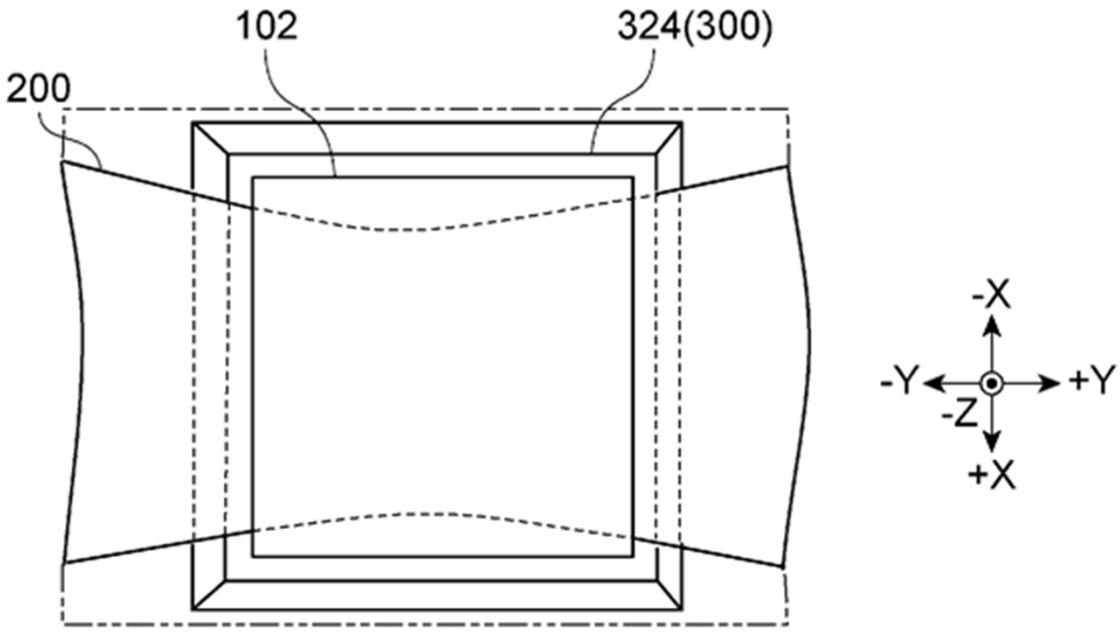

FIG. 9B

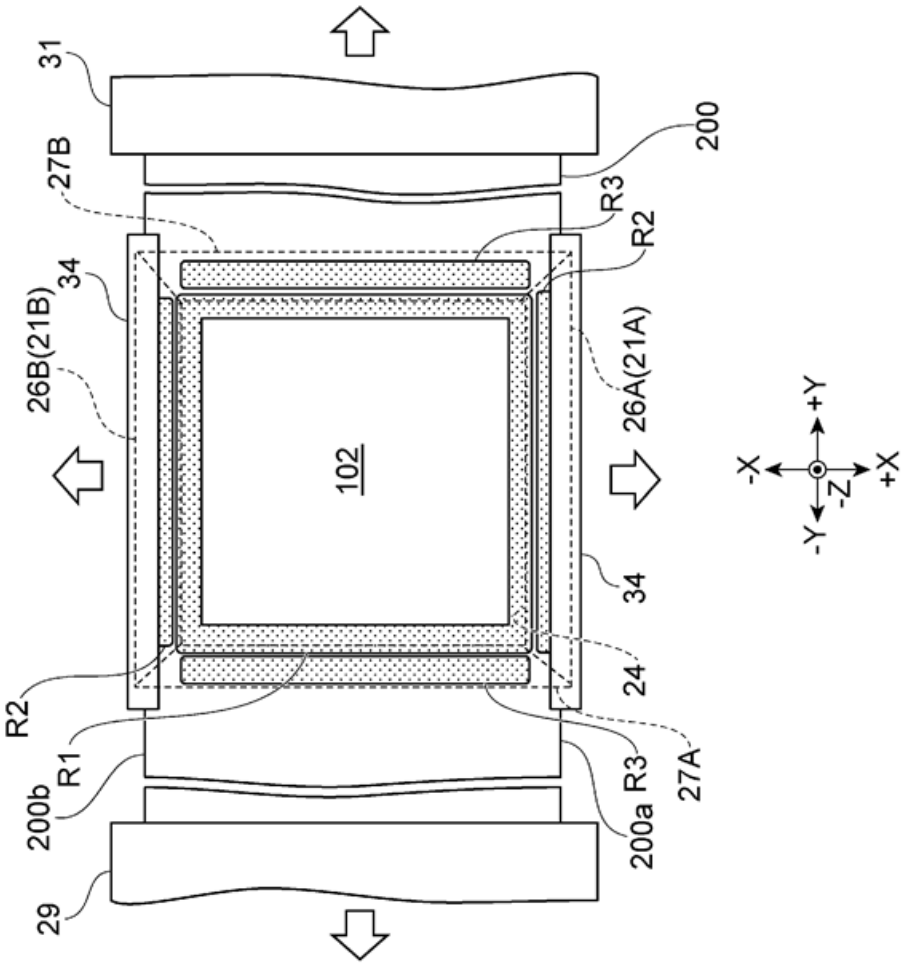
31
27B
200
R3
R2
34
26B(21B)
26A(21A)
102
34
24
R2
R1
27A
200b
200a
R3
29
+Y
-X
+X
-Z
-Y

FIG. 10

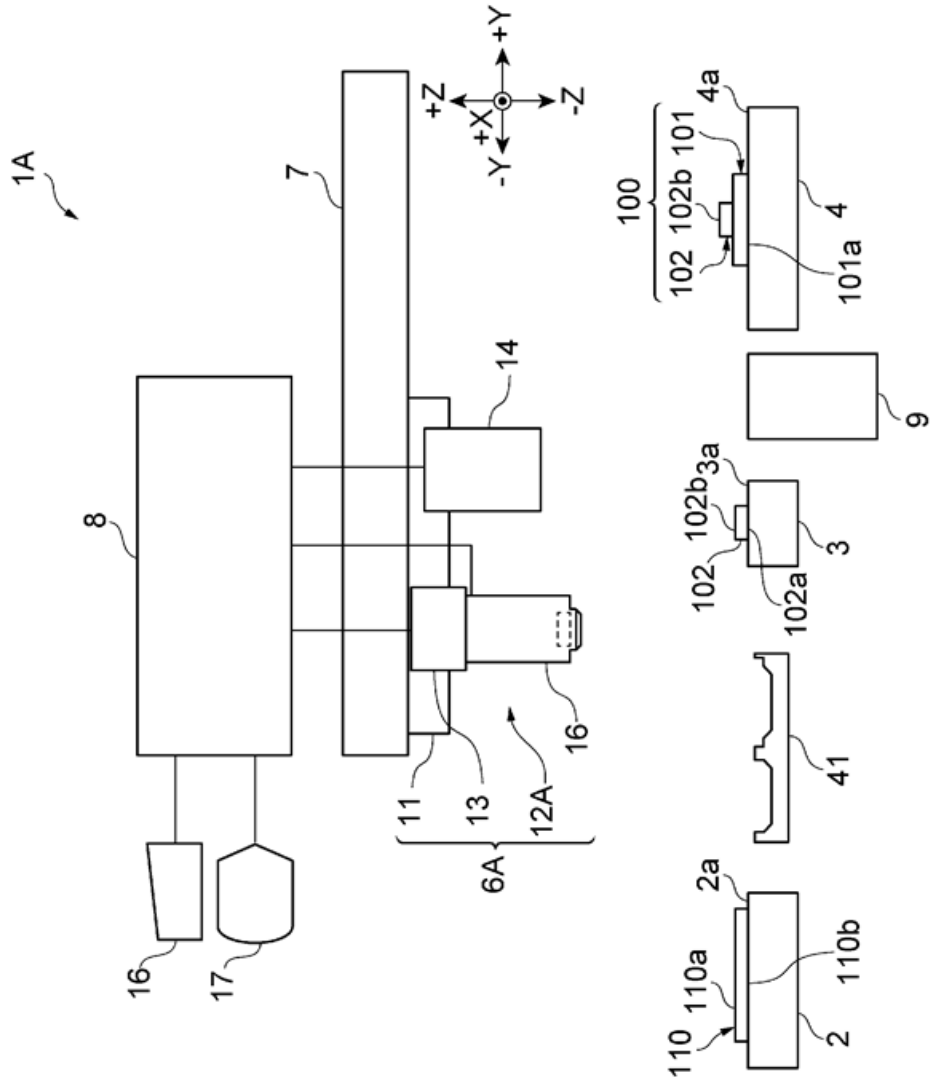
1A
7
+Z
+Y
-Z
+X
-Y
14
8
16
17
11
13
12A
16
6A
100
102
102b
101
4a
4
101a
9
3a
102b
102
102a
3
41
2a
110a
110b
110
2

FIG. 11

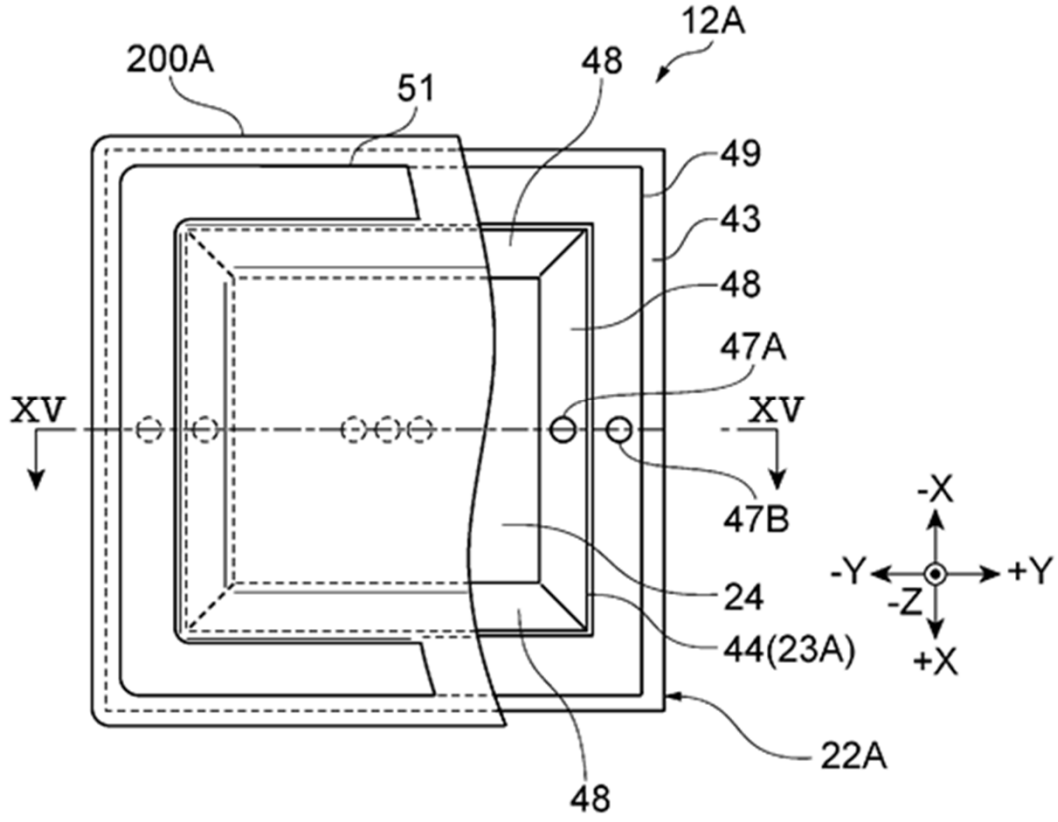

FIG. 12A

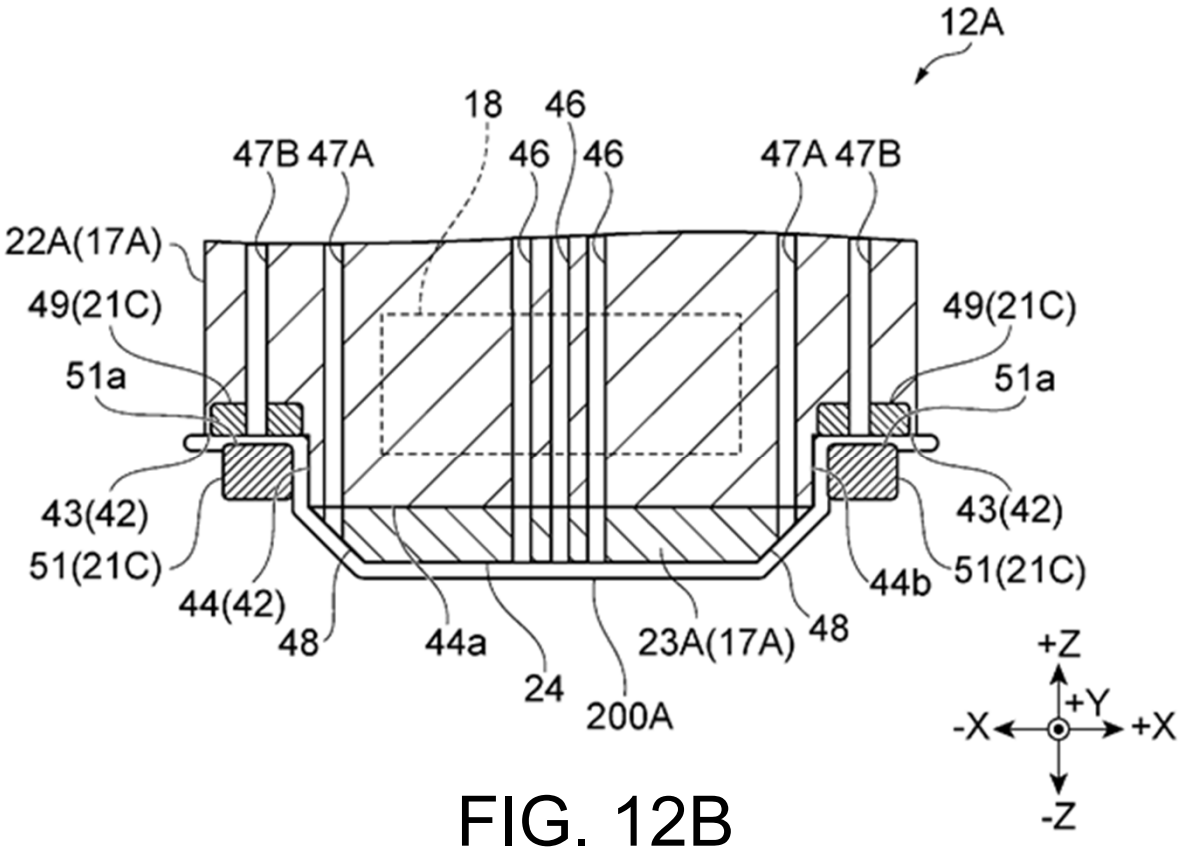

FIG. 12B

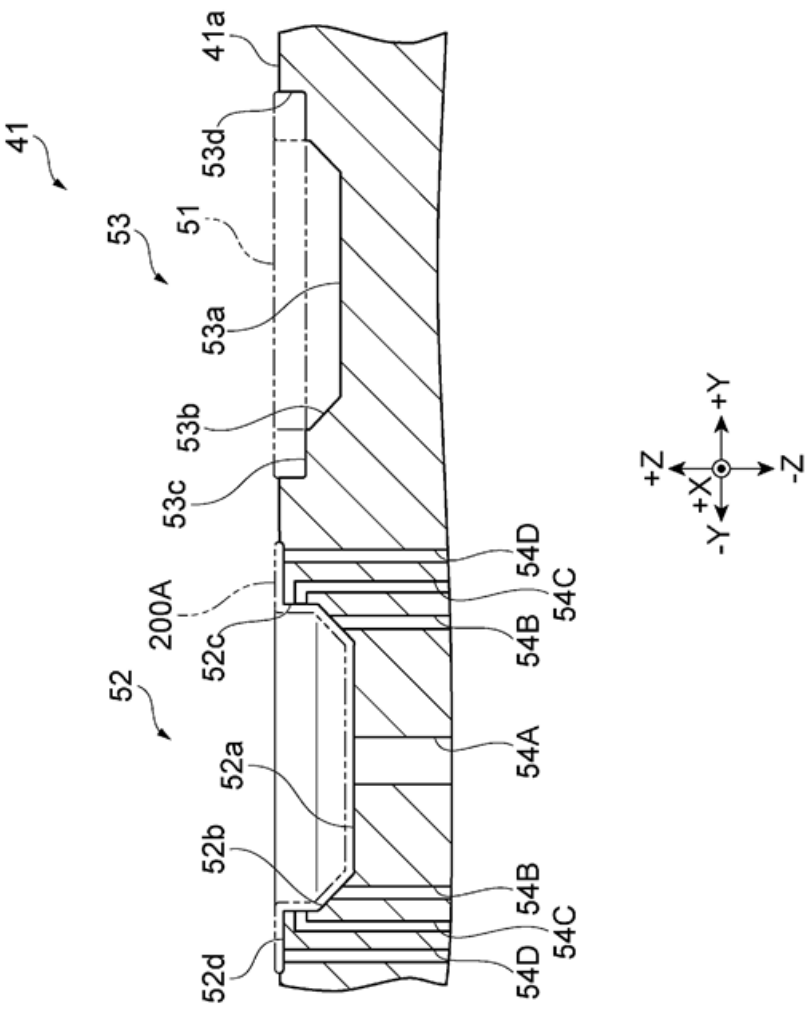
41
41a
53d
53
51
53a
53b
53c
200A
52c
52
52a
52b
52d
54D
54C
54B
54A
54B
54C
54D
+Z
-Z
+Y
-Y
+X

FIG. 13

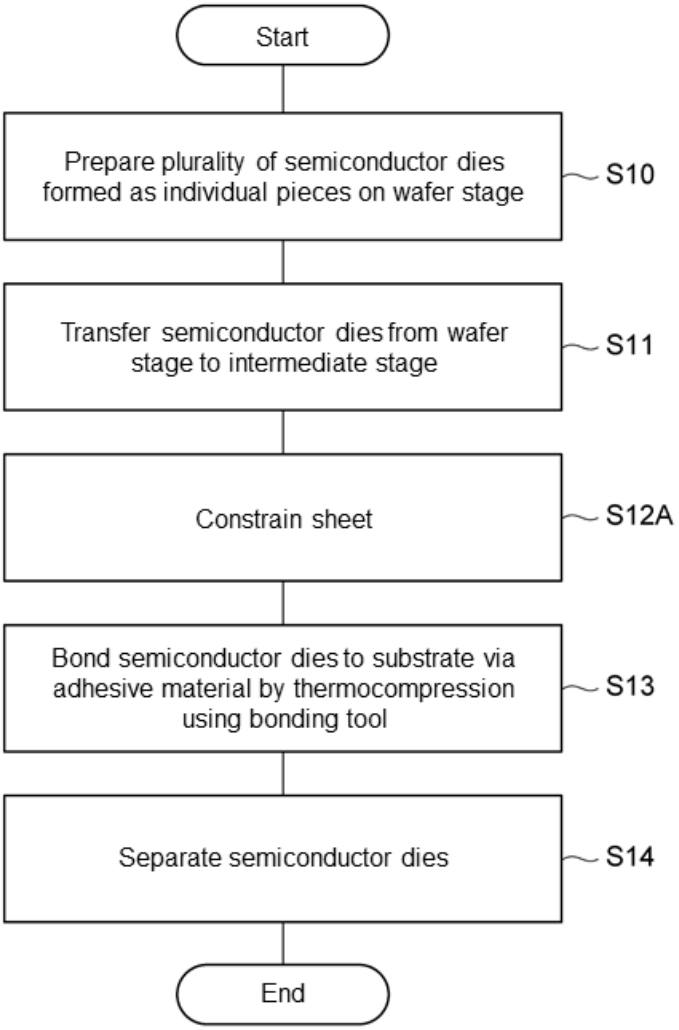
Start
Prepare plurality of semiconductor dies formed as individual pieces on wafer stage
S10
Transfer semiconductor dies from wafer stage to intermediate stage
S11
Constrain sheet
S12A
Bond semiconductor dies to substrate via adhesive material by thermocompression using bonding tool
S13
Separate semiconductor dies
S14
End

FIG. 14

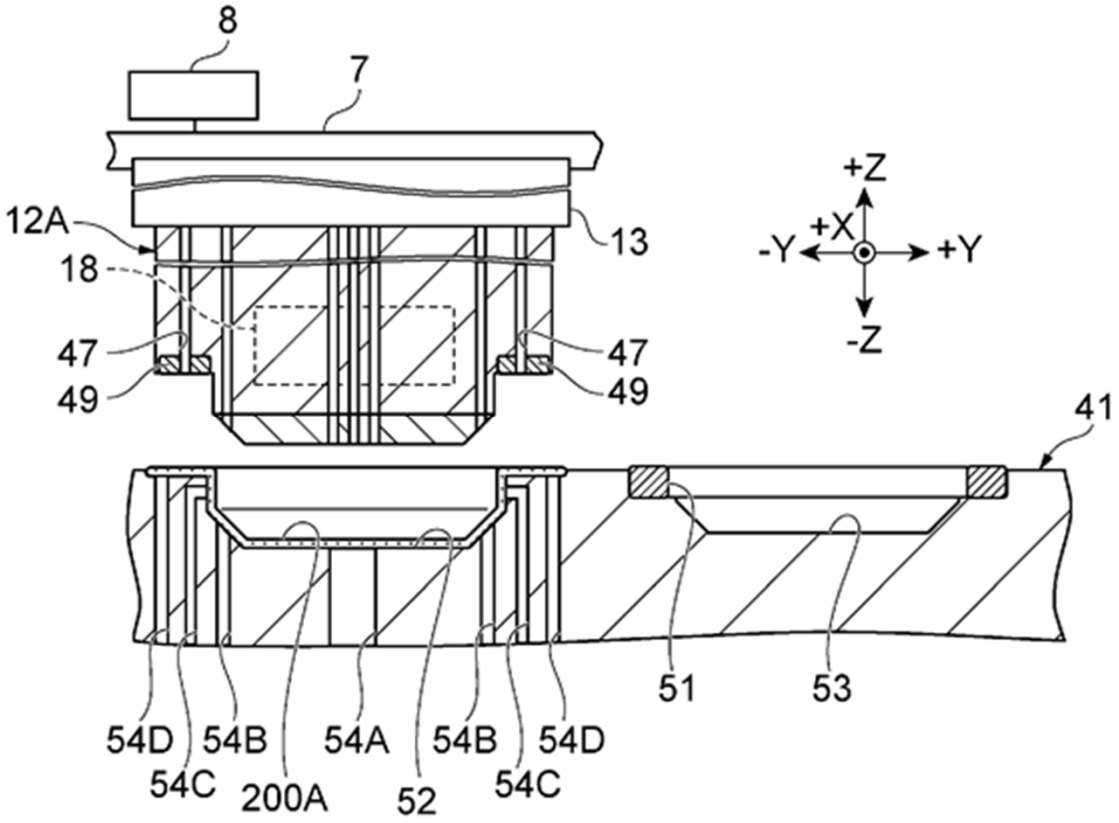

FIG. 15A

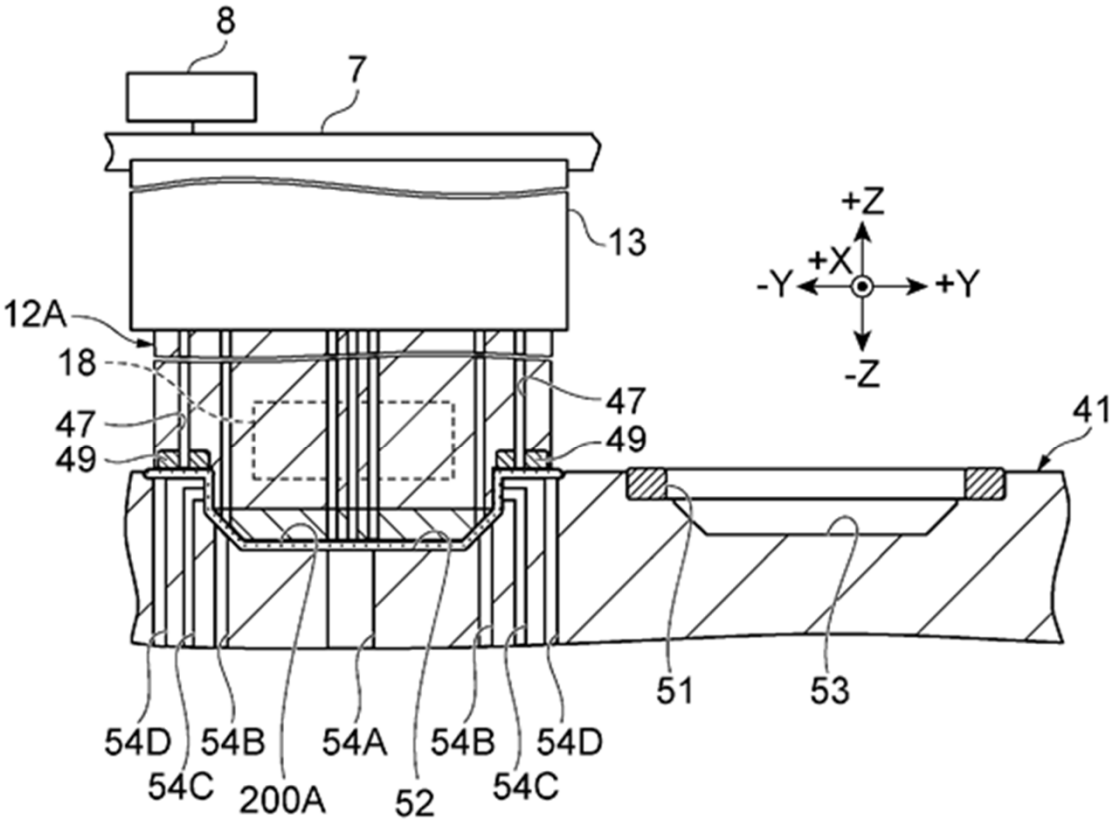

FIG. 15B

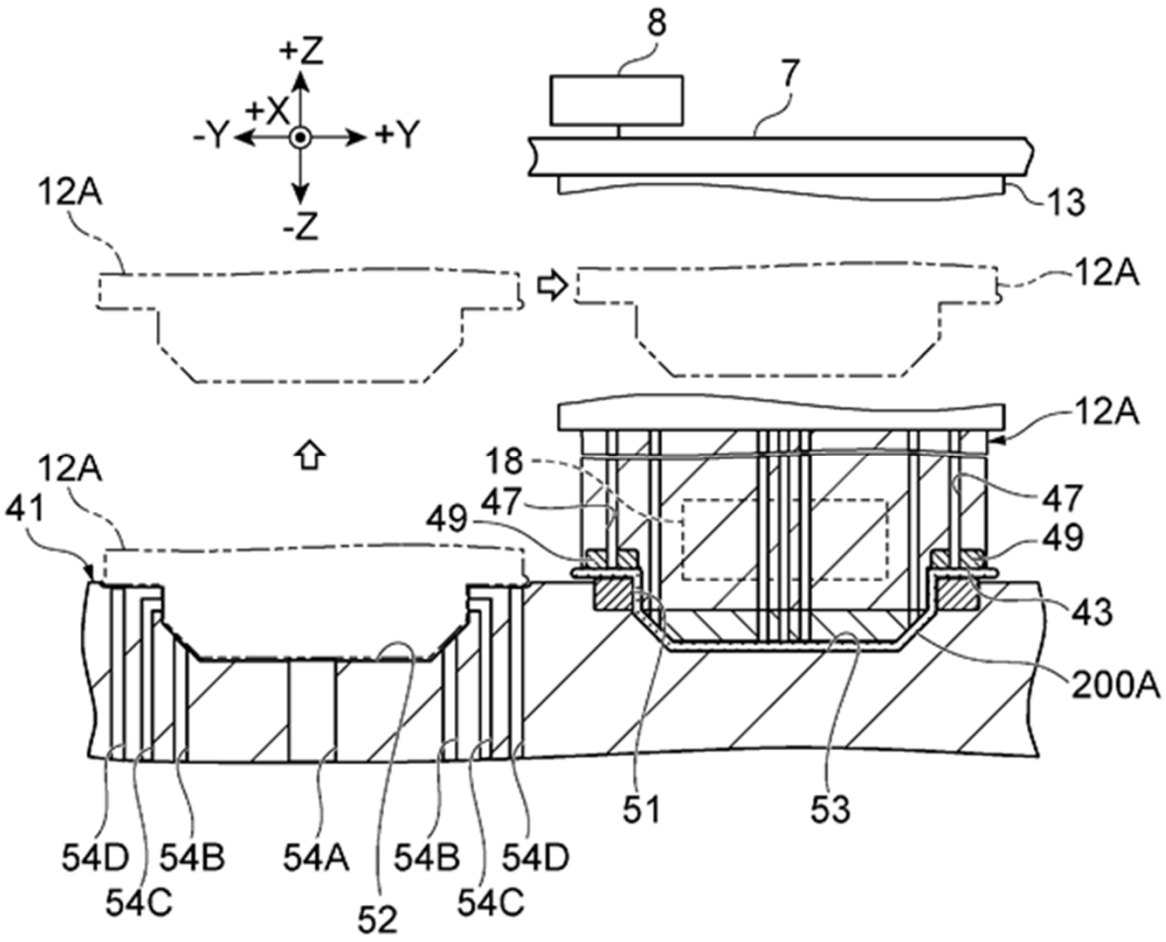

FIG. 16A

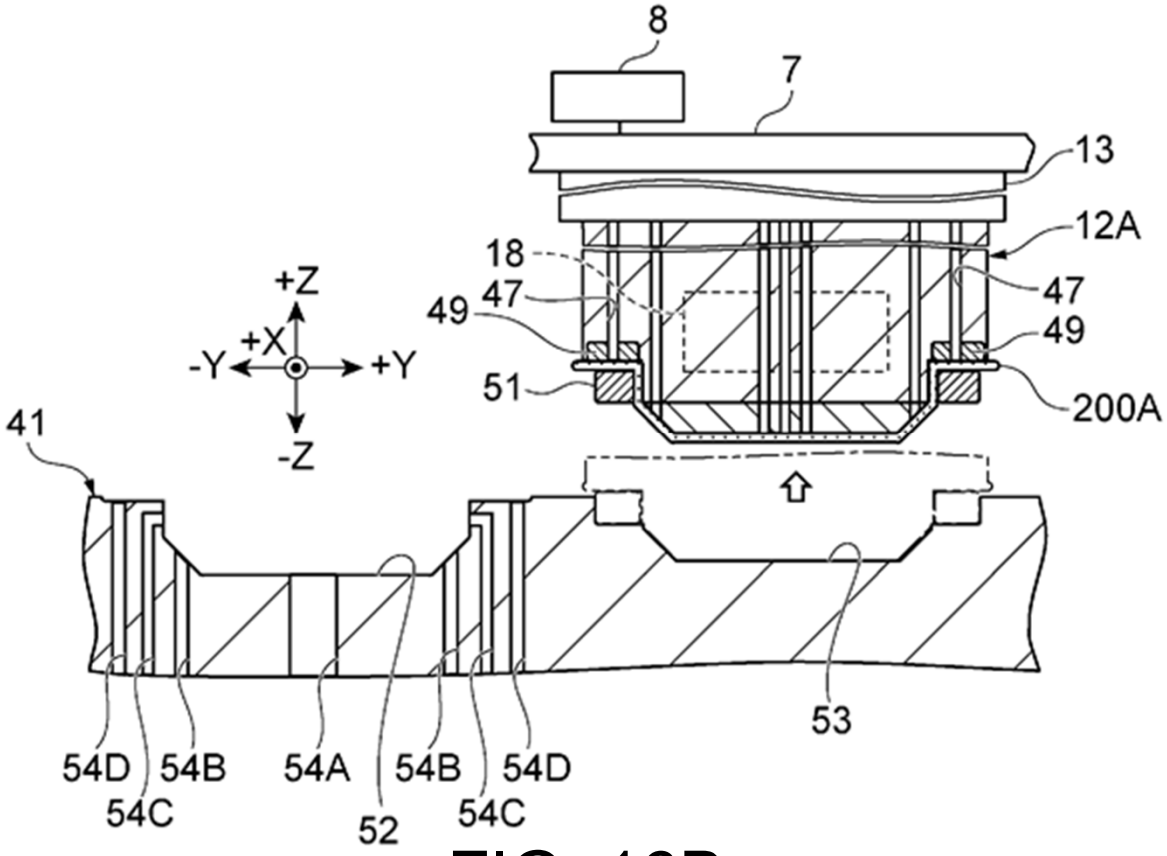

FIG. 16B

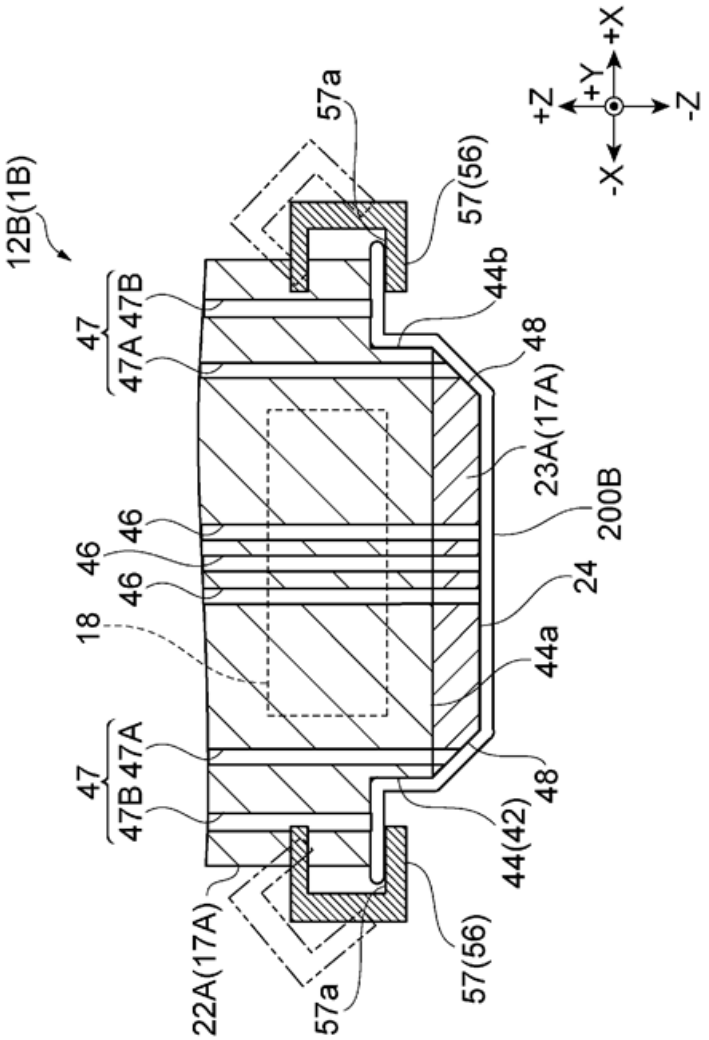
12B(1B)
47
47A
47B
46
46
46
18
47
47B
47A
22A(17A)
57a
57a
57(56)
57(56)
44b
48
23A(17A)
200B
24
44a
48
44(42)
+Z
+Y
+X
-X
-Z

FIG. 17

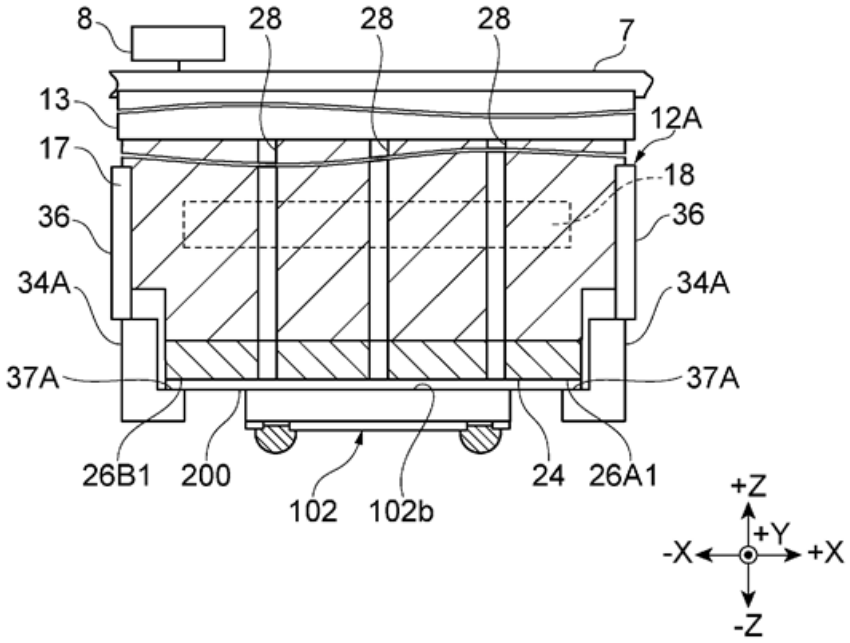
8
28
28
28
7
13
12A
17
18
36
36
34A
34A
37A
37A
26B1
200
102
102b
24
26A1
+Z
+Y
-X
+X
-Z

FIG. 18

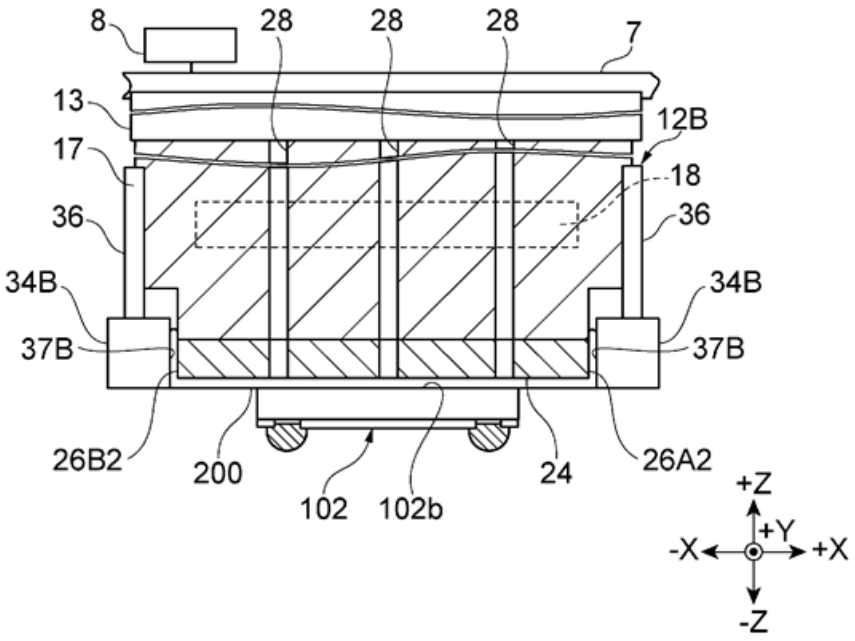
8
28
28
28
7
13
12B
17
18
36
36
34B
34B
37B
37B
26B2
200
102
102b
24
26A2
+Z
+Y
-X
+X
-Z

FIG. 19

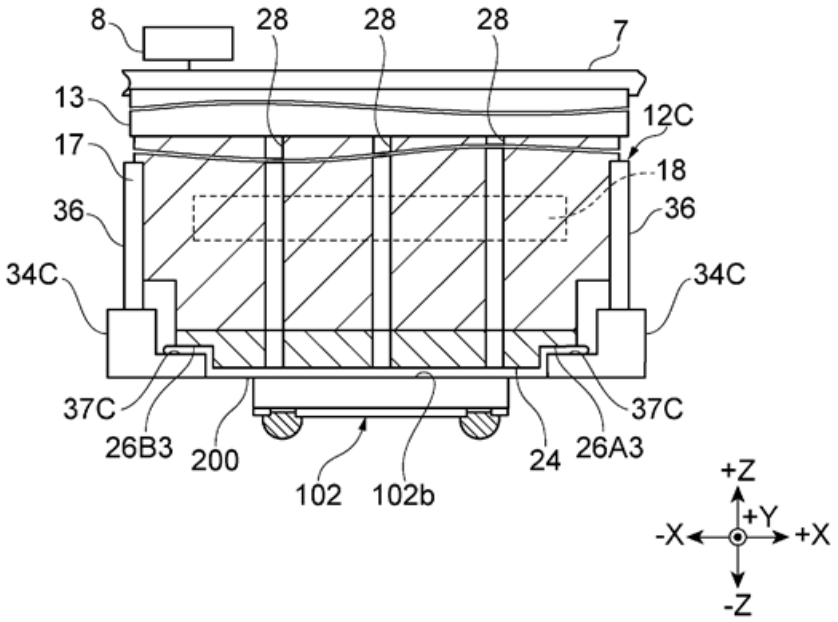
8
28
28
28
7
13
12C
17
18
36
36
34C
34C
37C
37C
26B3
200
102
102b
24
26A3
+Z
+Y
-X
+X
-Z

FIG. 20

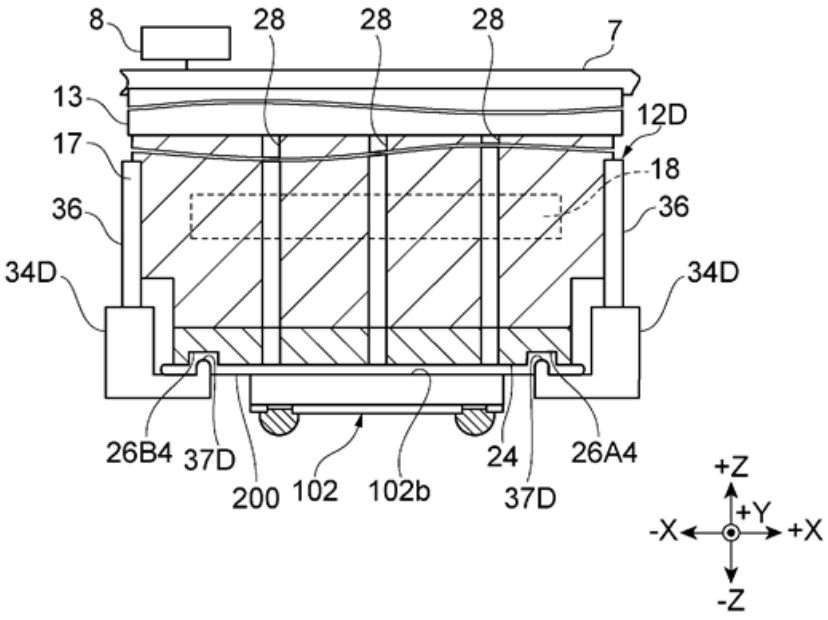
8
28
28
28
7
13
12D
17
18
36
36
34D
34D
26B4
37D
200
102
102b
24
37D
26A4
+Z
+Y
-X
+X
-Z

FIG. 21

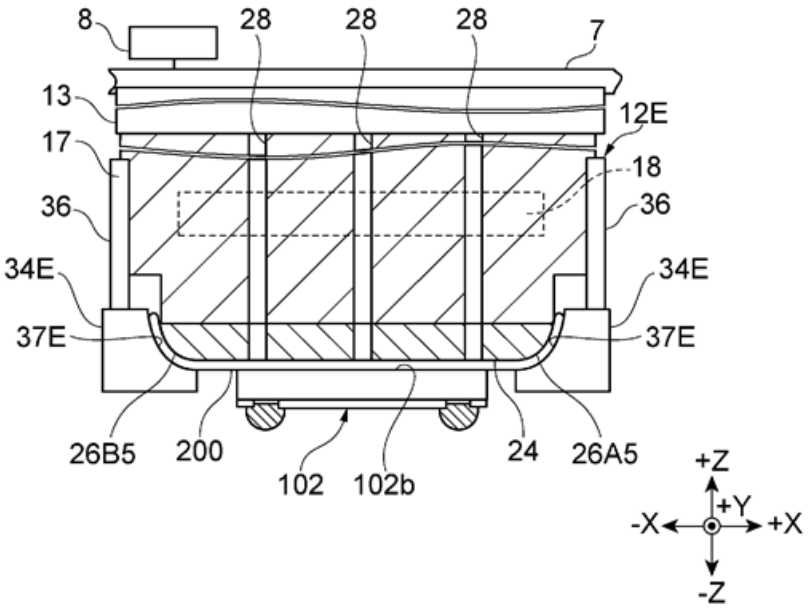
8
28
28
28
7
13
12E
17
18
36
36
34E
34E
37E
37E
26B5
200
102
102b
24
26A5
+Z
+Y
-X
+X
-Z

FIG. 22