ABSTRACT

AN OPTIMIZED Co/Ti-SALICIDE SCHEME FOR SHALLOW JUNCTION DEEP SUB-MICRON DEVICE FABRICATION

A new method is established to form different silicide layers over the top of the gate electrode and the surface of the source/drain regions. A thin layer of $TiSi_2$ is formed over the source/drain regions by depositing a layer of titanium and annealing this layer with the silicon substrate. The gate electrode is created as a recessed electrode, in the top recession of the electrode a layer of $CoSi_2$ is formed by depositing a layer of cobalt over the gate electrode. This layer of $CoSi_2$ serves as the electrical gate contact point.

(FIGURE 3 IS SUGGESTED FOR PUBLICATION)