

What is claimed is:

1. A method of operating an array of memory cells, the method comprising:
determining a first portion of a data state of a selected memory cell of the array of memory cells;
initiating a transfer of the determined first portion of the data state of the selected memory cell; and
determining a second portion of the data state of the selected memory cell at least partially concurrent with the transfer of the determined first portion of the data state of the selected memory cell.
2. The method of claim 1, wherein determining the first portion of the data state further comprises determining the first portion of the data state by completing a first sense phase.
3. The method of claim 2, wherein determining the second portion of the data state further comprises determining the second portion of the data state by completing a second sense phase.
4. The method of claim 3, wherein completing the first sense phase further comprises completing the first sense phase by applying an increasing sense potential to a control gate of the selected memory cell.
5. The method of claim 4, wherein completing the second sense phase further comprises completing the second sense phase by further increasing the sense potential being applied to the control gate of the selected memory cell after completing the first sense phase.
6. The method of any of claims 1-5, further comprising:
determining a first portion of a respective data state of each of a particular number of memory cells of the array of memory cells during a first sense phase, wherein the particular number of memory cells includes the selected memory cell;

initiating a second sense phase of the particular number of memory cells to determine a second portion of the respective data state of at least some of the particular number of memory cells including the selected memory cell; and
initiating a transfer of the determined first portions of the data states of each of the particular number of memory cells during the second sense phase.

7. The method of any of claims 1-5, further comprising:
wherein the first sense phase comprises applying a first increasing sense potential having a first range to the selected memory cell to determine a first data value from the selected memory cell;
wherein the second sense phase comprises applying a second increasing sense potential having a second range to the selected memory cell to determine a second data value from the selected memory cell.
8. The method of claim 7, wherein the first range and the second range comprise a substantially continuous range.
9. An apparatus, comprising:
an array of memory cells; and
a controller, wherein the controller is configured to cause one or more first sense operations to be performed on a selected memory cell to determine a first portion of a data state of the selected memory cell, and to cause one or more second sense operations to be performed on the selected memory cell to determine a second portion of the data state of the selected memory cell;
wherein the controller is further configured to cause the first portion of the data state to be transferred at least partially concurrent with at least one of the one or more of the second sense operations performed on the selected memory cell.
10. The apparatus of claim 9, wherein each memory cell is configured to store one of a plurality of data states, where each data state is representative of a particular bit pattern.

11. The apparatus of claim 9 or 10, further comprising:
a first register; and
a second register;
wherein the first register is configured to store the determined first portion of the data state of the selected memory cell, and where the second register is configured to store the determined second portion of the data state of the selected memory cell.
12. The apparatus of claim 11, wherein the controller is further configured to cause the first portion of the data state stored in the first register to be transferred out of the first register at least partially concurrent with at least one of the one or more second sense operations performed on the selected memory cell.
13. The apparatus of claim 9 or 10, wherein the controller is further configured to cause an initial sense operation to be performed on the selected memory cell prior to the one or more first sense operations to determine if the selected memory cell has a particular data state comprising a known first data portion and a known second data portion.
14. The apparatus of claim 13, wherein the known first data portion and the known second data portion are the same.

What is claimed is:

1. A method of operating an array of memory cells, the method comprising:
determining a first portion of a data state of a selected memory cell of the array of memory cells;
initiating a transfer of the determined first portion of the data state of the selected memory cell; and
determining a second portion of the data state of the selected memory cell at least partially concurrent with the transfer of the determined first portion of the data state of the selected memory cell.
2. The method of claim 1, wherein determining the first portion of the data state further comprises determining the first portion of the data state by completing a first sense phase.
3. The method of claim 2, wherein determining the second portion of the data state further comprises determining the second portion of the data state by completing a second sense phase.
4. The method of claim 3, wherein completing the first sense phase further comprises completing the first sense phase by applying an increasing sense potential to a control gate of the selected memory cell.
5. The method of claim 4, wherein completing the second sense phase further comprises completing the second sense phase by further increasing the sense potential being applied to the control gate of the selected memory cell after completing the first sense phase.
6. A method of operating an array of memory cells, the method comprising:
determining a first portion of a respective data state of each of a particular number of memory cells of the array during a first sense phase;

initiating a second sense phase of the particular number of memory cells to determine a second portion of the respective data state of at least some of the particular number of memory cells; and

initiating a transfer of the determined first portions of the data states of each of the particular number of memory cells during the second sense phase.

7. The method of claim 6, wherein initiating a transfer of the determined first portions of the data states further comprises initiating a transfer of the determined first portions of the data states out of a memory device that includes the particular number of memory cells.
8. A method of operating an array of multi-level memory cells, the method comprising:
performing one or more sense operations on a plurality of selected memory cells of the array during a first sense phase to determine a first portion of a respective data state of each of the selected memory cells;
performing one or more sense operations on the plurality of selected memory cells during a second sense phase to determine a second portion of the respective data state of at least some of the selected memory cells; and
initiating a transfer of the determined first data state portions;
wherein at least a portion of the second sense phase occurs during the transfer of the determined first data state portions.
9. The method of claim 8, wherein initiating a transfer further comprises initiating a transfer of the determined first data state portions prior to beginning the second sense phase.
10. The method of claim 8, wherein initiating a transfer further comprises initiating a transfer of the determined first data state portions substantially concurrently with beginning the second sense phase.

11. The method of claim 8, wherein initiating a transfer further comprises initiating a transfer of the determined first data state portions after beginning the second sense phase.
12. The method of claim 8, further comprising storing the determined first data state and the determined second data state portions in register circuitry of the memory device.
13. The method of claim 12, wherein initiating a transfer of the determined first data state portions further comprises initiating a transfer to shift the determined first data state portions out of the register circuitry prior to storing all of the determined second data state portions in the register circuitry.
14. The method of claim 8, further comprising performing an initial sense operation during the first sense phase to determine if one or more of the plurality of selected memory cells have a particular data state.
15. The method of claim 14, wherein the particular data state comprises an erased data state.
16. A method of operating an array of memory cells, the method comprising:
performing one or more first sense operations on one or more selected memory cells of the array during a first sense phase to determine a first portion of a respective data state of each selected memory cell;
performing one or more second sense operations on the one or more selected memory cells during a second sense phase to determine a second portion of the respective data state of at least one of the one or more selected memory cells;
and
initiating a transfer of the first portion of data states of the one or more selected memory cells while performing the one or more second sense operations.
17. The method of claim 16, wherein performing the one or more first sense operations further comprises performing the one or more first sense operations responsive to an

external read request received by a memory device including the array of memory cells.

18. The method of claim 16, wherein initiating a transfer of the first portion of data states further comprises initiating a transfer of at least a portion of the first determined portion of data states out of a memory device including the array of memory cells prior to completing the second sense phase.
19. A method of operating an array of memory cells, the method comprising:
applying a first increasing sense potential having a first range to a selected memory cell of the array to determine a first data value from the selected memory cell;
applying a second increasing sense potential having a second range to the selected memory cell to determine a second data value from the selected memory cell;
and
initiating a transfer of the first data value while determining the second data value of the selected memory cell.
20. The method of claim 19, wherein the first range and the second range comprise a substantially continuous range.
21. The method of claim 19, wherein the first data value comprises a first bit value and where the second data value comprises a second bit value.
22. An apparatus, comprising:
an array of memory cells; and
a controller, wherein the controller is configured to cause one or more first sense operations to be performed on a selected memory cell to determine a first portion of a data state of the selected memory cell, and to cause one or more second sense operations to be performed on the selected memory cell to determine a second portion of the data state of the selected memory cell;

wherein the controller is further configured to cause the first portion of the data state to be transferred at least partially concurrent with at least one of the one or more of the second sense operations performed on the selected memory cell.

23. The apparatus of claim 22, wherein the array of memory cells comprise an array of multilevel memory cells.
24. The apparatus of claim 23, wherein each memory cell is configured to store one of a plurality of data states, where each data state is representative of a particular bit pattern.
25. The apparatus of claim 24, wherein the first portion comprises a first bit value of the particular bit pattern and the second portion comprises a second bit value of the particular bit pattern.
26. The apparatus of claim 22, further comprising a memory device interface.
27. The apparatus of claim 26, wherein the memory device interface comprises a SPI bus.
28. The apparatus of claim 22, wherein the array of memory cells comprises an array of non-volatile memory cells.
29. The apparatus of claim 28, wherein the array of memory cells comprises an array of NAND configured non-volatile memory cells.
30. The apparatus of claim 28, wherein the array of memory cells comprises an array of NOR configured non-volatile memory cells.
31. The apparatus of claim 22, further comprising:
a first register; and
a second register;

wherein the first register is configured to store the determined first portion of the data state of the selected memory cell, and where the second register is configured to store the determined second portion of the data state of the selected memory cell.

32. The apparatus of claim 31, wherein the controller is further configured to cause the first portion of the data state stored in the first register to be transferred out of the first register at least partially concurrent with at least one of the one or more second sense operations performed on the selected memory cell.
33. The apparatus of claim 22, wherein the controller is further configured to cause an initial sense operation to be performed on the selected memory cell prior to the one or more first sense operations to determine if the selected memory cell has a particular data state comprising a known first data portion and a known second data portion.
34. The apparatus of claim 33, wherein the known first data portion and the known second data portion are the same.
35. The apparatus of claim 33, wherein the particular data state comprises an erased data state of the selected memory cell.
36. An electronic system, comprising:
 - a communications channel;
 - a memory access device coupled to the communications channel and configured to generate memory device commands; and
 - a memory device coupled to the communications channel and configured to be responsive to the memory device commands, the memory device comprising:
 - an array of memory cells; and
 - control circuitry, wherein the control circuitry is configured to determine a first portion of a data state of each of one or more selected memory cells of the array of memory cells, determine a second portion of the data states of the one or more selected memory cells, and initiate a

transfer from the memory device of the determined first portions of the data states of the one or more selected memory cells at least partially concurrent with the determination of the second portion of the data states of each of the one or more selected memory cells.

37. The apparatus of claim 36, wherein the controller is further configured to cause the determined second portions of data states to be transferred from the memory device following the transfer of the determined first portions of data states from the memory device.
38. The apparatus of claim 37, wherein the controller is further configured to cause the determined first portions and second portions of data states to be transferred responsive to a read request memory device command generated by the memory access device and received by the memory device over the communications channel.