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Abstract of the Disclosure

A high quality dielectric layer (35), typically silicon dioxide, is formed on a multi-layer deposited semiconductor structure (31, 32, 33, 34), typically polysilicon or amorphous silicon. The multi-layer structure is formed by varying the silicon deposition rate so as to obtain a low stress deposited silicon structure. The low stress allows for a higher quality dielectric to be formed on the exposed top surface. One application is for thin film transistor gate oxides. Other applications included capacitor dielectrics and the tunnel oxide on the floating gate of EEPROMs.

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