WHAT IS CLAIMED IS:

1. An integrated circuit device comprising:

registers each including two or more bit storages;

a shuffler configured to receive an address indicating one of the registers and data bits, to select target bit storages, at which the data bits are to be stored, from among bit storages of the registers depending on a shuffle configuration and the address, to store the data bits into the target bit storages, and to transfer the data bits from the target bit storages depending on the shuffle configuration; and

a logic unit configured to receive the data bits transferred from the shuffler and to operate using the received data bits,

wherein the shuffler is configured to adjust the shuffle configuration when a reset operation is performed,

wherein the shuffler comprises:

an address converter configured to receive the address and to generate a converted address from the address depending on the shuffle configuration;

an address decoder configured to select first bit storages of a first register, which is not assigned to a range of the address, from among the registers as the target bit storages when the converted address satisfies a dummy condition of the shuffle configuration, to select second bit storages of a second register, indicated by the converted address, from among the registers as the target bit storages when the converted address does not satisfy the dummy condition, and to transfer the data bits to the target bit storages; and

a restorer configured to transfer the data bits from one of the first register and the second register to the logic unit depending on the shuffle configuration.

2. The integrated circuit device of claim 1, wherein the shuffle configuration includes a random number including two or more bits, and

wherein the address converter is configured to generate the converted address from the address by performing an exclusive OR operation on first bits of the random number and the address.

3. The integrated circuit device of claim 1, wherein the logic unit includes inputs respectively corresponding to the range of address, and

wherein the restorer is configured to select one of the first register and the second register to be connected to an input of the inputs depending on the dummy condition.

4. The integrated circuit device of claim 1, wherein the shuffle configuration includes a random number including two or more bits, and

wherein the address converter is configured to generate the converted address by performing an exclusive OR operation on at least one first bit of the random number and at least one second bit of bits of the address.

5. The integrated circuit device of claim 1, wherein the shuffle configuration includes a random number including two or more bits, and

wherein the address converter is configured to generate the converted address from the address by performing an exclusive OR operation on first bits of the random number and the address, and to determine that the dummy condition is satisfied when a value of the converted address matches a value of second bits of the random number.

6. The integrated circuit device of claim 1, wherein the shuffler further comprises:

an offset converter configured to rearrange the data bits, which are arranged in a first order, in a second order depending on the shuffle configuration.

7. The integrated circuit device of claim 6, wherein the shuffle configuration includes a random number including two or more bits, and

wherein the offset converter is configured to

generate second offset bits that indicate the second order by performing an exclusive OR operation on first offset bits that indicate the first order of the data bits and first bits of the random number, and

rearrange the data bits depending on the second offset bits.

8. The integrated circuit device of claim 6, wherein the shuffle configuration includes a random number including two or more bits, and

wherein the offset converter is configured to

select first bits of the bits of the random number depending on the address,

generate second offset bits that indicate the second order by performing an exclusive OR operation on first offset bits that indicate the first order of the data bits and the first bits of the random number, and

rearrange the data bits depending on the second offset bits.

9. The integrated circuit device of claim 6, wherein the shuffle configuration includes a random number including two or more bits, and

wherein the offset converter is configured to

generate second offset bits that indicate the second order by performing an exclusive OR operation on at least one of first offset bits that indicate the first order of the data bits and at least one second bit of the random number, and

rearrange the data bits depending on the second offset bits.

10. The integrated circuit device of claim 1, wherein the shuffle configuration includes a random number, and

wherein the random number is newly generated when the reset operation is performed.

11. An integrated circuit device comprising:

a processor core configured to output an address and a key including two or more data bits;

a power manager configured to activate a reset signal when a reset operation is performed;

a random number generator configured to generate a random number in response to the reset signal; and

a peripheral circuit configured to store the key in response to the address and the random number and to perform encryption or decryption in response to the key,

wherein the peripheral circuit comprises

registers each including two or more bit storages, and

a shuffler configured to adjust target bit storages, at which the key is to be stored, from among bit storages of the registers depending on the address and the random number.

12. The integrated circuit device of claim 11, wherein the shuffler is configured to adjust the target bit storages by converting at least one of the address and an order of the two or more data bits of the key.

13. The integrated circuit device of claim 11 or claim 12, wherein the peripheral circuit further comprises:

a logic unit configured to perform the encryption or the decryption using the key, and

wherein the shuffler is configured to transfer the key from the target bit storages to the logic unit depending on the random number.

14. The integrated circuit device of any one of claims 11 to 13, wherein the bit storages of the registers include a dummy register which is not identified by the address, and

wherein the dummy register includes dummy bit storages which are selected as all or a part of the target bit storages depending on the random number.

15. An operation method of an integrated circuit device which includes registers, a shuffler, and a logic unit, the method comprising:

receiving, by the shuffler, a random number responsive to a detected reset;

receiving, by the shuffler, an address and data bits;

selecting, by the shuffler, bit storages of first registers of the registers as target bit storages depending on the random number and the address in response to satisfying a dummy condition; and

selecting, by the shuffler, bit storages of second registers of the registers as target bit storages based on the random number and the address in response not to satisfying the dummy condition, the second registers being different from the first registers;

storing, by the shuffler, the data bits into the target bit storages.

16. The method of claim 15, further comprising:

transferring, by the shuffler, the data bits from the target bit storages to the logic unit depending on the random number and the dummy condition.