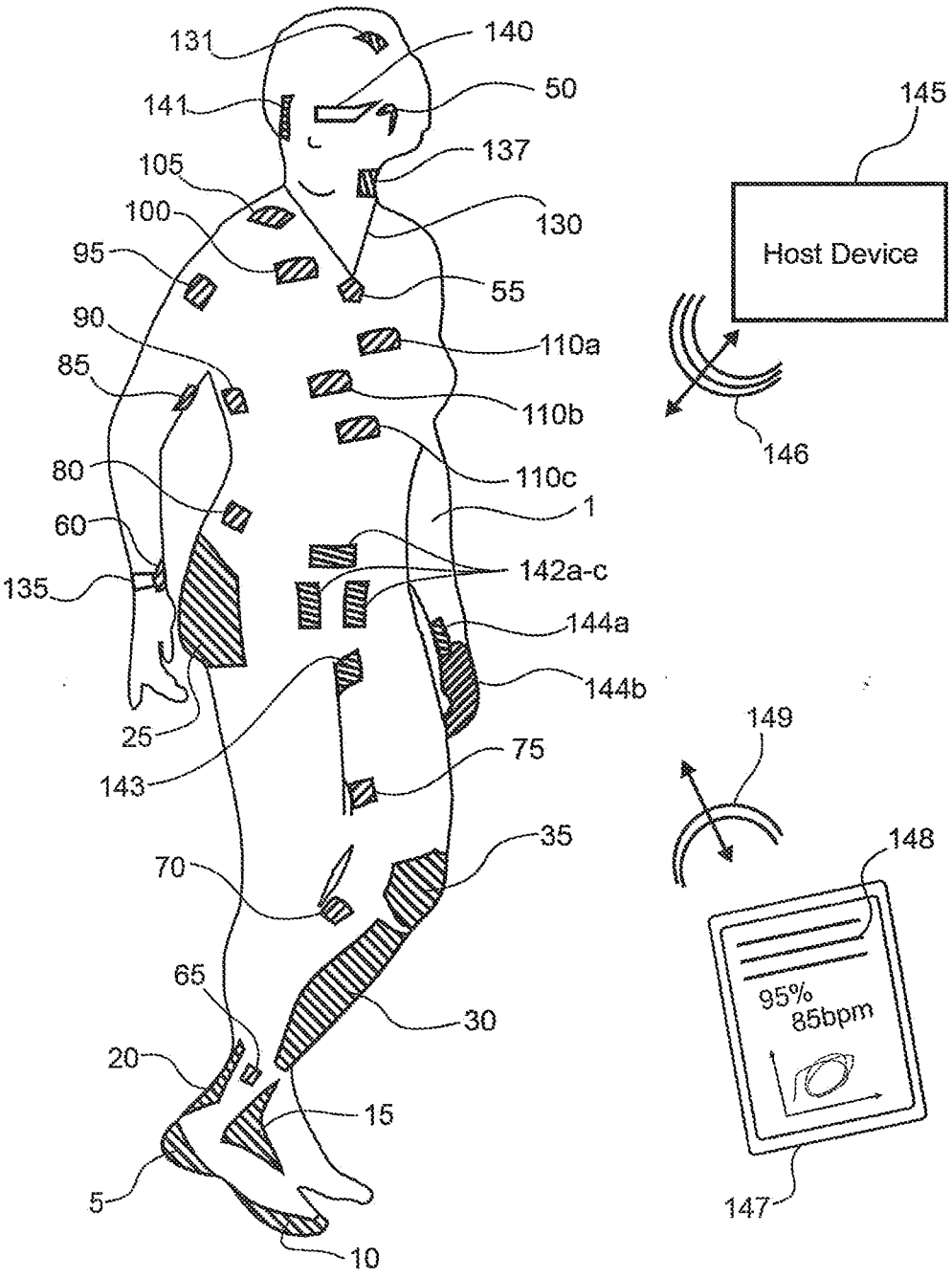

131
140
141
50
145
105
137
100
130
Host Device
95
55
90
110a
85
110b
146
110c
80
1
60
142a-c
135
144a
144b
149
25
75
143
35
148
70
65
95%
85bpm
30
20
15
5
147
10

Fig 1a

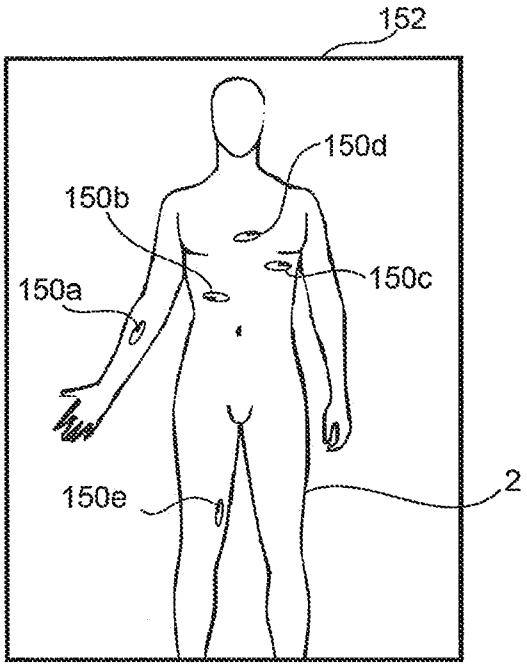


Fig 1b

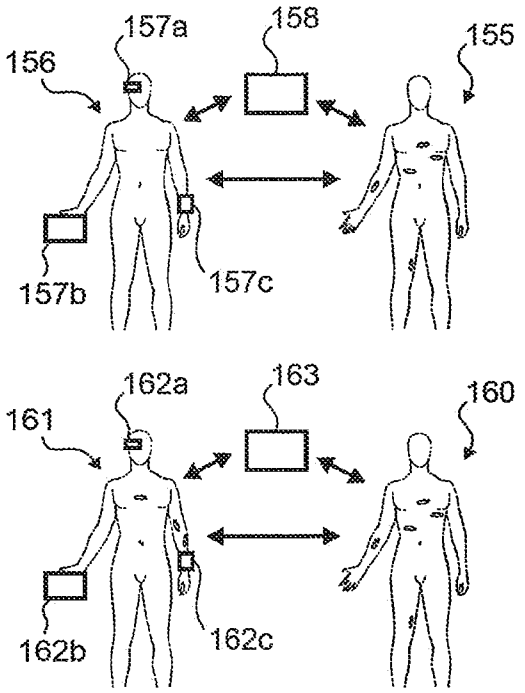


Fig 1c

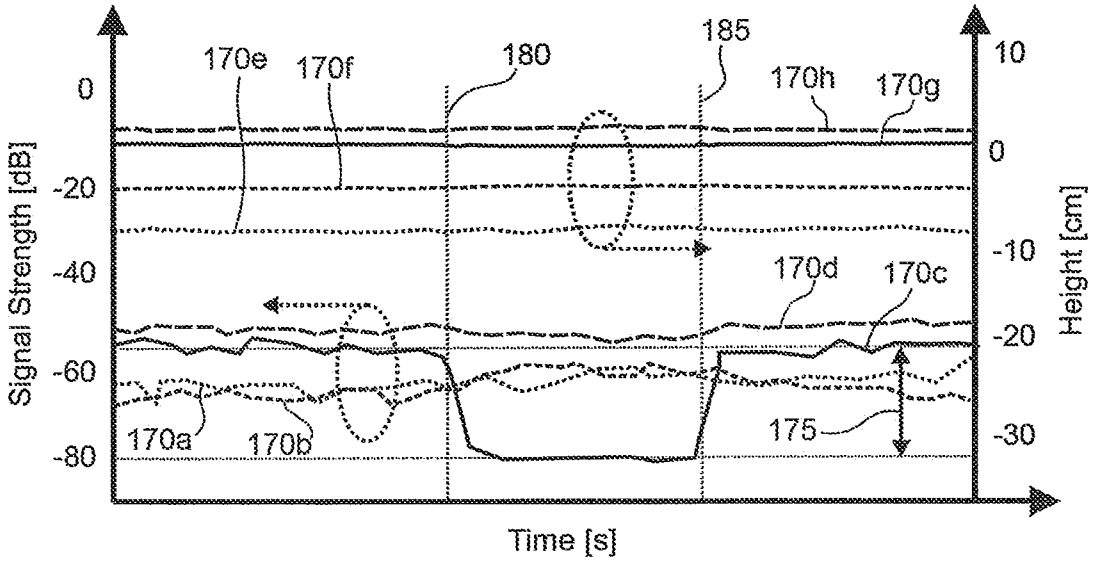


Fig 1d

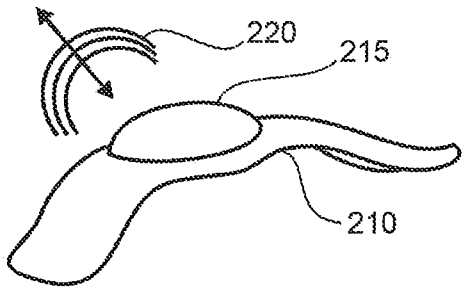
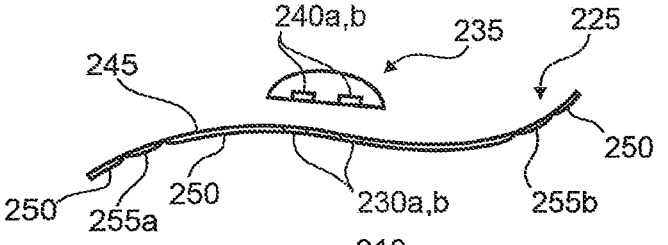


Fig 2a



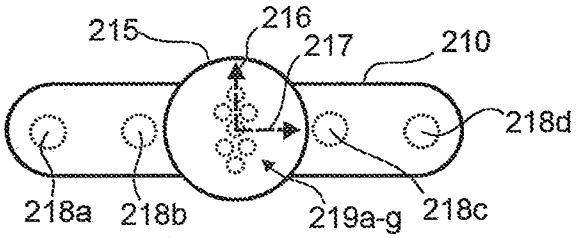


Fig 2b

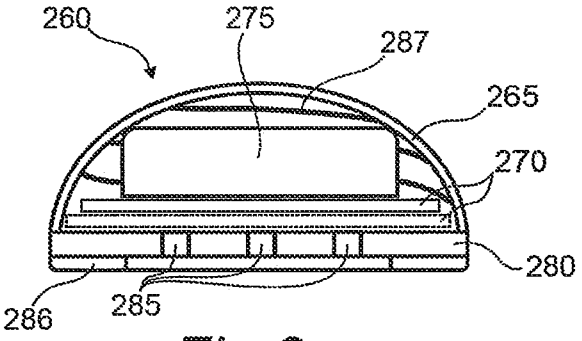


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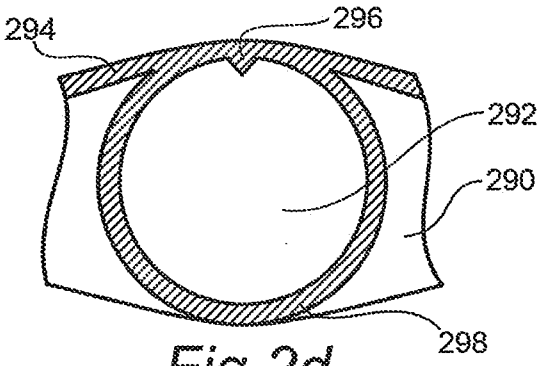


Fig 2d

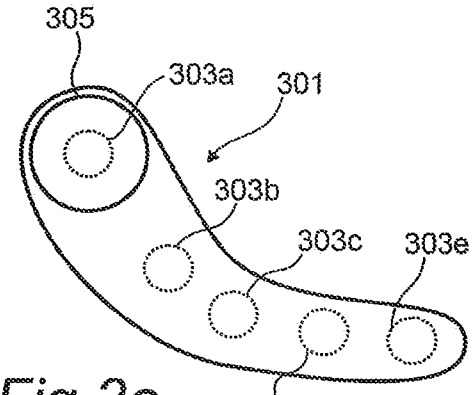


Fig 3a

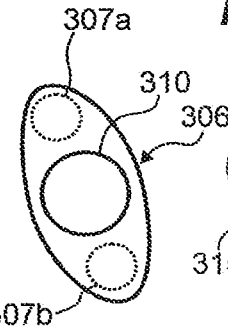


Fig 3b

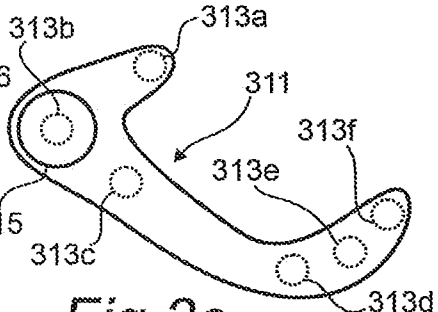


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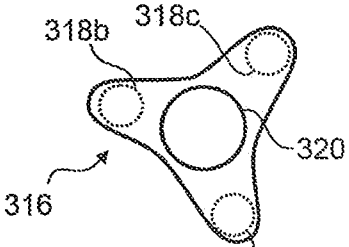


Fig 3d

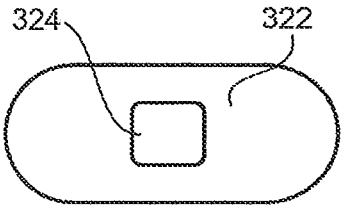


Fig 3e

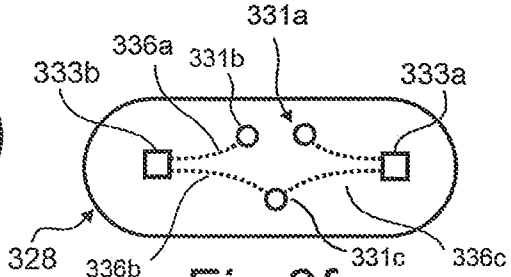


Fig 3f

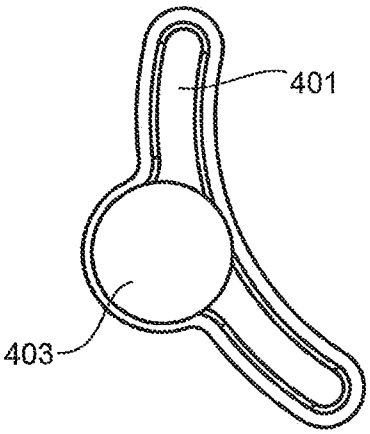


Fig 4a

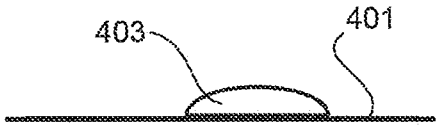


Fig 4b

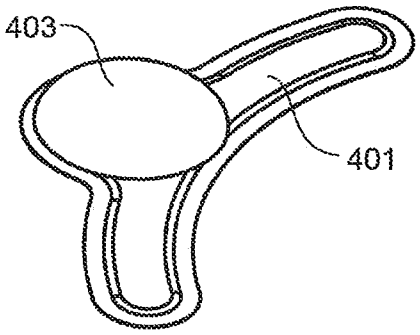


Fig 4c

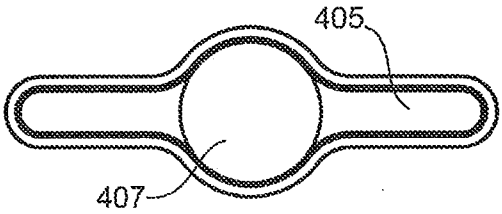


Fig 4d

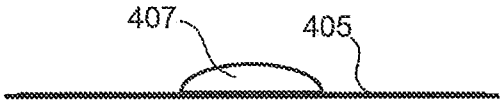


Fig 4e

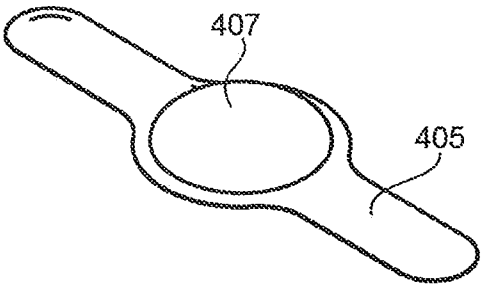


Fig 4f

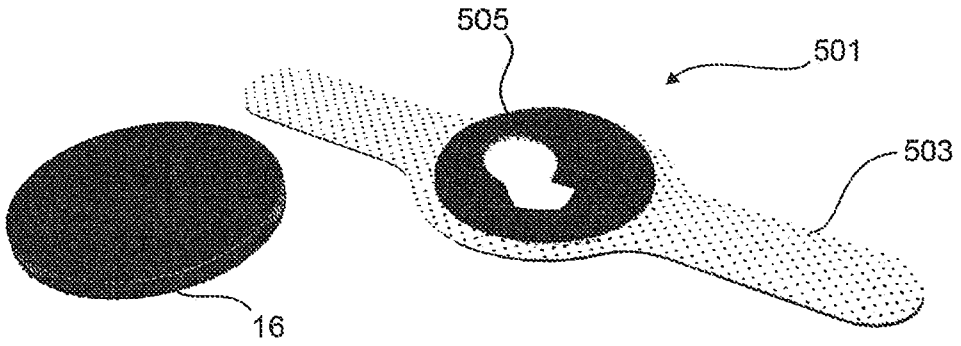

505
501
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Fig 5

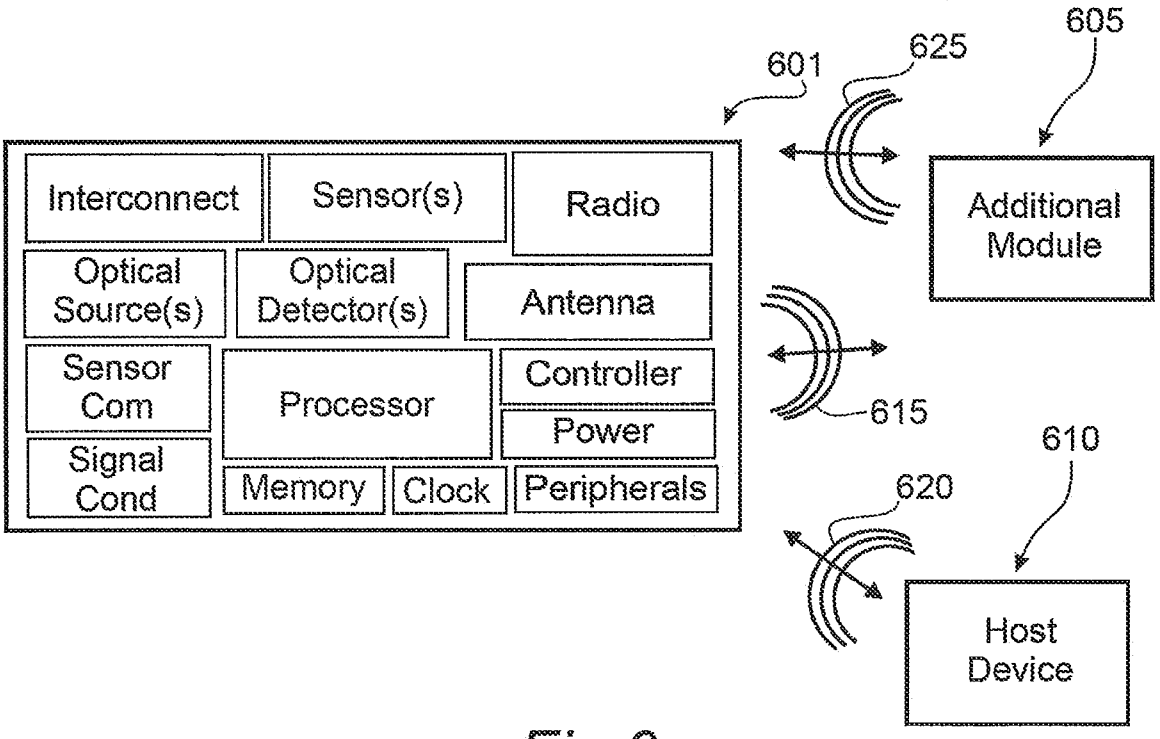

605
601
625
Interconnect
Sensor(s)
Radio
Additional Module
Optical Source(s)
Optical Detector(s)
Antenna
Sensor Com
Processor
Controller
Power
615
Signal Cond
Memory
Clock
Peripherals
610
620
Host Device

Fig 6

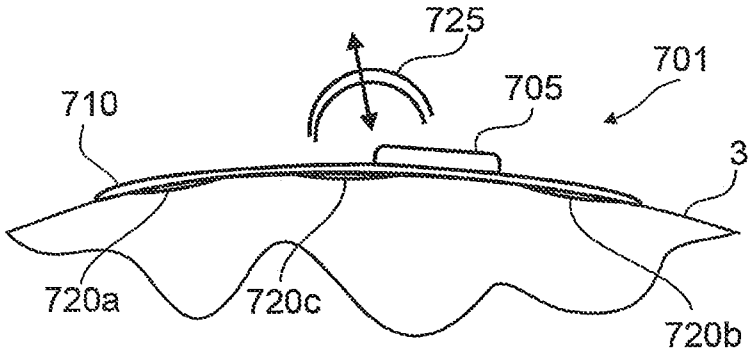


Fig 7

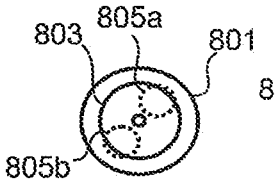


Fig 8a

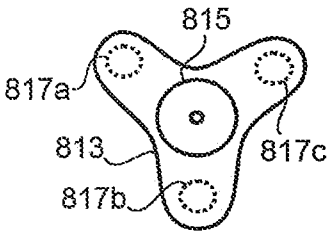


Fig 8c

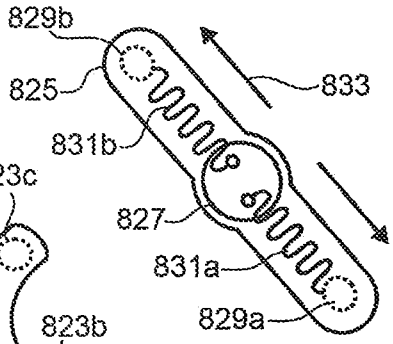


Fig 8e

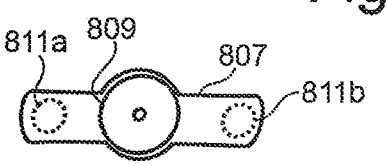


Fig 8b

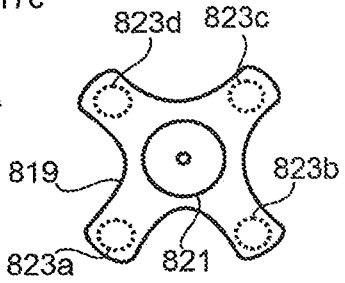


Fig 8d

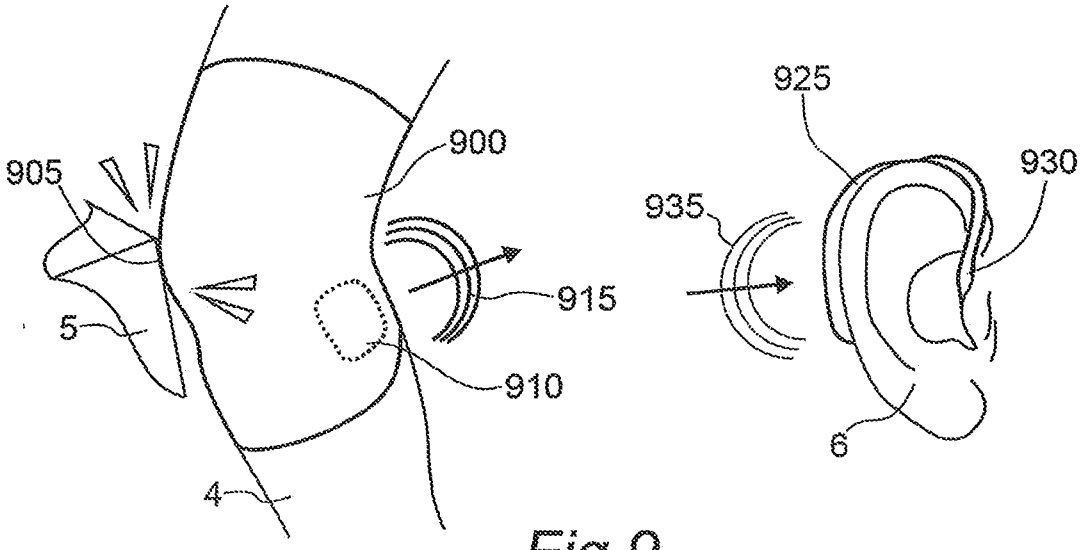


Fig 9

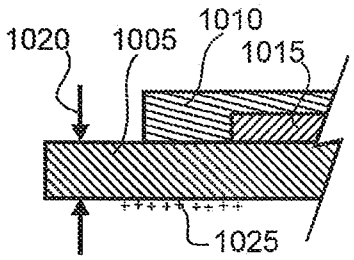


Fig 10a

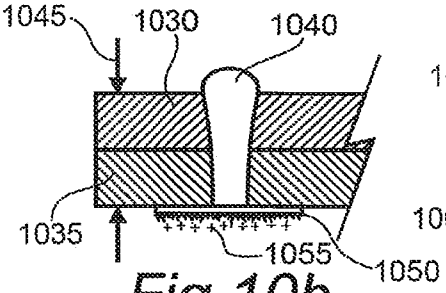


Fig 10b

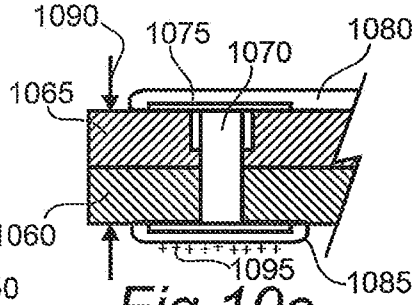


Fig 10c

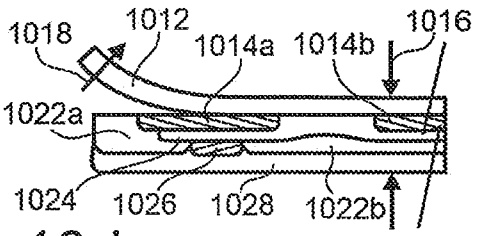


Fig 10d

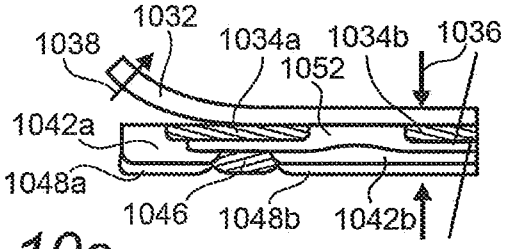


Fig 10e

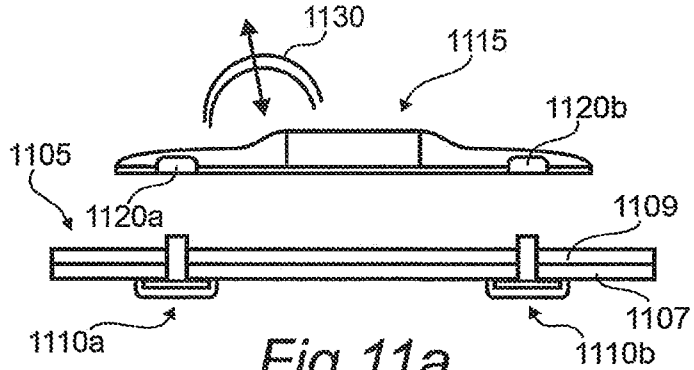


Fig 11a

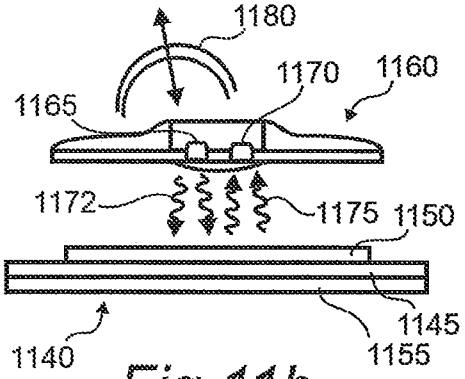


Fig 11b

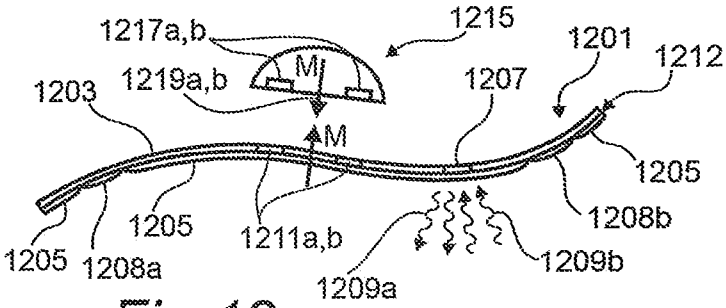


Fig 12a

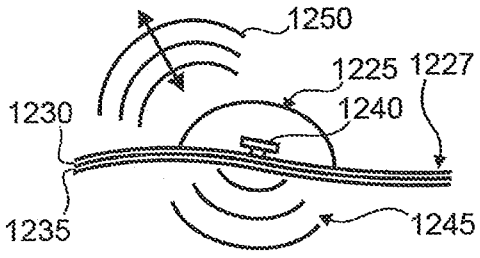


Fig 12b

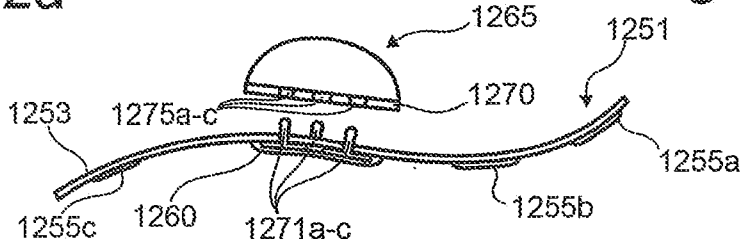


Fig 12c

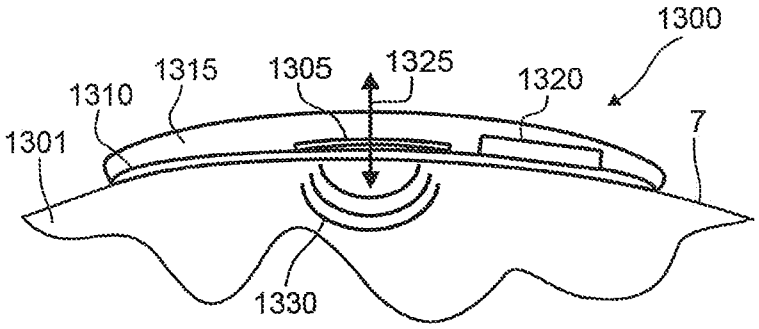


Fig 13

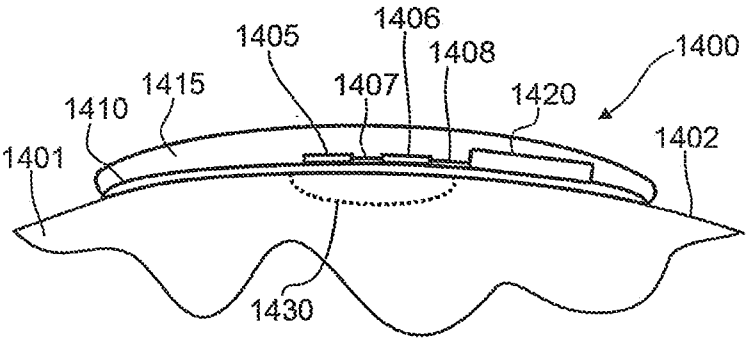


Fig 14

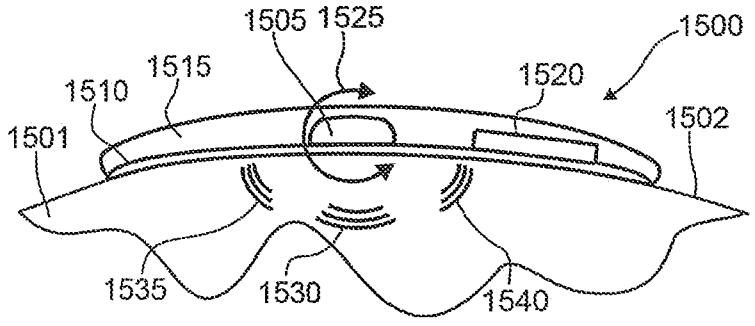


Fig 15

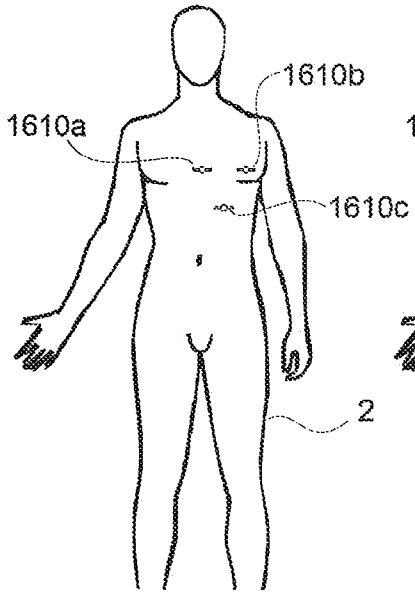


Fig 16a

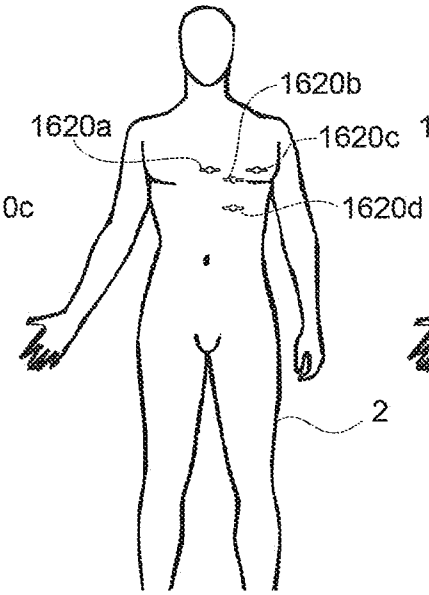


Fig 16b

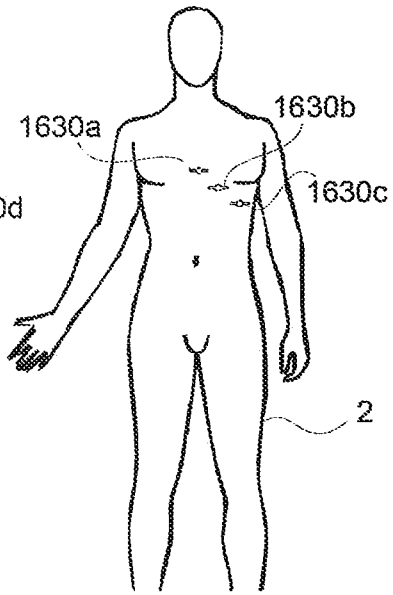


Fig 16c

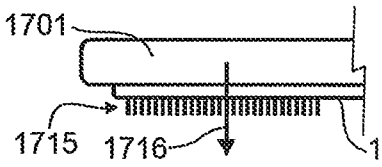


Fig 17a

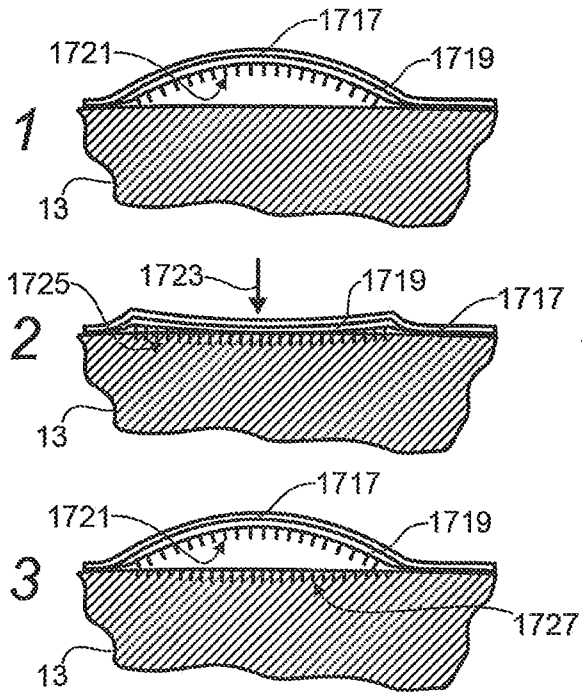


Fig 17b

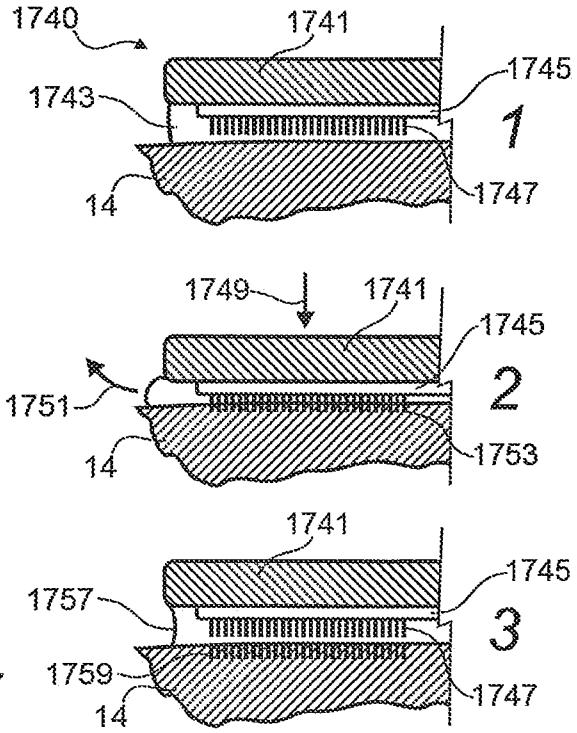


Fig 17c

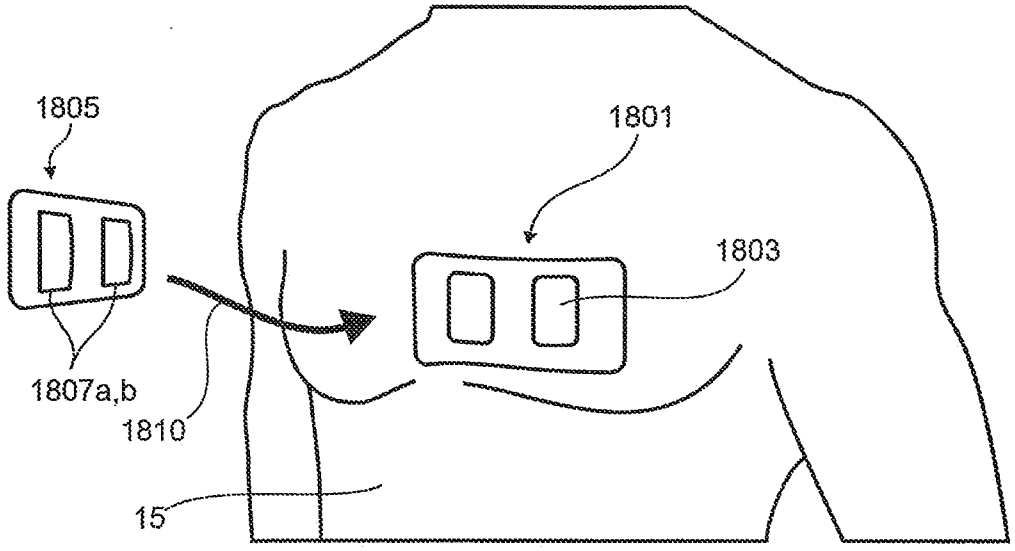

1805
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Fig 18

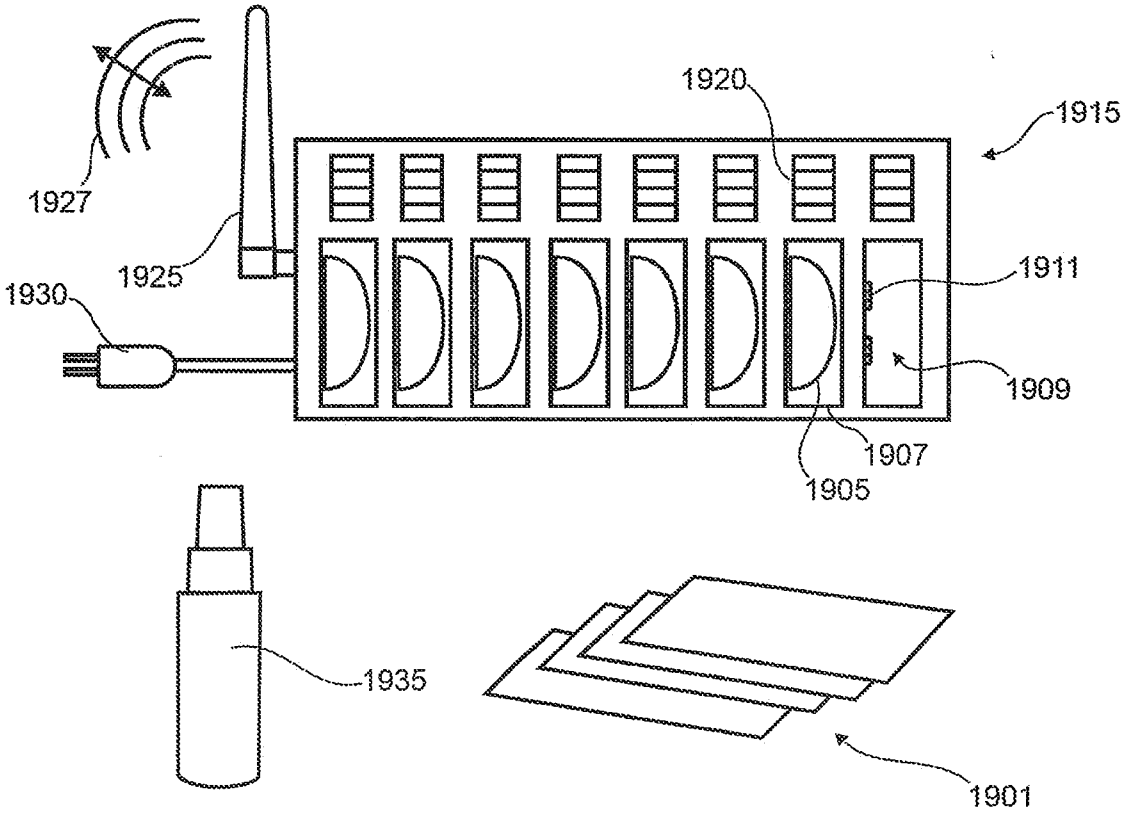

1920
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1901

Fig 19

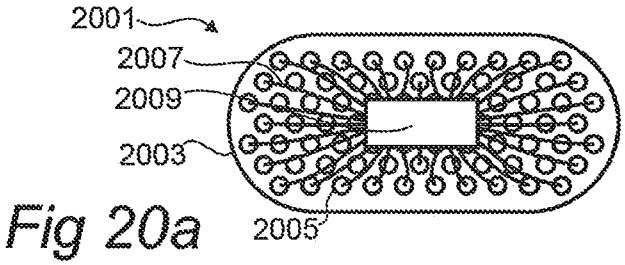


Fig 20a

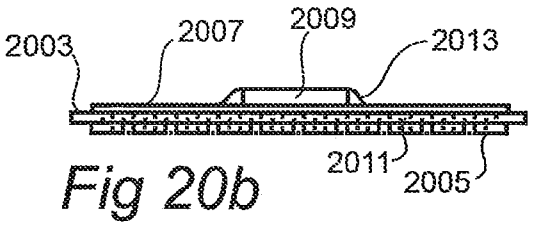


Fig 20b

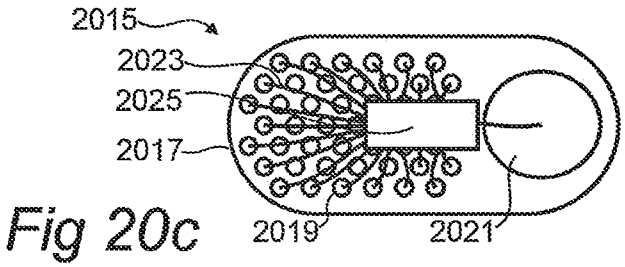


Fig 20c

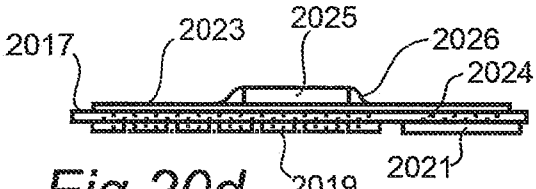


Fig 20d

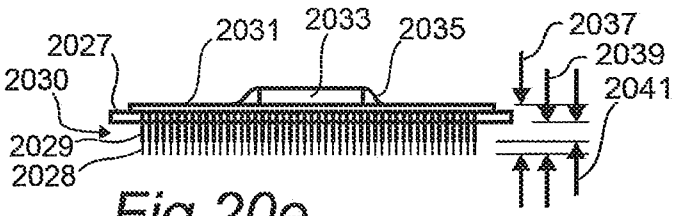


Fig 20e

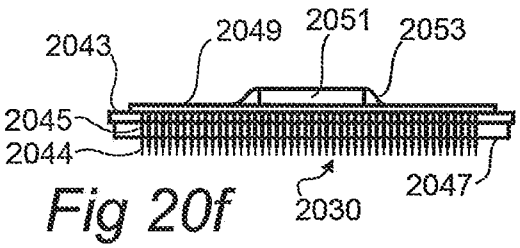


Fig 20f

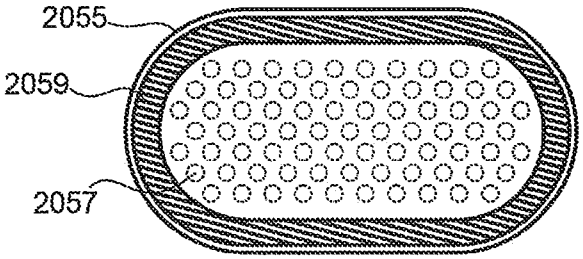


Fig 20g

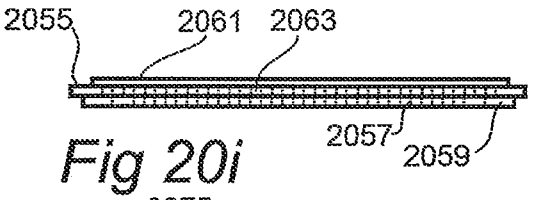


Fig 20i

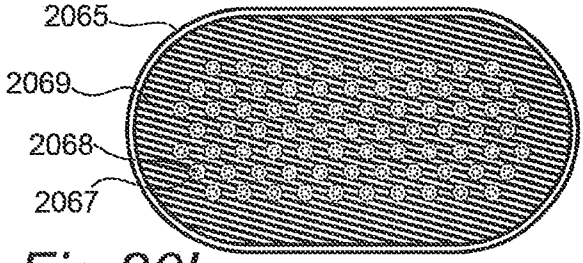


Fig 20h

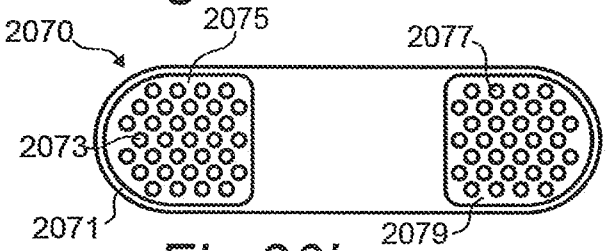


Fig 20j

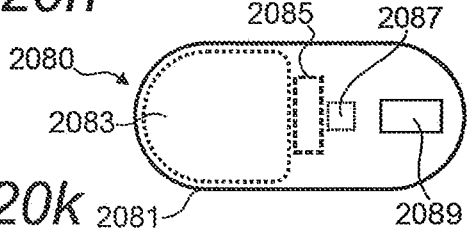


Fig 20k

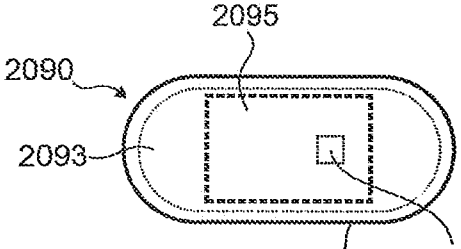


Fig 20l

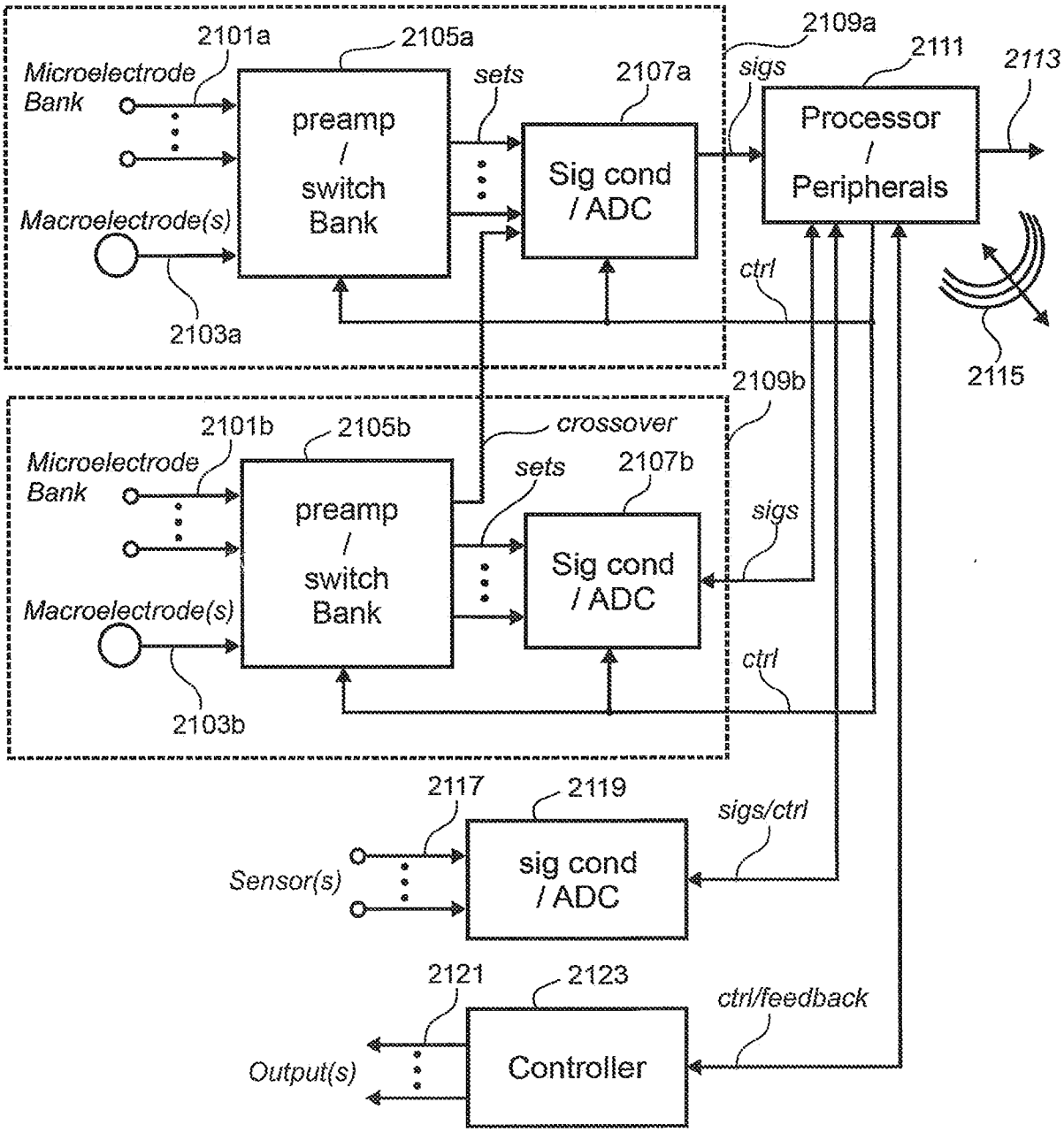

2101a
2105a
2109a
2111
2113
Microelectrode Bank
sets
2107a
sigs
preamp / switch Bank
Sig cond / ADC
Processor / Peripherals
Macroelectrode(s)
ctrl
2103a
2115
2109b
2101b
2105b
crossover
Microelectrode Bank
sets
2107b
sigs
preamp / switch Bank
Sig cond / ADC
Macroelectrode(s)
ctrl
2103b
2117
2119
sigs/ctrl
Sensor(s)
sig cond / ADC
2121
2123
ctrl/feedback
Output(s)
Controller

Fig 21

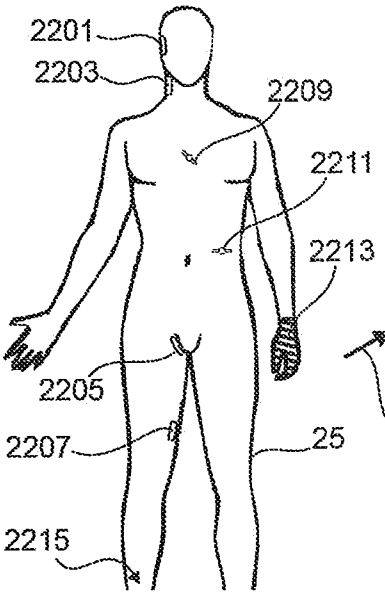


Fig 22a

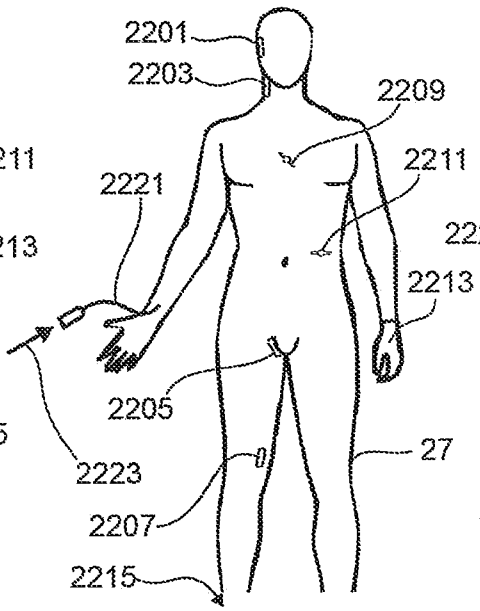


Fig 22b

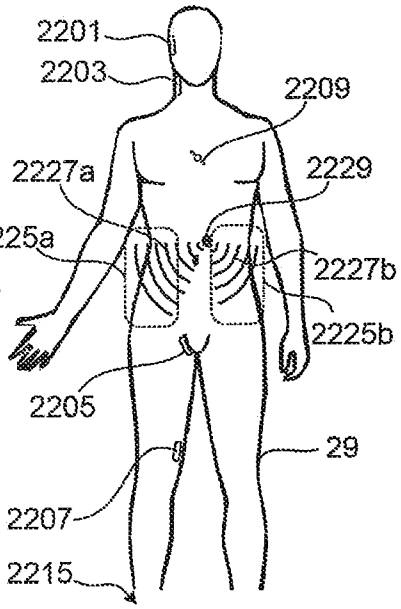


Fig 22c

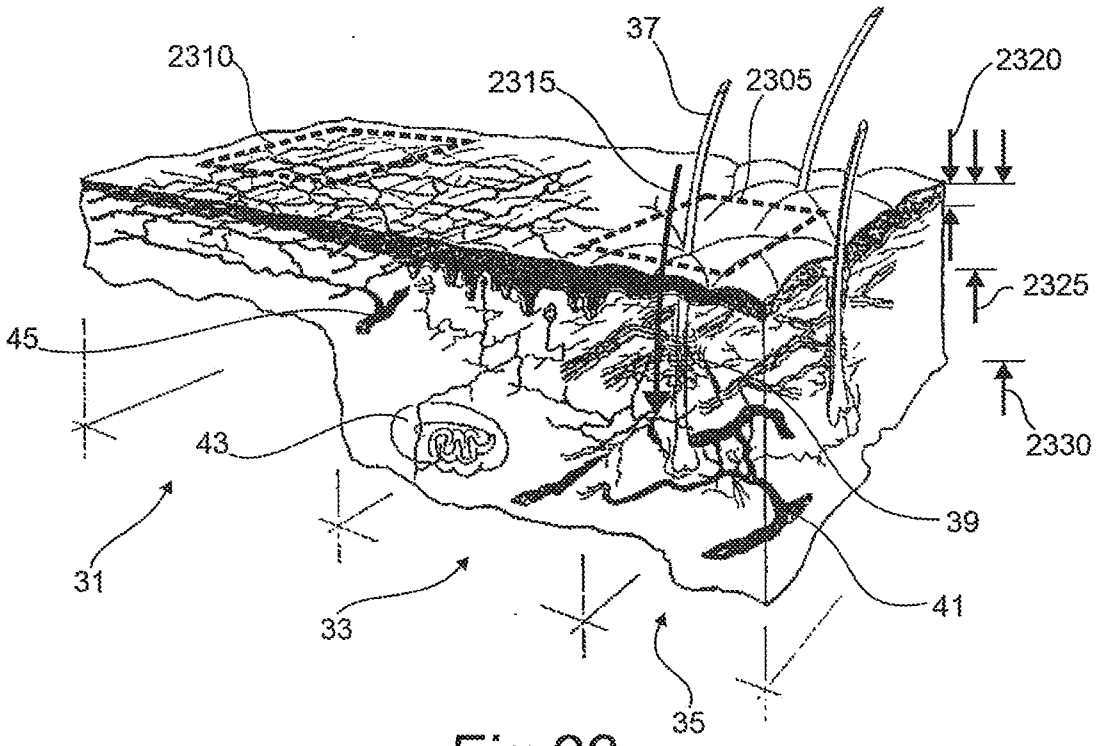


Fig 23

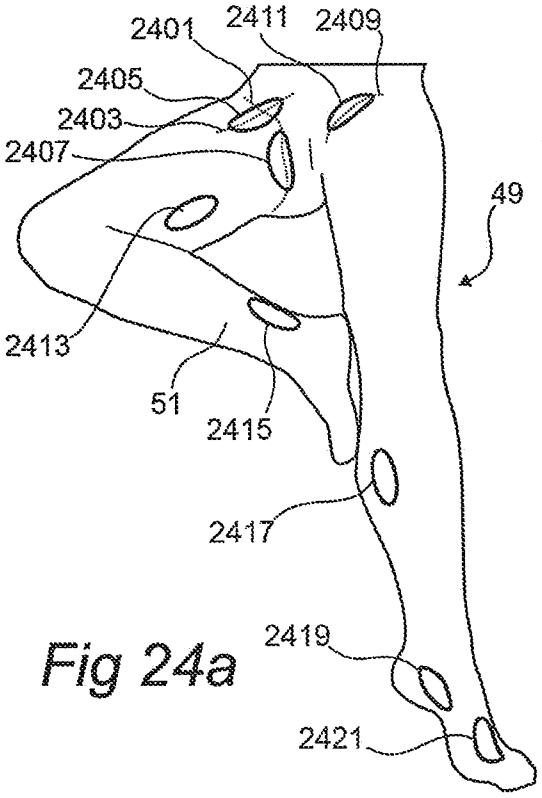


Fig 24a

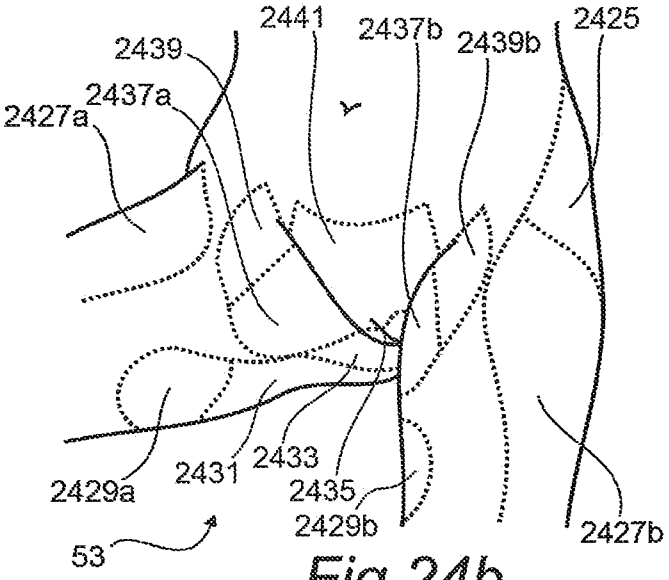


Fig 24b

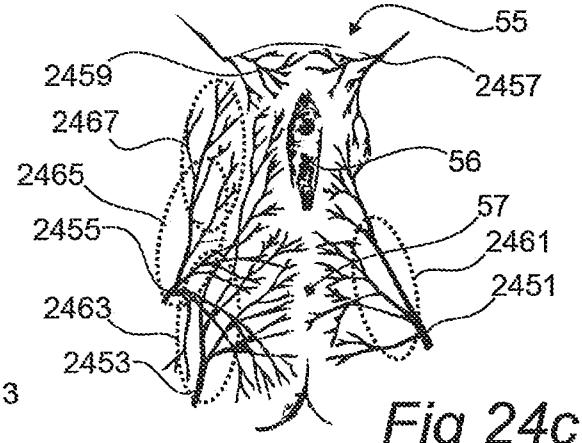


Fig 24c

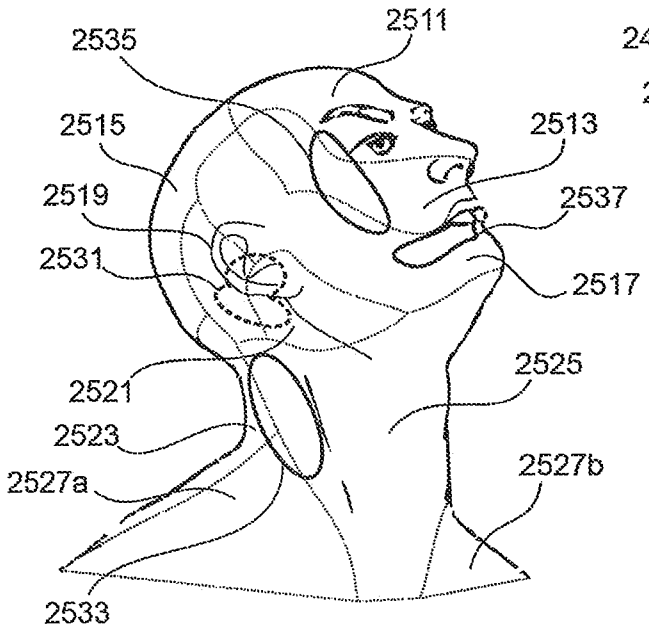


Fig 25a

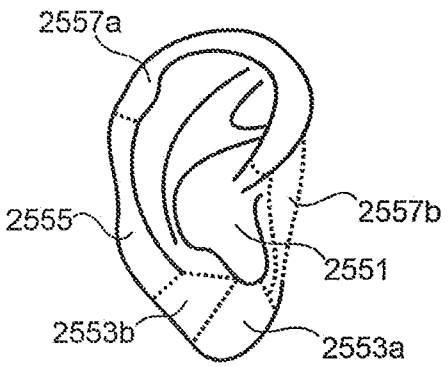


Fig 25b

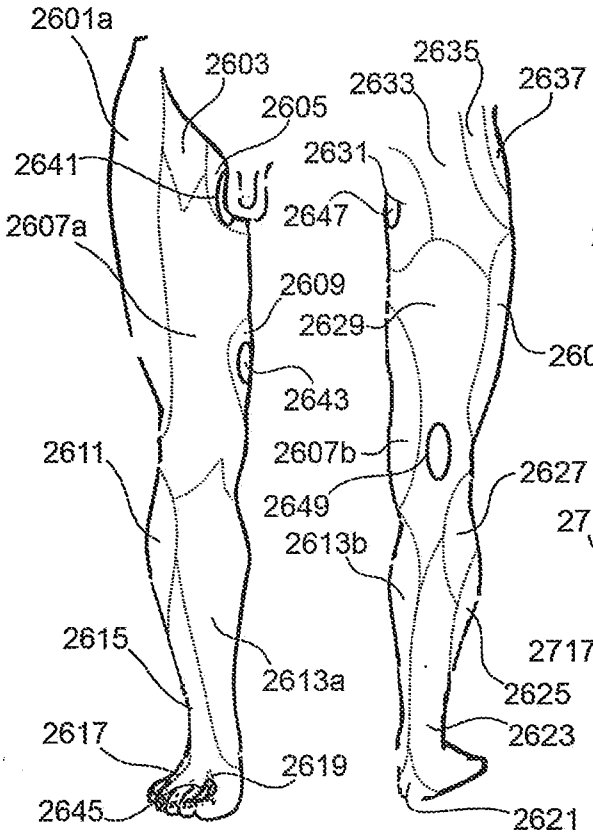


Fig 26a

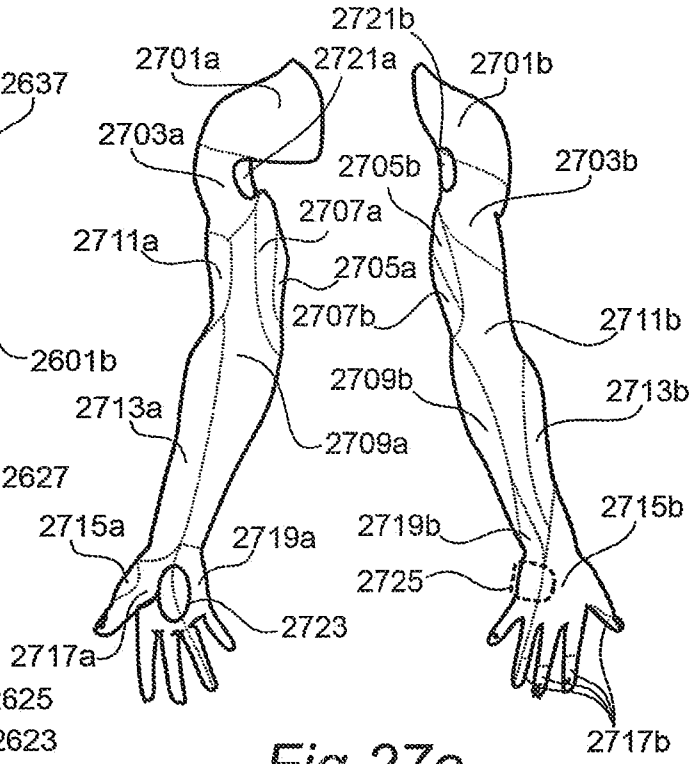


Fig 27a

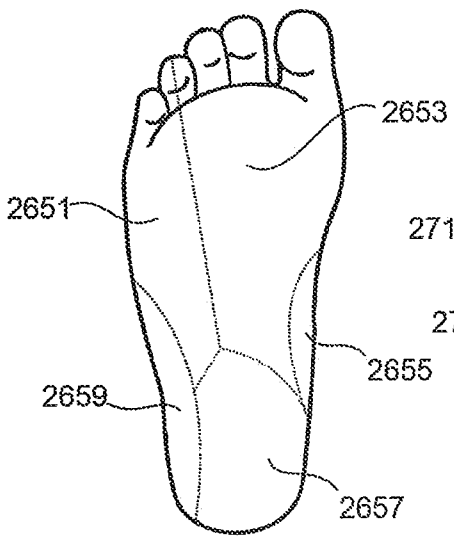


Fig 26b

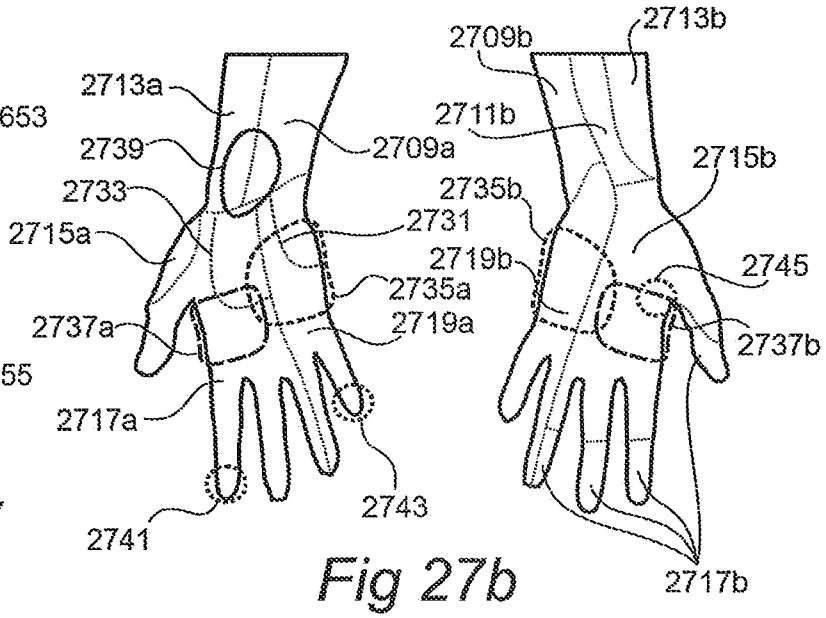


Fig 27b

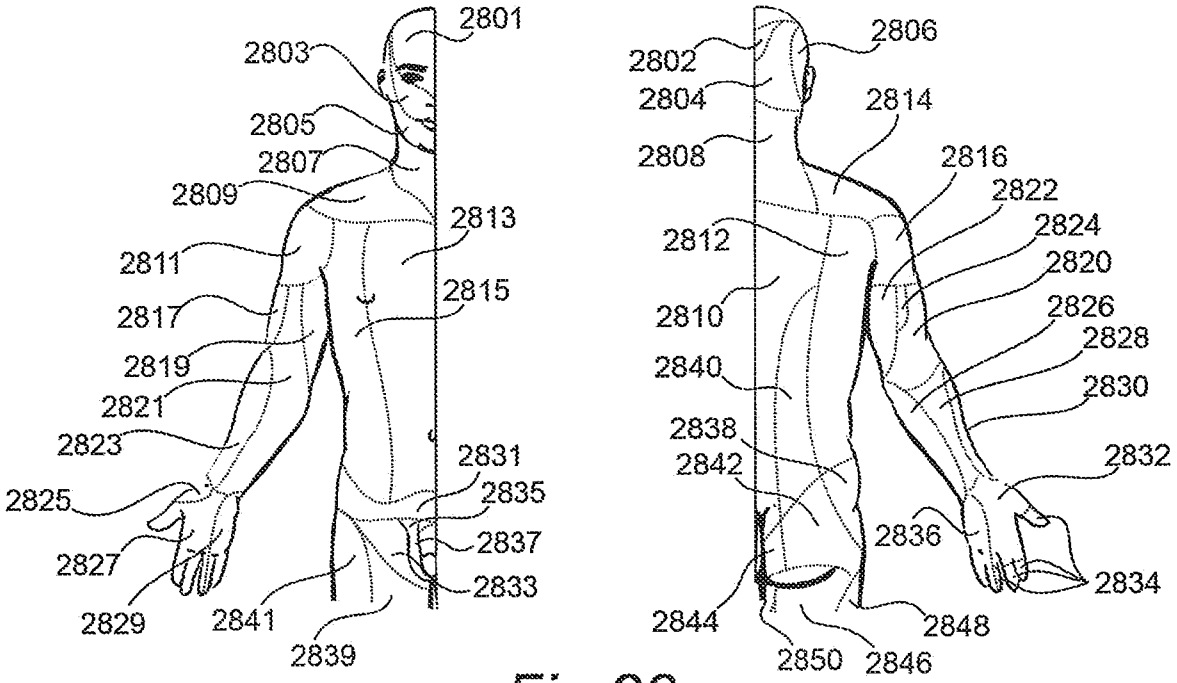


Fig 28a

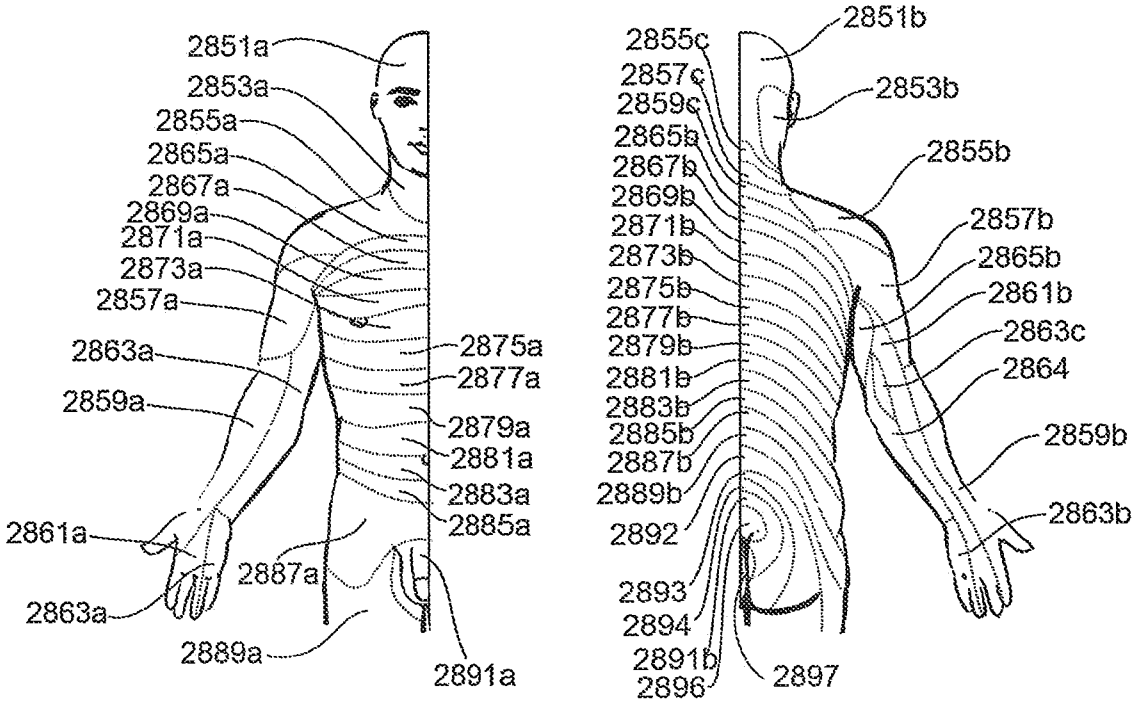


Fig 28b

Fig 29a

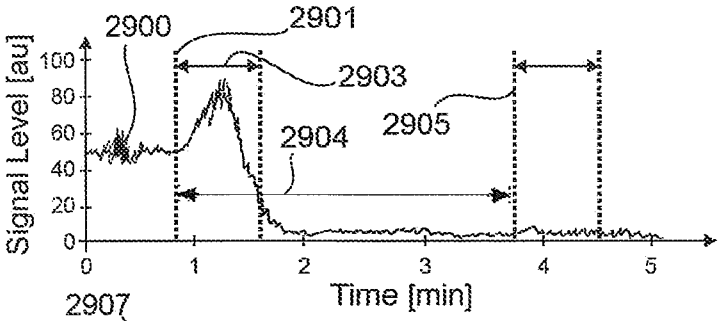


Fig 29b

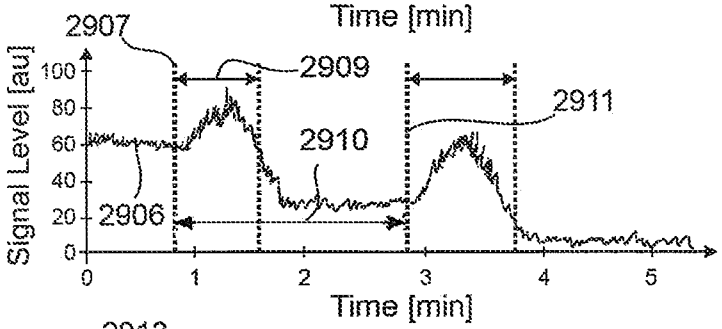


Fig 29c

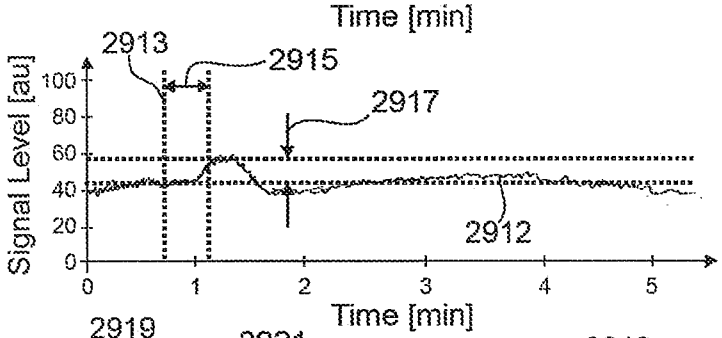


Fig 29d

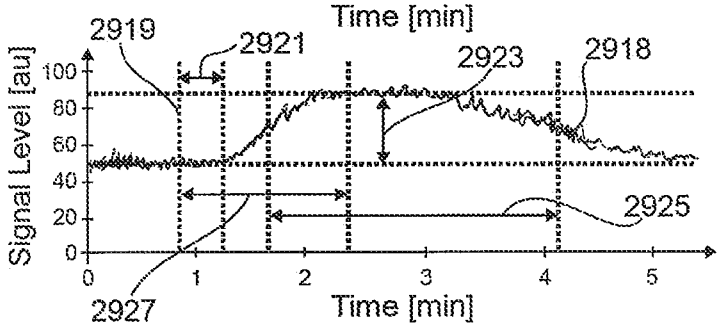
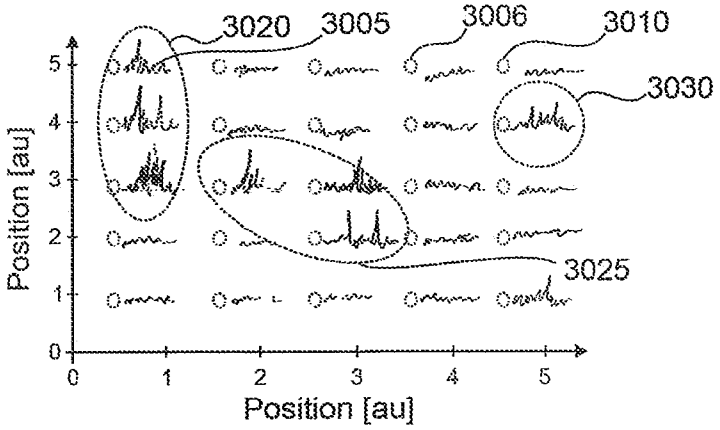


Fig 30



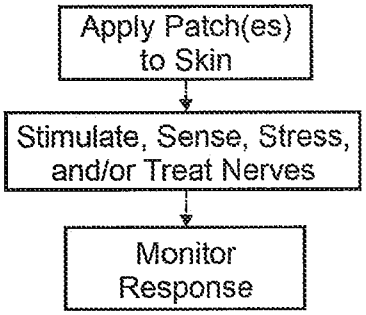


Fig 31a

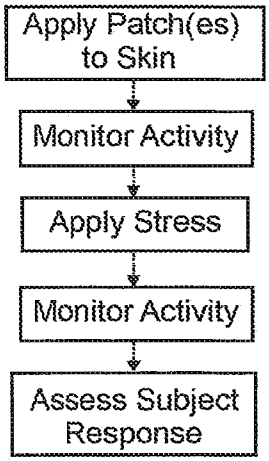


Fig 31b

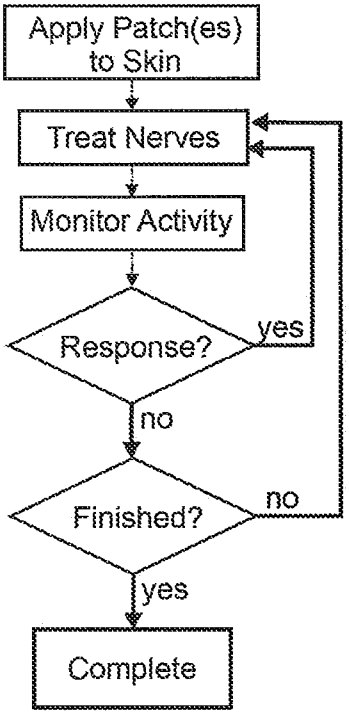


Fig 31c