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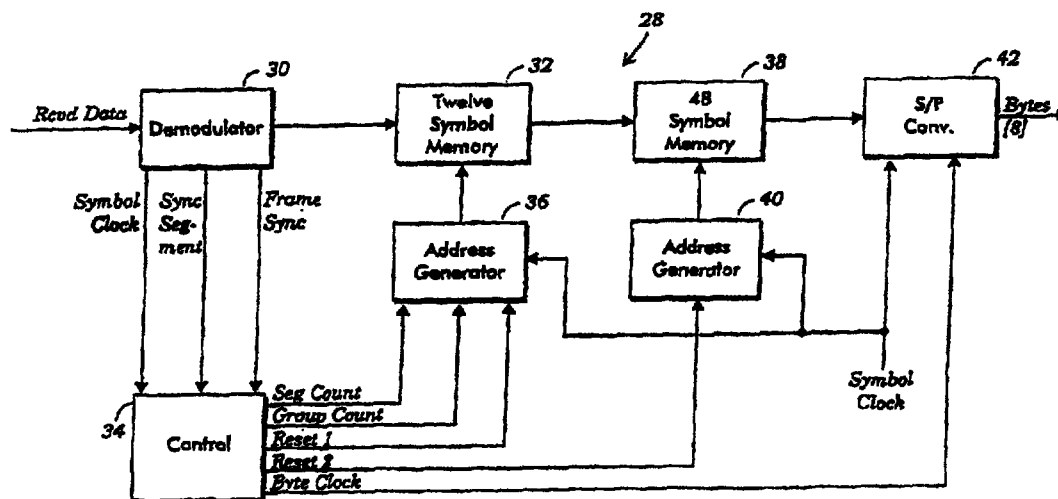
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(54) Title: DATA DE-ROTATOR AND DE-INTERLEAVER



(57) Abstract

An apparatus (28) for de-rotating and de-interleaving data includes (i) a first memory (32) for storing D elements of rotated and interleaved data in D storage locations, (ii) a first addresser (36) for addressing the first memory (32) in order to read de-rotated and interleaved data out of the D storage locations and to write rotated and interleaved data into the D storage locations, (iii) a second memory (38) for storing mD elements of the de-rotated and interleaved data read out of the first memory (32), wherein the de-rotated and interleaved data read out of the first memory (32) are stored in mD storage locations of the second memory (38), and (iv) a second addresser (40) for addressing the second memory (38) in order to read de-rotated and de-interleaved data out of the mD storage locations and to write de-rotated and interleaved data from the first memory (32) into the mD storage locations.