

ABSTRACT**A HIGH SPEED CMOS DUAL MODULUS PRESCALER USING PULL
DOWN TRANSISTOR**

The present invention provides a circuit and a method for high speed prescaler circuits which utilize pull-down transistors in the critical feedback path. This invention contains a high speed CMOS dual modulus prescaler circuit made up of data or D-flip flops connected serially where the flip-flop positive output Q of stage N is connected to the D-input of the N+1 flip-flop stage. It is also made up of a pull-down field effect transistor. The invention has a clock input which has a frequency known as a circuit input frequency, F_{in} . The output of this prescaler circuit has an output frequency, F_{out} . The frequency division which results from this prescaler circuit is a divide by $[2 \text{ to the power } (n+2)]$ minus 1 if a mode signal equals 1 as opposed to a divide by $[2 \text{ to the power } (n+2)]$ counter, which results when the mode signal is low.

(Figure 1)