WHAT IS CLAIMED:

1. A memory device comprising:

an output pin;

a mode register; and

a signal generator configured to generate a detection clock output signal including one of a random data pattern and a hold data pattern in response to a first control signal and a second control signal from the mode register, and output the detection clock output signal through the output pin,

wherein the random data pattern includes pseudo-random data generated by the memory device,

wherein the hold data pattern is a fixed pattern pre-stored in the memory device, and

wherein the detection clock output signal is used for a clock data recovery operation,

wherein the signal generator is configured to output the detection clock output signal through the output pin at one of a first rate and a second rate different from the first rate based on a third control signal output from the mode register.

2. The memory device of claim 1, wherein the detection clock output signal includes the random data pattern when the first control signal is a first logic level and the second control signal is a second other logic level, and the detection clock output signal includes the hold data pattern when the first control signal is the second logic level and the second control signal is the first logic level.

3. The memory device of claim 1, wherein the second rate is $1/2^N$ times the first rate, where N is a positive integer >= 1.

4. The memory device of claim 1 or claim 3, wherein the signal generator is further configured to generate an error detection code in response to a fourth control signal output from the mode register, and output the error detection code through the output pin at one of the first rate and the second rate based on the third control signal, wherein the detection clock output signal is output during a first time period and the error detection code is output during a second time period after the first time period.

5. The memory device of claim 4, wherein the signal generator is further configured to invert the detection clock output signal for output through the output pin in response to a fifth control signal output from the mode register.

6. The memory device of claim 5, wherein the signal generator is further configured to generate a command address signal for output through the output pin in response to a sixth control signal.

7. The memory device of claim 6, wherein the signal generator is further configured to generate a read data strobe in response to a seventh control signal output from the mode register, and output the read data strobe through the output pin, wherein the read data strobe is used by a device external to the memory device to latch read data output from the memory device.

8. The memory device of any one of claims 1 to 7, wherein the signal generator comprises:

a pseudo random bit sequence generator configured to generate a plurality of random bit signals in response to a first clock signal;

a logic circuit configured to receive the random bit signals and selectively perform an exclusive-OR operation on the random bit signals to generate a plurality of logic output signals;

a first pattern selector configured to receive one of the random bit signals and the logic output signals as first inputs and output some of the first inputs as a plurality of pattern signals in response to the first clock signal; and

a second pattern selector configured to receive the pattern signals as second inputs and output one of the second inputs to the output pin as the detection clock output signal in response to second clock signals,

wherein a clock cycle of the second clock signals is half a clock cycle of the first clock signal.

9. The memory device of any one of claims 3 to 7, wherein the signal generator comprises:

a pseudo random bit sequence generator configured to generate a plurality of random bit signals in response to a first clock signal;

a logic circuit configured to receive the random bit signals and generate a plurality of logic switching signals in response to the third control signal;

a first pattern selector configured to receive the logic switching signals as first inputs and output some of the first inputs as a plurality of pattern signals in response to the first clock signal; and

a second pattern selector configured to receive the pattern signals as second inputs and output one of the second inputs as the detection clock output signal in response to second clock signals,

wherein a clock cycle of the second clock signals is half a clock cycle of the first clock signal.

10. A memory system comprising:

the memory device of any one of claims 1 to 9; and

a controller configured to receive the detection clock output signal from the output pin and output a clock signal to the memory device, wherein the controller comprises a clock and data recovery (CDR) unit configured to perform the clock data recovery operation by adjusting the clock signal so that an edge of the clock signal is in a middle of the received detection clock output signal.

11. A memory device comprising:

an output pin;

a mode register; and

a signal generator configured to generate training data comprising a random data pattern in response to a first control signal output from the mode register during a first mode, and output the training data through the output pin at one of a first rate and a second rate different from the first rate based on a second control signal output from the mode register,

wherein the random data pattern includes pseudo-random data generated by the memory device, and

wherein the training data is used for a clock and data recovery operation.

12. The memory device of claim 11, wherein the second rate is $1/2^N$ times the first rate, where N is a positive integer >= 1.

13. The memory device of claim 11 or claim 12, wherein the signal generator is configured to generate the training data including a hold data pattern during a second mode in response to a third control signal from the mode register, where the hold data pattern is a fixed pattern pre-stored in the memory device.

14. The memory device of claim 12 or claim 13, wherein the signal generator is further configured to generate an error detection code in response to a third control signal output from the mode register, and output the error detection code through the output pin at one of the first rate and the second rate based on the second control signal, wherein the training data is output during a first time period and the error detection code is output during a second time period after the first time period.

15. The memory device of claim 14, wherein the signal generator is further configured to invert the training data for output through the output pin in response to a fourth control signal output from the mode register.

16. The memory device of claim 15, wherein the signal generator is further configured to generate a read data strobe in response to a fifth control signal output from the mode register, and output the read data strobe through the output pin, wherein the read data strobe is used by a device external to the memory device to latch read data output from the memory device.

17. The memory device of any one of claims 11 to 16, wherein the signal generator comprises:

a pseudo random bit sequence generator configured to generate a plurality of random bit signals in response to a first clock signal;

a logic circuit configured to receive the random bit signals and selectively perform an exclusive-OR operation on the random bit signals to generate a plurality of logic output signals;

a first pattern selector configured to receive one of the random bit signals and the logic output signals as first inputs and output some of the first inputs as a plurality of pattern signals in response to the first clock signal; and

a second pattern selector configured to receive the pattern signals as second inputs and output one of the second inputs to the output pin as the training data in response to second clock signals,

wherein a clock cycle of the second clock signals is half a clock cycle of the first clock signal.

18. The memory device of any one of claims 11 to 16, wherein the signal generator comprises:

a pseudo random bit sequence generator configured to generate a plurality of random bit signals in response to a first clock signal;

a logic circuit configured to receive the random bit signals and generate a plurality of logic switching signals in response to the second control signal;

a first pattern selector configured to receive the logic switching signals as first inputs and output some of the first inputs as a plurality of pattern signals in response to the first clock signal; and

a second pattern selector configured to receive the pattern signals as second inputs and output one of the second inputs as the training data in response to second clock signals,

wherein a clock cycle of the second clock signals is half a clock cycle of the first clock signal.

19. A memory system comprising:

the memory device of any one of claims 11 to 18; and

a controller configured to receive the training data from the output pin and output a clock signal to the memory device, wherein the controller comprises a clock and data recovery (CDR) unit configured to perform the clock data recovery operation by adjusting the clock signal so that an edge of the clock signal is in a middle of the received training data.