device shown in FIG. 77.

[FIG. 79] FIG. 79 is a flowchart showing a process example of the channeling ion implantation device.

[FIG. 80] FIG. 80 is a schematic view for illustrating an ion implantation step.

[FIG. 81] FIG. 81 is a schematic view for illustrating an ion implantation step.

[0008] [Detailed Description]

Hereinafter, specific embodiments will be described in detail with reference to the accompanying drawings. All of the accompanying drawings are schematic views and thus are not precisely drawn and are not always matched in relative positional relationships, reduced scales, ratios, angles, etc. Identical reference signs are assigned to corresponding structures in the accompanying drawings, and redundant descriptions thereof will be omitted or simplified. Descriptions provided before the omission or simplification will be applied to the structures described in an omitted or simplified manner.

[0009] When the wording "substantially" is used in this Description, the wording includes a numerical value (shape) equal to a numerical value (shape) of the comparison target and also includes numerical errors (shape errors) in a range of ±10% on a basis of the numerical value (shape) of the comparison target. Although the wordings "first," "second," "third," etc., are used in the following description, these are symbols attached to names of respective structures in order to clarify the order of description and are not attached with an intention of restricting the names of the respective structures.

[0010] In the following descriptions, a "p-type" or an "n-type" is used to indicate a conductivity type of a semiconductor (impurities), however, the "p-type" may be referred to as a "first conductivity type," and the "n-type" may be referred to as a "second conductivity type." As a matter of course, the "n-type" may be referred to as a "first conductivity type," and the "p-type" may be referred to as a "second conductivity type." The "p-type" is a conductivity type due to a trivalent element, and the "n-type" is a conductivity type due to a pentavalent element. The trivalent element may be at least one type among boron, aluminum, gallium, and indium, unless otherwise specified. The pentavalent element is at least one type among nitrogen, phosphorus, arsenic, antimony, and bismuth, unless otherwise specified.

[0011] FIG. 1 is a plan view showing an SiC semiconductor device 1A according to a first embodiment. FIG. 2A is a cross-sectional view taken along line IIA-IIA in FIG. 1. FIG. 2B is a cross-sectional view taken along line IIB-IIB in FIG. 1. FIG. 3A is a plan view showing a layout example of a chip 2 (a first layer 8). FIG. 3B is a plan view showing a layout example of the chip 2 (a second layer 9). FIG. 4A is a perspective view showing the chip 2 together with an

of second marks Mk2, the plurality of second spaces Sp2.

[0095] The second difference mark Md2 has electrical characteristics (impurities = a trivalent element) different from the electrical characteristics (impurities = a pentavalent element) of the plurality of second spaces Sp2. Therefore, the plurality of second difference marks Md2 and the plurality of second spaces Sp2 are identified by measuring the electrical characteristics (impurities, concentrations, resistance values, etc.) of the second difference mark Md2 and the plurality of second spaces Sp2. For example, the second difference mark Md2 and the plurality of second spaces Sp2 can be identified using an electron microscope such as an SEM or a TEM, etc., and/or EBIC analysis, etc.

[0096] The second difference mark Md2 has a lower end portion on the lower end side of the first layer 8 and an upper end portion on the upper end side of the first layer 8. The lower end portion of the second difference mark Md2 is positioned in a region on the lower end side of the first layer 8 with respect to the thickness range intermediate portion of the first layer 8, and the upper end portion of the second difference mark Md2 is positioned in a region on the upper end side of the first layer 8 with respect to the thickness range intermediate portion of the first layer 8. That is, the second difference mark Md2 is constituted of a single impurity region having a thickness (a depth) that crosses the intermediate portion of the first layer 8 along the first axis channel CH1.

[0097] The lower end portion of the second difference mark Md2 may be formed at an interval from the lower end (that is, the base layer 6) of the first layer 8 to the upper end (the second layer 9) side of the first layer 8 and may oppose the base layer 6 across a part (the lower end portion) of the first layer 8. The lower end portion of the second difference mark Md2 may be substantially matched with the lower end of the first layer 8 and may be connected to the base layer 6. The lower end portion of the second difference mark Md2 may have an extension portion that crosses the boundary portion between the base layer 6 and the first layer 8 and is positioned in the base layer 6.

[0098] The upper end portion of the second difference mark Md2 may be formed at an interval from the upper end (that is, the second layer 9) to the lower end side of the first layer 8 and may oppose the plurality of second marks Mk2 across a part (the upper end portion) of the first layer 8. The upper end portion of the second difference mark Md2 may be exposed from the upper end (that is, the second layer 9) of the first layer 8.

[0099] In this case, the upper end portion of the second difference mark Md2 may be connected to the lower end portions of the plurality of second marks Mk2. As a matter of course, the upper end portion of the second difference mark Md2 may be formed at an interval from the lower end portions of the plurality of second marks Mk2 to the lower end side of the first layer 8 and may

pattern PT according to the fifth configuration example. In this case, the first difference mark Md1 described above is formed in the upper range of the second side surface 5B. Also, the second difference mark Md2 described above is formed in the lower range of the first side surface 5A.

[0105] With reference to FIGS. 2 to 7, the SiC semiconductor device 1A includes the column region 12 of the p-type formed at least in the laminated portion 7 in the active region 10. The column region 12 may be referred to as a "column layer," a "pillar layer (region)," a "p-type layer (region)," a "p-type zone," etc. The column region 12 is formed in a three-dimensional lattice shape in the laminated portion 7 and defines three-dimensional lattice-shaped drift region 13 of the n-type which is constituted of a part of the laminated portion 7.

[0106] The column region 12 is formed in at least one semiconductor layer among the plurality of semiconductor layers constituting the laminated portion 7 and form a super junction structure SJ with the drift region 13 in the laminated portion 7. In this embodiment, the column region 12 has a laminated structure including a plurality of first regions 14 of the p-type and a plurality of second regions 15 of the p-type.

[0107] The plurality of first regions 14 are formed at intervals in the horizontal direction in the first layer 8 and define a plurality of first drift regions 16 of the n-type that are each constituted of a part of the first layer 8. The plurality of first regions 14 form a plurality of first pn-junction portions having charge balance together with the plurality of first drift regions 16.

[0108] That is, the plurality of first regions 14 constitute a first super junction structure SJ1 with the plurality of first drift regions 16. The state of having the charge balance means a state in which, regarding the plurality of first regions 14 adjacent to each other, a depletion layer expanding from one first pn-junction portion and a depletion layer expanding from the other first pn-junction portion are connected in the plurality of first drift regions 16.

[0109] The plurality of first regions 14 are arrayed at intervals in a first array direction Da1 in the first layer 8 and are each formed as a band extending in a first extension direction De1. The first extension direction De1 is a direction intersecting or orthogonal to the first array direction Da1. That is, the plurality of first regions 14 are formed as stripes extending in the first extension direction De1, and the plurality of first drift regions 16 are formed as stripes extending in the first extension direction De1.

[0110] In this embodiment, the plurality of first regions 14 are led out from the active region 10 to the outer peripheral region 11 (see FIG. 3A). That is, the plurality of first regions 14 are led out from a portion of the first layer 8 positioned in the active region 10 to a portion of the first layer 8 positioned in the outer peripheral region 11. The plurality of first regions 14 are arrayed

value) of the second region 15 may be less than the p-type impurity concentration (the peak value) of the first region 14. The p-type impurity concentration (the peak value) of the second region 15 may be substantially equal to the p-type impurity concentration (the peak value) of the first region 14.

[0148] The p-type impurity concentration of the second region 15 is preferably adjusted by at least one type of trivalent element. The p-type impurity concentration of the second region 15 is particularly preferably adjusted by a trivalent element belonging to heavy elements heavier than carbon. That is, the second region 15 preferably includes a trivalent element other than boron (at least one type among aluminum, gallium, and indium). In this embodiment, the p-type impurity concentration of the second region 15 is adjusted by aluminum.

[0149] Each of the plurality of second regions 15 has a second width W2. The second width W2 is a width along the second array direction Da2 of the second regions 15. The second width W2 is preferably less than the second thickness T2 of the second layer 9. As a matter of course, the second width W2 may be not less than the second thickness T2.

[0150] The second width W2 is preferably less than the first thickness T1 of the first layer 8. As a matter of course, the second width W2 may be not less than the first thickness T1. The second width W2 is preferably substantially equal to the first width W1 of the first region 14. As a matter of course, the second width W2 may be not less than the first width W1 or may be less than the first width W1.

[0151] The second width W2 may be not less than 0.1 μm and not more than 5 μm. The second width W2 may have a value falling within any one of ranges of not less than 0.1 μm and not more than 0.25 μm, not less than 0.25 μm and not more than 0.5 μm, not less than 0.5 μm and not more than 0.75 μm, not less than 0.75 μm and not more than 1 μm, not less than 1 μm and not more than 1.5 μm, not less than 1.5 μm and not more than 2 μm, not less than 2 μm and not more than 2.5 μm, not less than 2.5 μm and not more than 3 μm, not less than 3 μm and not more than 3.5 μm, not less than 3.5 μm and not more than 4 μm, not less than 4 μm and not more than 4.5 μm, and not less than 4.5 μm and not more than 5 μm. The second width W2 is preferably not less than 0.5 μm and not more than 1.5 μm.

[0152] Each of the plurality of second regions 15 has a second region thickness TR2 (a second region depth). The second region thickness TR2 may be less than the second thickness T2 of the second layer 9. The second region thickness TR2 may be larger than the second thickness T2. The second region thickness TR2 may be substantially equal to the second thickness T2.

[0153] The second region thickness TR2 may be less than the first thickness T1 of the first layer 8. The second region thickness TR2 may be larger than the first thickness T1. The second

energies in five stages (190 KeV, 380 KeV, 650 KeV and 960 KeV). In the case of this step, the trivalent elements can be introduced into a target depth position, but the depth position to which the trivalent element can be introduced is shallow. Hence, the number of steps of epitaxial growth and the number of steps of the random implantation method need to be increased, and a problem similar to that in the multi-epitaxial growth method arises.

[0223] On the other hand, in the case of the channeling implantation method, the second region 15 including the gentle gradient portion 22 having a thickness of not less than 0.5 μm and not more than 2 μm is formed with respect to the second layer 9 having a relatively large thickness (for example, a thickness of not less than 1 μm and not more than 5 μm). Therefore, the second region 15 having the charge balance is formed with fewer man-hours than the man-hours in the case of employing the random implantation method.

[0224] As a matter of course, this Description does not exclude a technical idea of forming the single second region 15 by introducing the plurality of second regions 15 into different depth positions in multiple stages by the channeling implantation method using a plurality of implantation energies. In this case, each of the second regions 15 is constituted of an integrated region of a plurality of impurity regions (the second regions 15) which are respectively formed in the second layer 9 along the second axis channel CH2 such as to cross the intermediate portion of the second layer 9.

[0225] In this case, the p-type impurity concentration (the concentration gradient) of each of the second regions 15 is an added value of p-type impurity concentrations (concentration gradients) of the plurality of impurity regions (the second regions 15). For example, the p-type impurity concentrations of the respective second regions 15 have a concentration gradient (added concentration gradient) obtained by superimposing at least two of the five graphs shown in FIGS. 13A to 13E.

[0226] In the examples in FIGS. 13A to 13E, an upper limit of the implantation energy of the channeling implantation method is 2000 KeV, but the second region 15 can also be formed with an implantation energy higher than 2000 KeV. In this case, the relatively thick second region 15 is formed at a position deeper than the concentration gradient shown in FIG. 13E.

[0227] However, in a case where the implantation energy higher than 2000 KeV is realized, a design difficulty of the column region 12 increases since the amount of the trivalent elements passing the upper end portion of the second layer 9 increases and a range of an empty region on this upper end portion side (that is, a distance between the first main surface 3 and the second region 15) increases. Also, in the case where the implantation energy higher than 2000 KeV is realized, it is assumed that the implantation energy is not realistic from the viewpoint of cost

portion 15a of the second region 15 may have an extension portion that crosses the boundary portion between the first layer 8 and the second layer 9 and is positioned in the first layer 8.

[0241] Since the second axis channel CH2 is substantially matched with the first axis channel CH1, the extension portion of the second lower end portion 15a is formed along the first axis channel CH1 in the first layer 8. The extension portion of the second lower end portion 15a is preferably positioned on the upper end side of the first layer 8 with respect to the thickness range intermediate portion of the first layer 8. The extension portion of the second lower end portion 15a is connected to the first region 14 (the first upper end portion 14b) in the first layer 8.

[0242] In this configuration, a part (the extension portion) of the second region 15 is provided in a space between the upper end of the first layer 8 and the first upper end portion 14b of the first region 14, and one column region 12 continuously extending in a three-dimensional lattice shape is formed by the first region 14 and the second region 15. Therefore, the accuracy of the charge balance is improved.

[0243] In this example, the second region 15 has the second region thickness TR2 larger than the second thickness T2 of the second layer 9. Also, the second region thickness TR2 may be larger than the first thickness T1 of the first layer 8. Also, the second region thickness TR2 may be larger than the first region thickness TR1 of the first region 14. As a matter of course, the second region thickness TR2 may be less than the second thickness T2. Also, the second region thickness TR2 may be less than the first region thickness TR1. Also, the second region thickness TR2 may be less than the first region thickness TR1.

[0244] The second gradual increase portion 20B, the second peak portion 21B, the second gentle gradient portion 22B, and the second gradual decrease portion 23B of the second region 15 are positioned in the second layer 9. At least a part of the second gradual decrease portion 23B is positioned in the first layer 8. That is, the extension portion of the second lower end portion 15a includes the second gradual decrease portion 23B. As a matter of course, a part of the second gentle gradient portion 22B may be positioned in the first layer 8 (see FIG. 13E). That is, the extension portion of the second lower end portion 15a may include a part of the second gentle gradient portion 22B and the second gradual decrease portion 23B.

[0245] FIG. 18 shows an example in which the second layer 9 has the first thickness T1 of 3 μm, and the second region 15 is formed in the second layer 9 with the implantation energy of 960 KeV. As a matter of course, the second region 15 may be formed with the implantation energy of not less than 960 KeV. For example, the second thickness T2 may be more than 3 μm and be not more than 5 μm. In this case, the second regions 15 connected to the first regions 14 in the first layer 8 are formed with the implantation energy of not less than 960 KeV (see also FIGS. 13A to

decrease portion 23A. As a matter of course, a part of the first gentle gradient portion 22A may be positioned in the base layer 6 (see FIG. 13E). That is, the extension portion of the first lower end portion 14a may include a part of the first gentle gradient portion 22A and the first gradual decrease portion 23A.

[0257] FIG. 22 shows an example in which the first layer 8 has the first thickness T1 of 3 μm, and the first region 14 is formed in the first layer 8 with the implantation energy of 960 KeV. As a matter of course, the first region 14 may be formed with the implantation energy of not less than 960 KeV. For example, the first thickness T1 may be more than 3 μm and be not more than 5 μm. In this case, the first regions 14 that are partially positioned in the base layer 6 are formed with the implantation energy of not less than 960 KeV (see also FIGS. 13A to 13E).

[0258] FIG. 23 is a cross-sectional perspective view showing the column region 12 according to the fifth configuration example. FIG. 24 is a graph showing an example of a concentration gradient of the column region 12 shown in FIG. 23. With reference to FIGS. 23 and 24, the column region 12 according to the fifth configuration example has a form obtained by modifying the first region 14 according to the fourth configuration example. The second region 15 according to the fifth configuration example has a form identical to the form of the second region 15 according to the second configuration example. As a matter of course, the second region 15 according to the fifth configuration example has a form identical to the form of the second region 15 according to the third configuration example.

[0259] In the fourth configuration example, the first layer 8 has the first thickness T1 of 3 μm, and the first region 14 is formed in the first layer 8 with the implantation energy of not less than 960 KeV. On the other hand, in the fifth configuration example, the first layer 8 has the first thickness T1 of less than 3 μm, and the first region 14 is formed in the first layer 8 with the implantation energy of not less than 650 KeV. In this example, the first region 14 has the first region thickness TR1 larger than the first thickness T1. In this example, the first thickness T1 is less than the second thickness T2 of the second layer 9.

[0260] For example, the first thickness T1 may be not less than 1 μm and not more than 2 μm. In this case, the first region 14 that is partially positioned in the base layer 6 is formed with the implantation energy of not less than 190 KeV (see also FIGS. 13A to 13E). For example, the first thickness T1 may be not less than 2 μm and less than 3 μm. In this case, the first region 14 that is partially positioned in the base layer 6 is formed with the implantation energy of not less than 380 KeV (see also FIGS. 13B to 13E).

[0261] FIG. 25 is a cross-sectional perspective view showing the column region 12 according to the sixth configuration example. FIG. 26 is a graph showing an example of a concentration

regions 15. On the other hand, the plurality of gate structures 35 according to the second configuration example extend in a direction other than the second extension direction De2 such as to intersect the plurality of second regions 15.

[0426] In this embodiment, the plurality of body regions 32 described above extend in a direction other than the second extension direction De2 such as to intersect the plurality of second regions 15 in the lamination direction. In this embodiment, the plurality of body regions 32 are arrayed at intervals in the first array direction Da1 of the first regions 14 and extend in the first extension direction De1 of the first regions 14. That is, the plurality of body regions 32 are orthogonal to the plurality of second regions 15. In this example, the first array direction Da1 is the a-axis direction (the first direction X), and the first extension direction De1 is the m-axis direction (the second direction Y).

[0427] The plurality of body regions 32 may oppose the plurality of first regions 14 in the lamination direction in a one-to-one correspondence relationship. As a matter of course, the respective body regions 32 may oppose the plurality of first regions 14 in the lamination direction. The plurality of body regions 32 may oppose the plurality of first drift regions 16 in the lamination direction in a one-to-one correspondence relationship.

[0428] As a matter of course, the respective body regions 32 may oppose the plurality of first drift regions 16 in the lamination direction. The plurality of body regions 32 may be arrayed shifted from the plurality of first regions 14 in the first array direction Da1 and may oppose one or both of the first region 14 and the first drift region 16 in the lamination direction.

[0429] As a matter of course, an array direction and an extension direction of the plurality of body regions 32 are changed in accordance with the first array direction Da1 and the first extension direction De1 of the plurality of first regions 14. Therefore, the first array direction Da1 may be the m-axis direction, and the first extension direction De1 may be the a-axis direction. Also, the first array direction Da1 may be a direction other than the a-axis direction and the m-axis direction, and the first extension direction De1 may be a direction other than the a-axis direction and the m-axis direction.

[0430] As a matter of course, the array direction of the plurality of body regions 32 may be a direction other than the first array direction Da1 and the second array direction De2. Also, the extension direction of the plurality of body regions 32 may be a direction other than the first extension direction De1 and the second extension direction De2. That is, the plurality of body regions 32 may intersect both the plurality of first regions 14 and the plurality of second regions 15 in plan view. In this case, a form in which the array direction of the plurality of body regions 32 is one of the a-axis direction and the m-axis direction, and the extension direction of the

[0437] As a matter of course, the array direction of the plurality of gate structures 35 may be a direction other than the first array direction Da1 and the second array direction De2. Also, the extension direction of the plurality of gate structures 35 may be a direction other than the first extension direction De1 and the second extension direction De2. That is, the plurality of gate structures 35 may intersect both the plurality of first regions 14 and the plurality of second regions 15 in plan view. In this case, a form in which the array direction of the plurality of gate structures 35 is one of the a-axis direction and the m-axis direction, and the extension direction of the plurality of gate structures 35 is the other of the a-axis direction and the m-axis direction is not precluded.

[0438] For example, an angle (an absolute value) between the extension direction of the gate structures 35 and the second extension direction De2 may exceed 0° and be not more than 90°. The angle (the absolute value) of the gate structures 35 may have a value falling within any one of ranges of exceeding 0° and not more than 18°, not less than 18° and not more than 36°, not less than 36° and not more than 54°, not less than 54° and not more than 72°, and not less than 72° and not more than 90°. The angle (the absolute value) of the gate structures 35 may be set to a value falling within any one of ranges of 30° ± 5°, 45° ± 5°, and 60° ± 5°.

[0439] In this embodiment, the plurality of gate structures 35 are each arranged such as to straddle two adjacent body regions 32 and each cover the plurality of source regions 33 positioned in one and the other body regions 32. Also, the plurality of gate structures 35 respectively oppose the plurality of second regions 15 (second regions 15) and the plurality of second drift regions 17 in the lamination direction.

[0440] FIG. 40 is a schematic view showing a wafer 50 used in manufacturing the SiC semiconductor device 1A. The wafer 50 is a base material of the base layer 6 and includes an SiC monocrystal. The wafer 50 is formed in a flat disk shape. As a matter of course, the wafer 50 may be formed in a flat rectangular parallelepiped shape. The wafer 50 has a first wafer main surface 51 on one side, a second wafer main surface 52 on the other side, and a wafer side surface 53 connecting the first wafer main surface 51 and the second wafer main surface 52.

[0441] The first wafer main surface 51 corresponds to the upper end of the base layer 6, and the second wafer main surface 52 corresponds to the lower end of the base layer 6. The first wafer main surface 51 and the second wafer main surface 52 are formed of c-planes of the SiC monocrystal. The first wafer main surface 51 is formed of a silicon plane of the SiC monocrystal, and the second wafer main surface 52 is formed of a carbon plane of the SiC monocrystal. The wafer 50 (the first wafer main surface 51 and the second wafer main surface 52) has the off direction Doff and the off angle θoff described above.

epitaxial growth method. Consequently, an epitaxial wafer including the wafer 50 and the first layer 8 as an epitaxial layer is formed.

[0455] In a case where the buffer layer 26 is formed, the first layer 8 is formed with the buffer layer 26 as a starting point by the epitaxial growth method. Consequently, the epitaxial wafer including the wafer 50, the buffer layer 26 as an epitaxial layer, and the first layer 8 as another epitaxial layer is formed. In this case, after the forming step of the buffer layer 26, the first layer 8 may be formed by being continuously crystal-grown from the buffer layer 26 by using the forming step of the buffer layer 26.

[0456] Next, a measurement step of a crystal orientation of the first layer 8 is performed (step S5 in FIG. 41). The measurement step of the crystal orientation of the first layer 8 includes a step of measuring the off angle θoff of the first layer 8. That is, this step includes a step of measuring a crystal orientation of the first axis channel CH1 of the first layer 8.

[0457] The wafer 50 is cut out from an ingot (an SiC ingot) which is a crystalline lump, but there is a risk that an error occurs in the off angle θoff due to a process error. In a case where an error occurs in the off angle θoff of the wafer 50, a process error also occurs in the off angle θoff of the first layer 8, and this becomes an obstacle at the time of a channeling implantation step. Therefore, it is preferable that data (information) of the off angle θoff is acquired before the channeling implantation step, and the channeling implantation step is performed based on the data (information) of this off angle θoff.

[0458] The off angle θoff of the first layer 8 is substantially matched with the off angle θoff of the wafer 50 and the off angle θoff of the buffer layer 26. Therefore, the measurement step of the crystal orientation may be performed on the wafer 50 or the buffer layer 26 before the forming step of the first layer 8. However, from the viewpoint of ensuring accuracy, the measurement step of the crystal orientation is preferably performed on the first layer 8.

[0459] Next, with reference to FIG. 42C, a forming step of a first mask 60 having a predetermined pattern is performed (step S6 in FIG. 41). The first mask 60 is preferably an organic mask (a resist mask). The first mask 60 is arranged on the upper end of the first layer 8 and has a plurality of first openings 61 that expose regions of the first layer 8 in which the plurality of first regions 14 are to be formed.

[0460] Specifically, the plurality of first openings 61 are formed at intervals in the first array direction Da1 in the entire surface of the upper end of the first layer 8 and are each defined as a band extending in the first extension direction De1. That is, the plurality of first openings 61 cross the plurality of device regions 55 and the plurality of intended cutting lines 56 in the first extension direction De1 and expose the plurality of device regions 55 and the plurality of intended

top layer 30 is performed (step S19 in FIG. 41: YES), the top layer 30 is formed with the second layer 9 as a starting point by the epitaxial growth method (step S20 in FIG. 41). In the case where the forming step of the top layer 30 is not performed (step S19 in FIG. 41: NO), this step is omitted.

[0514] Thereafter, with reference to FIG. 42H, the MIS structure 31, the plurality of field regions 38, the interlayer insulating film 40, the gate pad 45, the gate wiring 46, the source pad 47, the drain pad 48, etc., are formed (step S21 in FIG. 41).

[0515] Then, the wafer 50 is cut along the plurality of intended cutting lines 56. Portions of the plurality of first regions 14 positioned on the plurality of intended cutting lines 56 are exposed from the first side surface 5A (the third side surface 5C) as the plurality of first marks Mk1. In a case where the plurality of intermediate regions 25 are formed, a portion of each of the plurality of intermediate regions 25 positioned on the plurality of intended cutting lines 56 is exposed as a part (the upper end portion) of each of the plurality of first marks Mk1 from the first side surface 5A (the third side surface 5C). Portions of the plurality of second regions 15 positioned on the plurality of intended cutting lines 56 are exposed as the plurality of second marks Mk2 from the second side surface 5B (the fourth side surface 5D).

[0516] Also, in a case where the intermediate portion of the second region 15 is cut along the second extension direction De2, a part of the second region 15 is exposed as the first difference mark Md1 from the first side surface 5A (the third side surface 5C). Also, in a case where the intermediate portion of the first region 14 is cut along the first extension direction De1, a part of the first region 14 is exposed as the second difference mark Md2 from the second side surface 5B (the fourth side surface 5D).

[0517] A cutting step of the wafer 50 may include a machining step of the wafer 50. In this case, the wafer 50 is cut along the plurality of intended cutting lines 56 by a dicing blade. Consequently, the chip 2 having the first to fourth side surfaces 5A to 5D that are each constituted of the ground surface is formed.

[0518] The cutting step of the wafer 50 may include a cleavage step of the wafer 50. In this case, a plurality of modified layers (damaged layers) along the plurality of intended cutting lines 56 are formed inside the wafer 50 by a laser light irradiation method, and the wafer 50 is cleaved along the plurality of intended cutting lines 56 with the plurality of modified layers as starting points. Consequently, the chip 2 having the first to fourth side surfaces 5A to 5D that are each constituted of a cleavage surface is formed.

[0519] In the case of the cleavage step of the wafer 50, the plurality of modified layers are preferably formed in a thickness range of the wafer 50 (the base layer 6) with respect to a thickness range of the laminated portion 7. Specifically, the plurality of modified layers are preferably

both sides of the plurality of gate structures 35 in the surface layer portion of the first main surface 3 (the active surface 71). The plurality of source regions 33 are formed in surface layer portions of body regions 32. The plurality of source regions 33 have an n-type impurity concentration (a peak value) higher than that of the second layer 9 (the second drift regions 17). The plurality of source regions 33 may have an n-type impurity concentration of not less than 1×10^{18} cm^{-3} and not more than 1×10^{21} cm^{-3} as a peak value.

[0566] The plurality of source regions 33 extend as a band along the corresponding gate structures 35 in plan view. The plurality of source regions 33 are formed at intervals from bottom portions of the body regions 32 toward the active surface 71 side and oppose the second drift regions 17 across parts of the body regions 32 in the lamination direction. The plurality of source regions 33 define, together with the plurality of second drift regions 17 positioned directly below the source regions 33, the channels (current paths) extending along the wall surfaces of the corresponding gate structures 35.

[0567] The plurality of source regions 33 may oppose the second regions 15 across parts of the body regions 32 in the lamination direction. As a matter of course, the plurality of source regions 33 may be formed at intervals from the second regions 15 toward the second drift regions 17 side (the gate structures 35 side) such as not to oppose the second regions 15 in the lamination direction.

[0568] The SiC semiconductor device 1B includes the plurality of contact regions 34 formed in regions between the plurality of gate structures 35 in the surface layer portion of the first main surface 3 (the active surface 71). The plurality of contact regions 34 are formed in surface layer portions of body regions 32.

[0569] The plurality of contact regions 34 have a p-type impurity concentration (a peak value) higher than the p-type impurity concentration (the peak value) of the plurality of body regions 32. The p-type impurity concentration (the peak value) of the plurality of contact regions 34 is higher than the p-type impurity concentration (the peak value) of the plurality of second regions 15. The plurality of contact regions 34 may have a p-type impurity concentration of not less than 1×10^{18} cm^{-3} and not more than 1×10^{21} cm^{-3} as a peak value.

[0570] The plurality of contact regions 34 are interposed in regions between the plurality of source regions 33 adjacent to each other and each extend as a band along the plurality of gate structures 35. The plurality of contact regions 34 are formed at intervals from the bottom portions of the body regions 32 toward active surface 71 side and oppose the plurality of second regions 15 across parts of the body regions 32 in the lamination direction.

[0571] The plurality of contact regions 34 may oppose the second drift regions 17 across parts of the body regions 32 in the lamination direction. As a matter of course, the plurality of contact

outer surface 72. As a matter of course, the second insulating film 42 may be formed at an interval inward from the peripheral edges of the outer surface 72 and may expose the plurality of second marks Mk2 (the plurality of second regions 15) from the peripheral edges of the outer surface 72 together with the first insulating film 41.

[0590] The SiC semiconductor device 1B includes a plurality of contact openings 43 formed in the interlayer insulating film 40. The plurality of contact openings 43 include the plurality of contact openings 43 (not shown) that expose the plurality of gate structures 35 (the embedded electrodes 77) and the plurality of contact openings 43 that expose the plurality of source regions 33. The plurality of contact openings 43 for the source regions 33 are formed in regions between the plurality of adjacent gate structures 35 and expose the plurality of source regions 33 and the plurality of contact regions 34.

[0591] The SiC semiconductor device 1B includes a side wall structure 79 which is arranged in the interlayer insulating film 40 such as to cover at least one of the first to fourth connecting surfaces 73A to 73D. The side wall structure 79 is arranged on the first insulating film 41 and is covered with the second insulating film 42. The side wall structure 79 moderates a level difference formed between the active surface 71 and the outer surface 72.

[0592] The side wall structure 79 is formed as a band extending along at least one of the first to fourth connecting surfaces 73A to 73D. In this embodiment, the side wall structure 79 is formed in an annular shape (specifically, a quadrangular annular shape) extending along the first to fourth connecting surfaces 73A to 73D such as to surround the active surface 71 in plan view.

[0593] The side wall structure 79 has a portion extending in a film shape along the outer surface 72 and a portion extending in a film shape along the first to fourth connecting surfaces 73A to 73D. In this embodiment, the side wall structure 79 is formed at an interval from the innermost field region 38 to the side of the active surface 71 and opposes the plurality of second regions 15 and the well region 78 across the first insulating film 41 in the horizontal direction and the lamination direction. The side wall structure 79 may oppose the body region 32 across the first insulating film 41.

[0594] As in the case of the SiC semiconductor device 1A, the SiC semiconductor device 1B includes the gate pad 45, the plurality of gate wirings 46, the source pad 47, and the drain pad 48. The drain pad 48 is formed in a configuration as in the case of the first configuration example.

[0595] In this embodiment, the gate pad 45 is arranged on the active surface 71 at an interval from the outer surface 72 in plan view. The gate pad 45 is arranged in a region close to a central portion of one side (the second connecting surface 73B in this embodiment) of the active surface 71 in plan view. As a matter of course, the gate pad 45 may be arranged at a corner portion of

[0602] That is, the embedded electrode 77 opposes the corresponding second region 15 across the insulating film 76 in the lamination direction and opposes the corresponding second drift region 17 across the insulating film 76 in the horizontal direction. The plurality of source regions 33 and the plurality of contact regions 34 described above respectively oppose the corresponding second drift regions 17 across parts of the body regions 32 in the lamination direction.

[0603] FIG. 52 is a cross-sectional perspective view showing the gate structure 35 according to a third configuration example. The plurality of gate structures 35 according to the third configuration example respectively have layouts in which there is no need to consider a positional deviation with respect to the plurality of second regions 15.

[0604] Specifically, with reference to FIG. 52, the plurality of gate structures 35 extend in a direction other than the second extension direction De2 such as to intersect the plurality of second regions 15. In this embodiment, the plurality of gate structures 35 are arrayed at intervals in the first array direction Da1 of the first regions 14 and extend in the first extension direction De1 of the first regions 14. In this example, the first array direction Da1 is the a-axis direction (the first direction X), and the first extension direction De1 is the m-axis direction (the second direction Y).

[0605] The plurality of gate structures 35 may oppose the plurality of first regions 14 in the lamination direction in a one-to-one correspondence relationship. As a matter of course, the respective gate structures 35 may oppose the plurality of first regions 14 in the lamination direction. The plurality of gate structures 35 may oppose the plurality of first drift regions 16 in the lamination direction in a one-to-one correspondence relationship.

[0606] As a matter of course, the respective gate structures 35 may oppose the plurality of first drift regions 16 in the lamination direction. The plurality of gate structures 35 may be arrayed shifted from the plurality of first regions 14 in the first array direction Da1 and may oppose one or both of the first region 14 and the first drift region 16 in the lamination direction.

[0607] As a matter of course, the array direction and the extension direction of the plurality of gate structures 35 are changed in accordance with the first array direction Da1 and the first extension direction De1 of the plurality of first regions 14. Therefore, the first array direction Da1 may be the m-axis direction, and the first extension direction De1 may be the a-axis direction. Also, the first array direction Da1 may be a direction other than the a-axis direction and the m-axis direction, and the first extension direction De1 may be a direction other than the a-axis direction and the m-axis direction.

[0608] As a matter of course, the array direction of the plurality of gate structures 35 may be a direction other than the first array direction Da1 and the second array direction De2. Also, the extension direction of the plurality of gate structures 35 may be a direction other than the first

innermost field region 38 and exposes the entire active region 10 and an inner edge portion of the innermost field region 38.

[0653] The SiC semiconductor device 1C includes a first pad electrode 92 that covers the first main surface 3 in the active region 10. The first pad electrode 92 is formed as an anode pad. The first pad electrode 92 is arranged at an interval inward from the peripheral edges of the chip 2. The first pad electrode 92 is formed in a polygonal shape (a quadrangular shape in this embodiment) along the peripheral edges of the chip 2 in plan view.

[0654] The first pad electrode 92 enters into the contact opening 91 from above the interlayer insulating film 90 and is electrically connected to the first main surface 3 and the innermost field region 38 in the contact opening 91. The first pad electrode 92 forms a Schottky junction with the first main surface 3 (the second layer 9). Consequently, an SBD structure 93 (Schottky barrier diode structure) as a diode structure (a device structural component) is formed in the active region 10.

[0655] The SiC semiconductor device 1C includes a second pad electrode 94 that covers the second main surface 4. The second pad electrode 94 is formed as a cathode pad. The second pad electrode 94 forms an ohmic contact with the base layer 6 exposed from the second main surface 4. That is, the second pad electrode 94 is electrically connected to the first layer 8 (the plurality of first drift regions 16) and the second layer 9 (the plurality of second drift regions 17) through the base layer 6.

[0656] The second pad electrode 94 may cover the entire region of the second main surface 4 such as to be continuous with the peripheral edges (the first to fourth side surfaces 5A to 5D) of the chip 2. The second pad electrode 94 may cover the second main surface 4 at an interval inward from the peripheral edges of the chip 2 such as to expose the peripheral edge portions of the chip 2.

[0657] A breakdown voltage that can be applied between the first pad electrode 92 and the second pad electrode 94 (between the first main surface 3 and the second main surface 4) may be not less than 500 V and not more than 3000 V. The breakdown voltage may have a value falling within any one of ranges of not less than 500 V and not more than 1000 V, not less than 1000 V and not more than 1500 V, not less than 1500 V and not more than 2000 V, not less than 2000 V and not more than 2500 V and not less than 2500 V and not more than 3000 V.

[0658] In a case where the laminated portion 7 having a two-layer structure is employed, the breakdown voltage is preferably set to a value falling within any one of ranges of not less than 500 V and not more than 1000 V, not less than 1000 V and not more than 1500 V, and not less than 1500 V and not more than 2000 V. In a case where the laminated portion 7 having a three-layer

is, in the SBD structure 93 according to the fourth configuration example, restrictions on the layout of the JBS structure and restrictions on the electrical characteristics due to the layout of the super junction structure SJ (the second super junction structure SJ2) are relaxed.

[0674] In this example, the plurality of surface layer regions 95 are formed in the top layer 30. However, in the case where a sufficient space is formed between the first main surface 3 and the column region 12 in the second layer 9 in a state in which the top layer 30 is not formed, the top layer 30 may be omitted.

[0675] FIG. 64 is a cross-sectional perspective view showing the SBD structure 93 according to the fifth configuration example. The SBD structure 93 according to the fifth configuration example has a layout obtained by modifying the layout of the plurality of surface layer regions 95 according to the fourth configuration example. Specifically, the plurality of surface layer regions 95 are arrayed as stripes extending in a direction intersecting the second extension direction De2 of the plurality of second regions 15 in the active region 10.

[0676] In this embodiment, the plurality of surface layer regions 95 are arrayed at intervals in the first array direction Da1 of the first regions 14 and extend in the first extension direction De1 of the first regions 14. In this example, the first array direction Da1 is the m-axis direction, and the first extension direction De1 is the a-axis direction. As a matter of course, the array direction and the extension direction of the plurality of surface layer regions 95 are changed in accordance with the first array direction Da1 and the first extension direction De1 of the plurality of first regions 14. Therefore, the first array direction Da1 may be the a-axis direction, and the first extension direction De1 may be the m-axis direction. Also, the first array direction Da1 may be a direction other than the a-axis direction and the m-axis direction, and the first extension direction De1 may be a direction other than the a-axis direction and the m-axis direction.

[0677] As a matter of course, the array direction of the plurality of surface layer regions 95 may be a direction other than the first array direction Da1 and the second array direction De2. Also, the extension direction of the plurality of surface layer regions 95 may be a direction other than the first extension direction De1 and the second extension direction De2. That is, the plurality of surface layer regions 95 may intersect both the plurality of first regions 14 and the plurality of second regions 15 in plan view.

[0678] For example, an angle (an absolute value) between the extension direction of the surface layer regions 95 and the second extension direction De2 may exceed 0° and be not more than 90°. The angle (the absolute value) of the surface layer regions 95 may have a value falling within any one of ranges of exceeding 0° and not more than 18°, not less than 18° and not more than 36°, not less than 36° and not more than 54°, not less than 54° and not more than 72°, and not less than 72°

and not more than 90°. The angle (the absolute value) of the surface layer regions 95 may be set to a value falling within any one of ranges of 30° ± 5°, 45° ± 5°, and 60° ± 5°.

[0679] Hereinafter, modification examples of the ornamental pattern PT will be described. Hereinafter, an example will be described in which the ornamental pattern PT according to a modification example is employed in the SiC semiconductor device 1A according to the first embodiment, but the ornamental pattern PT according to the modification example can also be applied to the SiC semiconductor device 1B according to the second embodiment and the SiC semiconductor device 1C according to the third embodiment.

[0680] FIG. 65 is a perspective view showing the chip 2 together with the ornamental pattern PT according to a first modification example. In each of the embodiments described above, the example has been described in which the plurality of first marks Mk1 are formed in a side surface different from that of the plurality of second marks Mk2. However, with reference to FIG. 65, the plurality of first marks Mk1 may be formed in the same side surface as the plurality of second marks Mk2. FIG. 65 shows an example in which the plurality of first marks Mk1 are formed in both the first side surface 5A and the second side surface 5B.

[0681] The plurality of first marks Mk1 may have a width (the first width W1) different from the width (the second width W2) of the plurality of second marks Mk2 in the second side surface 5B. The plurality of first marks Mk1 may have a pitch (the first pitch P1) different from the pitch (the second pitch P2) of the plurality of second marks Mk2 in the second side surface 5B. The plurality of first marks Mk1 may overlap one or both of the plurality of second marks Mk2 and the plurality of second spaces Sp2 in the thickness direction in the second side surface 5B.

[0682] The ornamental pattern PT according to the first modification example is realized by forming the plurality of first regions 14 extending in a direction intersecting both the first side surface 5A and the second side surface 5B. For example, the first extension direction De1 of the plurality of first regions 14 is a direction intersecting both the a-axis direction and the m-axis direction. In a case where the plurality of first marks Mk1 are formed in the second side surface 5B, the second difference mark Md2 is not formed in the second side surface 5B.

[0683] FIG. 66 is a perspective view showing the chip 2 together with the ornamental pattern PT according to a second modification example. In each of the embodiments described above, the example has been described in which the plurality of second marks Mk2 are formed in a side surface different from that of the plurality of first marks Mk1. However, with reference to FIG. 66, the plurality of second marks Mk2 may be formed in the same side surface as the plurality of first marks Mk1. FIG. 66 shows an example in which the plurality of second marks Mk2 are formed in both the first side surface 5A and the second side surface 5B.

position of the ingot is irradiated with a laser beam having a focal point (light focus portion) along a predetermined plane direction along the off angle θoff, and the plurality of modified layers along the predetermined plane direction are formed inside the ingot. The plurality of modified layers are portions (laser irradiation marks) in which a part of a crystal structure of the ingot is modified to have different properties, and have fragile physical properties as compared with the other regions.

[0760] In the external force applying step, an external force (stress) is applied to the ingot, and the ingot is separated (cleaved) with the plurality of modified layers as starting points. Consequently, the wafer 50 having the off angle θoff is cut out of the ingot. Examples of the external force (stress) applied to the ingot may include at least one of stress caused by the cutting member, stress caused by a pressing member, stress caused by ultrasonic vibrations, and thermal stress caused by heating and cooling.

[0761] The separation step includes an introduction step of light ions and a thermal treatment step. In the introduction step of light ions, light ions are introduced into a predetermined depth position of the ingot along a predetermined plane direction along the off angle θoff by an ion implantation method (ion beam), and an ion embrittlement portion (an ion embrittlement region) along the predetermined plane direction is formed in the ingot.

[0762] Light ions are ions of an element lighter than carbon (that is, at least one type among hydrogen ions, helium ions, lithium ions, beryllium ions, and boron ions). The light ions are preferably one or both types of hydrogen ions and helium ions. The light ions are particularly preferably hydrogen ions. In this case, an embrittlement portion is formed using a hydrogen embrittlement phenomenon. In the thermal treatment step, a thermal load is applied to the ion embrittlement portion by a thermal treatment, and the wafer 50 having the off angle θoff is separated from the ingot with the ion embrittlement portion as a start point.

[0763] After the preparation step of the wafer 50, the wafer ID 57 is provided in a predetermined portion of the wafer 50 (the first wafer main surface 51). The wafer ID 57 may be formed by irradiating the first wafer main surface 51 with laser light. The wafer ID 57 may be formed by notching the first wafer main surface 51 in a groove shape with a needle, etc. The wafer ID 57 may be printed on the first wafer main surface 51 with an ink, etc. The wafer ID 57 may be formed by digging into the first wafer main surface 51 by an etching method.

[0764] After the wafer ID 57 is provided, an acquisition step of the wafer ID 57 is performed by the first ID reading device 120 (step S32 in FIG. 74). The wafer ID 57 acquired by the first ID reading device 120 is stored in the transfer-side control device 124.

[0765] Next, the forming step of the first layer 8 as the epitaxial layer is performed by the epitaxial